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Selective area growth of high quality InP on Si (001) substrates

G. Wang,^{1,2,a)} M. R. Leys,¹ R. Loo,¹ O. Richard,¹ H. Bender,¹ N. Waldron,¹ G. Brammertz,¹ J. Dekoster,¹ W. Wang,¹ M. Seefeldt,² M. Caymax,¹ and M. M. Heyns^{1,2}

¹IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

²Department of MTM, KULeuven, Kasteelpark Arenberg 44, Box 2450, Leuven B-3001, Belgium

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In this work, we demonstrate the selective area growth of high quality InP layers in submicron trenches on exactly (001) oriented Si substrates by using a thin Ge buffer layer. Antiphase domain boundaries were avoided by annealing at the Ge surface roughening temperature to create additional atomic steps on the Ge buffer layer. The mechanism of Ge surface atomic step formation and the corresponding step density control method are illustrated. The elimination of antiphase boundaries from the optimized Ge buffer layer, together with the defect necking effect, yield defect-free top InP layers inside the trenches. © 2010 American Institute of Physics. [doi:10.1063/1.3491554]

Selective area growth (SAG) is widely used in fabricating III–V heterojunction devices and photonic integrated circuits.^{1,2} Recently, there has been great interest in integrating InP and other high mobility materials such as InGaAs on Si substrates to make high performance complementary metal oxide semiconductor (CMOS) devices. One approach to integrate these materials on Si substrates is SAG in shallow trench isolation (STI) structures.^{3,4} By utilizing the defect necking effect in submicron trenches, extended defect-free materials can be obtained.⁵ SAG also makes it possible to fabricate Ge p-channel metal oxide semiconductor (pMOS) devices in the vicinity of III–V n-channel MOS (nMOS) devices so that high performance CMOS devices can be realized on a single Si substrate.⁶ In addition, the integration of optoelectronic devices on a Si chip will also likely need SAG of III–V materials on dedicated Si areas.

For III–V compound semiconductor epitaxial layers grown on Si (001) or Ge (001) substrates, the reduced symmetry of III–V compounds induces antiphase (domain) boundaries (APBs) which cause deep-level defects in the band gap.⁷ These APBs are either in {111} or in {110} planes. The APBs in {111} may get annihilated with increasing layer thickness⁸ while the APBs in {110} will penetrate to the surface.⁹ To avoid APBs, miscut Si (001) or Ge (001) substrates are commonly used.^{10,11} Off-oriented Si (001) or Ge (001) substrates provide a high density of atomic steps that form double-B atomic steps at elevated temperatures, preventing APB formation.¹² However, miscut substrates induce additional issues in SAG, such as crystal quality and surface morphology dependence on trench orientations, resulting in a significant barrier for their application in CMOS device fabrication.^{4,13} In addition, miscut Si (001) substrates are not standard in Si CMOS industry. Consequently, it is of great importance to obtain APB-free III–V layers on exactly (001) oriented Si substrates.

It has been reported that the atomic steps can be artificially created on exactly (001) oriented Si substrates.⁹ However, it is well known that, compared to Si, the double steps on a Ge surface are more stable and easy to form with a lower thermal budget.¹⁴ We will show in this letter, in the case of SAG, especially in submicron trenches, the atomic

steps on a Ge surface can be created in a controlled manner so that the formation of double atomic steps is energetically favored. Via this mechanism, we have eliminated APBs in InP grown in Si (001) STI trenches by using a thin Ge buffer layer.

Trenches with widths from 0.1 to 0.2 μm (trench lengths from 0.5 to 100 μm) were fabricated on 200 mm Si (001) wafers by using a typical SiO₂ STI patterning scheme routinely employed in Si-CMOS technologies. The thickness of STI-SiO₂ is 300 nm. After a standard wet clean and an HF dip, the Si was etched back to a depth of ~ 400 nm by HCl vapor phase etching at 850 °C and 10 Torr in an ASM-Epsilon™ 2000 reactor. An *in situ* H₂ bake was used at 850 °C for the removal of the Si native oxide.¹⁵ Subsequently, a thin (~ 30 nm) Ge layer was grown at 450 °C and atmospheric pressure using GeH₄ (1% in H₂) in a H₂ carrier gas. About 10% of the total Si wafer surface was exposed for the Ge and the subsequent InP deposition.

After the thin Ge layer deposition, the wafers were cleaved into 50 \times 50 mm² pieces and loaded into an Aixtron/Thomas Swan close coupled showerhead metal organic vapor phase epitaxy reactor. Trimethylindium was used as the group-III element precursor. For the group V element, tertiarybutylarsine (TBAs) and tertiarybutylphosphine were available. Before the growth, a pre-epi bake at 740 °C and reduced pressure was carried out using TBAs and H₂ as a carrier gas. The purpose of this bake is to remove the Ge native oxide and to promote double step formation. Following this bake, the temperature was ramped down to 420 °C to grow ~ 30 nm InP seed layer. After the growth of the InP seed layer, the temperature was ramped to 640 °C for the bulk InP layer growth. More details of the growth optimization can be found in Refs. 4 and 13. The crystalline defects were characterized with transmission electron microscopy (TEM).

This thin Ge buffer layer is important as Ge double steps are more stable and can be formed at a much lower temperature compared to that of Si.^{16,17} The atomic step creation mechanism is schematically shown in Fig. 1. A concave surface can be obtained by over etching the Si during the HCl vapor phase etch step.^{4,13} Si facets may form in the bottom of the trenches during the Si etch [Fig. 1(b)]. In the wider trenches [>1 μm , depicted on the right side of Fig. 1(b)],

^{a)}Electronic mail: wangga@imec.be.

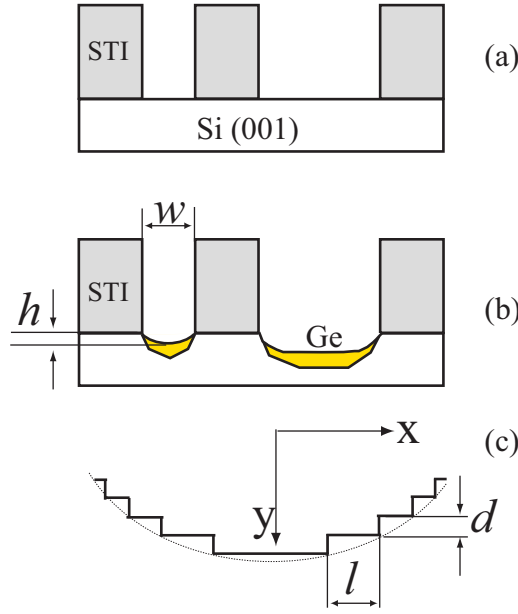


FIG. 1. (Color online) Schematics of Ge surface step creation in STI trenches of different widths. (a) STI trenches are defined on a Si (001) substrate by standard Si STI processing. (b) The Si is over etched so that a concave surface is obtained then a thin Ge layer is deposited followed by annealing. The zoom-in view of atomic steps on the Ge surface at the center of a submicron trench is shown in (c). The parameters associated with the atomic steps are shown, trench width w , atomic step height, d , terrace width, l , and the maximum distance from the Ge surface to the reference Si surface, h .

the (001) surface still remains in the center of the trench. In the next step, a thin Ge layer is grown on the faceted Si surface. The Ge epitaxial layer follows the starting Si surface but smoothens the sharp intersection between two adjacent facets as a result of the different Ge growth rates on the facets. To create a relatively uniform step density on the Ge buffer layer, a bake at an elevated temperature is used. At about 700 °C, the Ge surface roughening temperature, the step formation energy approaches zero, facilitating surface step formation.¹⁸ As a result of the high temperature anneal, the Ge surface tends to evolve into a rounded continuous surface. The atomic step density on the rounded Ge surface can be estimated analytically by assuming a given surface profile. In a submicron trench, the surface profile can be considered elliptical,

$$\frac{x^2}{(\frac{w}{2})^2} + \frac{y^2}{h^2} = 1, \quad (1)$$

with w being the trench width and h the maximum distance from the Ge surface to the reference Si surface [see Fig. 1(c)]. x and y are the coordinates of the point of interest. The surface step density, ρ , is given by $\rho = |y'/d|$ with y' being the slope of the surface and d the step height. The surface step density is,

$$\rho = \left| \frac{y'}{d} \right| = \left| \frac{4hx}{dw^2\sqrt{1 - (\frac{2x}{w})^2}} \right|. \quad (2)$$

From Eq. (2), it can be seen that surface step density depends on the trench width, w , as well as the maximum distance between the Ge surface and the Si reference level, h . In general, the Ge surface step density at the edge of the trench is much larger than that at the trench center. Accord-

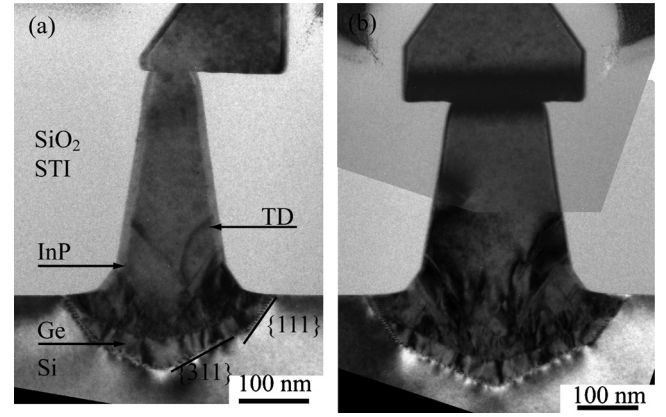


FIG. 2. Bright field cross- section TEM images ($g[004]$) of InP grown in the 100 nm (a) and 200 nm (b) wide STI trenches. {111} and {311} Si facets were obtained after Si etch with HCl vapor. TDs are confined in the bottom of the trenches.

ing to the double step formation energetics on vicinal Ge (001) surfaces, to ensure the formation of Ge double steps, a minimum step density of 0.14 nm^{-1} (equivalent to the step density on a 2° off-oriented vicinal surface) in the vicinity of $\sim 4 \text{ nm}$ ($x \approx 4 \text{ nm}$) is required.^{14,16} From Eq. (2), it is evident that larger h is needed for wider trenches.

The concept shown in Fig. 1 is demonstrated experimentally. Figure 2 shows the cross-section TEM images of 100 nm and 200 nm wide trenches after InP growth. Si {111} and {311} facets are observed after the Si recess. The sharp edges could cause voids if InP was directly grown on the faceted Si surface.³ The thin Ge buffer layer mitigates the sharp edges and a relatively round surface is obtained. From the slope of the Ge surface, we can deduce that the step density near the trench center is significantly larger than 0.14 nm^{-1} in both trenches. This rounded Ge surface is crucial for several reasons. First of all, the rounded surface creates a high density of single atomic steps. Upon annealing at a temperature above the Ge surface roughening point, single surface steps migrate and merge into double steps. The formation of double steps is essential to avoid any APB formation. Second, the rounded Ge surface removes facets and the subsequent InP growth follows the Ge surface in a step flow growth mode and thus different crystal orientation can be avoided. As a result, no void formation occurs. Finally, the atomic steps on the rounded Ge surface facilitate InP nucleation thereby retarding islanding, which results in an improved InP nucleation layer. The TEM images show no trace of APBs which means that the artificial Ge surface steps have transformed into double steps. In addition, all the threading dislocations (TDs) are confined at the bottom of the trench. With the suppression of APBs and by the extended defect necking effect, a defect-free InP layer is obtained at the top of the trenches.

To further confirm the absence of APBs, we performed a TEM analysis along the length of a 200 nm trench in order to cover a larger area. Figure 3 shows the cross-section TEM image of the same trench as in Fig. 2(b). No APBs are observed in this long trench. Furthermore, a flat and uniform InP layer grown on the smooth Ge buffer layer along the complete length of the trench is obtained. This uniform Ge layer thickness maintains the Ge surface profile and the surface atomic step density. From Eq. (2), if the local

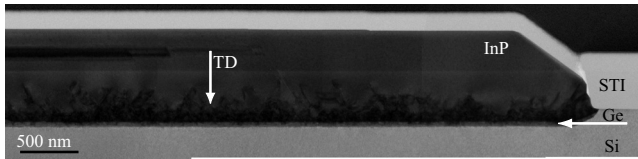


FIG. 3. Cross-section TEM image taken along the 200 nm trench in Fig. 2(b). The twin defects on the left side of the overgrown InP are believed to be caused by the imperfection of the STI side walls that disturbs the crystal growth. The vertical line on the right part of InP is an artifact of the TEM sample preparation.

Ge thickness, h , changes, the corresponding atomic step density will vary. Figure 3 suggests that the Ge surface profile and the surface step density are well controlled even in a long trench.

In summary, we have demonstrated the growth of high quality InP in submicron STI trenches on exactly (001) oriented Si substrates. The APBs are avoided by artificially creating atomic steps on a rounded thin Ge buffer layer by annealing the Ge surface at the roughening temperature. An analytical model is given to determine the surface step density as a function of the trench width and the maximum distance between the Ge surface and Si reference level. This provides a method to control the atomic step density. Our approach solves the long-standing issue regarding APB formation in the growth of III–V epitaxial layers on exactly (001) oriented elementary semiconductor substrates. The resulting defect-free top InP layers enable the fabrication of III–V channel-based devices after a chemical mechanical polishing step to planarize the InP surface. This work also gives insight into the SAG of other III–V zinc-blende compound semiconductors on Si (001) substrates.

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