Timing and design optimization of RISC-V on flexible technologies

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Introduction

Thin-film electronics is a cutting-edge technology that uses thin-film semiconducting layers on flexible plastic substrates to create transistors and circuits. This technology allows the electronic properties and functionality of flexible ICs to remain intact even when folded or rolled. However, using thin-film transistors comes with certain challenges. For example, the semiconductor used in this thesis is IGZO, resulting in n-type-only transistors, which requires unipolar logic. Flexible chips also operate at much lower frequencies compared to standard silicon chips. This master's thesis researches design and timing optimizations of a flexible chip based on TFT technology using a RISC-V architecture.

Measurements and methods

First, different topologies that can be used for TFTs were analyzed. Next, the design process started with the creation of a standard cell library. This library was then utilized in the digital design flow (Fig. 3), which is the process that is used to progress the initial design of cells and architecture to a design that is suitable for manufacturing. The final layout of the chip is shown in Fig. 4. Finally, the impact of clock tree synthesis was investigated on the timing performance of the chip through the use of simulation and analysis.

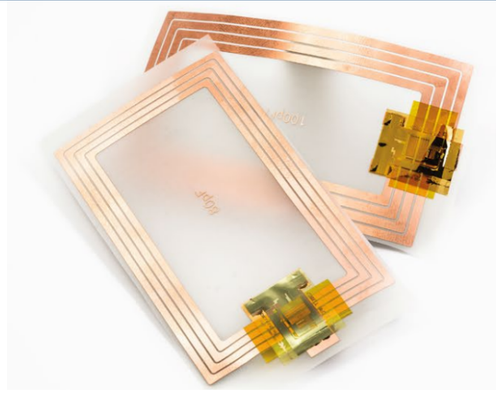

Fig. 1: Photograph of a flexible TFT-based NFC tag [1]

Design topology

Standard CMOS logic cannot be used in the design. Therefore pseudo-CMOS (Fig. 2) is used, which is a topology for unipolar logic.

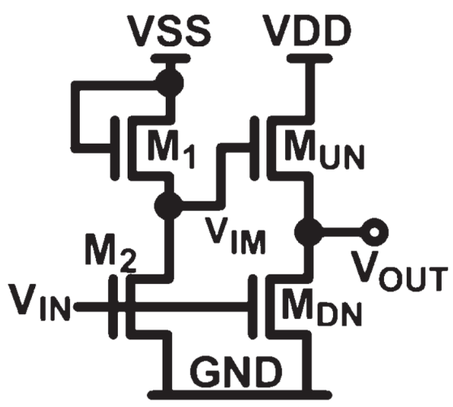

Fig. 2: A pseudo-CMOS inverter [2]

Design flow

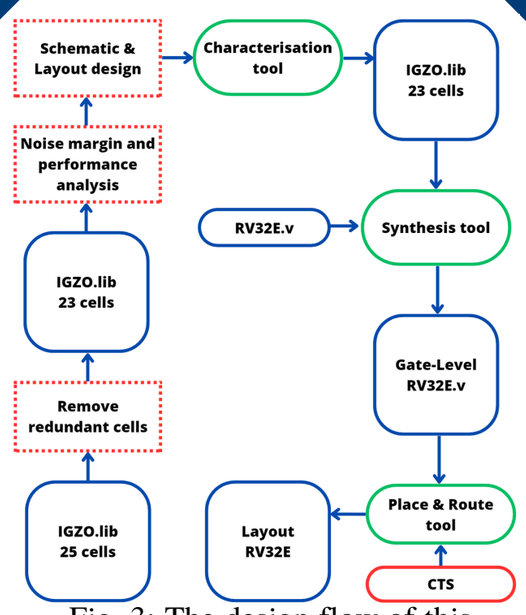

Fig. 3: The design flow of this thesis

Final design

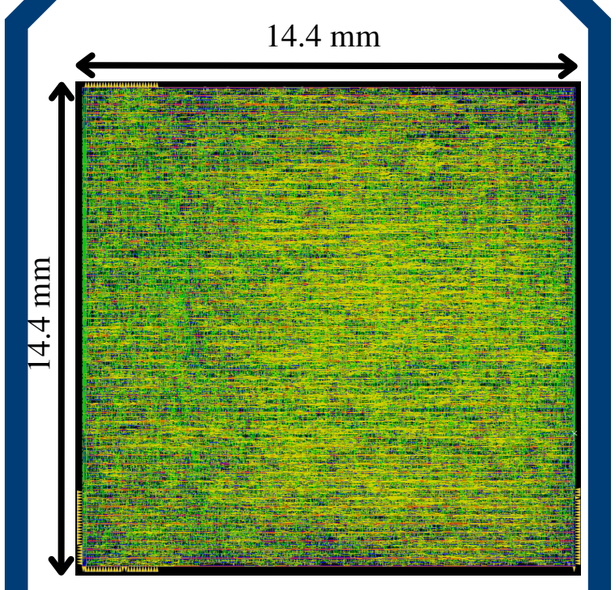

Fig. 4: Final layout of the flexible RV32E

CTS results

Fig. 5 displays the percentage increase in maximum frequency for different designs, indicating that implementing a clock tree is extremely beneficial to achieve faster digital IC cores.

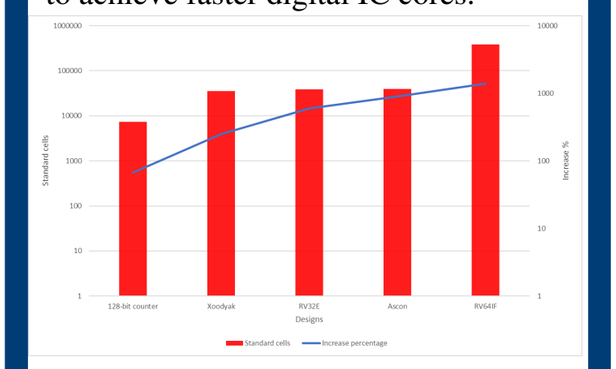

Fig. 5: Timing analysis of an RV32E at different frequencies

Conclusion

In conclusion, it was observed that for our test that the implementation tool reports an increase in frequency of between 1.5 and 10 times the original frequency without CTS. Performing CTS also had a negligible impact on both area and power consumption for TFT-based chips.

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[1] Myny, K. The development of flexible integrated circuits based on thin-film transistors. Nature Electronics, vol 1, pp. 30–39, 2018
[2] T.-C. Huang, K. Fukuda, C.-M. Lo, Y.-H. Yeh, T. Sekitani, T. Someya, and K.-T. Cheng, "Pseudo-cmos: A design style for low-cost and robust flexible electronics," IEEE Transactions on Electron Devices, vol. 58, no. 1, pp. 141–150, 2011

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