Mitigation of potential-induced degradation in perovskite solar cells using overnight voltage recovery

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PID Mitigation in Perovskite Solar Cells using Overnight Voltage Recovery

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Abstract

Potential-induced degradation (PID) poses a critical threat to the long-term stability of perovskite solar cells (PSCs), driven by sodium ion (Na^+) migration from soda-lime glass (SLG) substrates to the active layer. This study examines the effect of periodically interspersing PID stress with overnight voltage recovery or shelf storage on 48 PSCs during a 500-hour experimental protocol comprising 150 hours of accumulated PID stress and 350 hours of accumulated recovery or storage. Overnight shelf-stored devices degraded to 79% normalized efficiency, while those subjected to overnight voltage recovery maintained 94%. These results highlight overnight voltage recovery as an effective PID mitigation strategy, preserving PSC performance and advancing their stability for practical applications.

Keywords: Perovskites, Recovery, Efficiency, Na, Potential-induced degradation

1 Introduction

In the last decades, thin-film perovskite solar cells (PSCs) have emerged as a promising technology due to their superior photo-electronic properties, including micrometer-scale diffusion lengths surpassing their sub-micrometer thickness and highly tunable bandgaps [1–4]. However, PSCs face significant challenges in terms of environmental stability, with performance susceptible to external factors like moisture, oxygen exposure, light, and elevated temperatures [1–4]. These stability issues currently hinder the commercialization of PSCs, highlighting the need for further advancements in long-term stability [3–5].

Additionally, when deployed in field conditions, perovskite devices can be subject to system-level degradation processes, such as potential-induced degradation (PID). Several studies have identified PID as a significant and aggressive degradation mechanism in perovskite devices, further compromising the long-term stability [6–13]. An overview of the literature is presented by Table S1 in the supporting information.

PID occurs in photovoltaic (PV) devices when they are subjected to high negative potentials (e.g., -1000 V) relative to their grounded frame [14]. Studies have identified that PID in PSCs arises from the migration of positively charged sodium ions (Na^+) from soda-lime glass (SLG) substrates toward the PSC, driven by the electric field induced in these conditions [6, 7, 9, 11, 12]. Previous studies have demonstrated that reversing the voltage stress at the conclusion of a continuous PID stress test facilitates the migration of Na^+ ions back into the SLG substrate, significantly recovering device performance [7–10].

PID has already been extensively investigated in crystalline silicon (c-Si) PV because it has led to substantial financial losses in large-scale PV installations [15]. Accordingly, numerous mitigation and prevention strategies have been developed. One effective mitigation method is to apply a reverse potential during the night, which drives Na^+ out of the PV stack and back into the SLG, thereby immediately recovering performance [16–18]. This strategy's success has led to commercial solutions from various companies, offering systems that automatically reverse voltage during nighttime to mitigate PID [19, 20].

This study evaluates the effectiveness of an overnight reverse-voltage recovery strategy on triple-cation (3C) p-i-n PSCs as a potential method to mitigate PID and enhance their long-term stability. During the day, 48 PSCs undergo PID stress, while at night, one group is subjected to reverse-voltage recovery, and another group is stored without any stress.

2 Methods and Materials

While previous studies primarily investigated post-experiment voltage recovery, this study evaluates the effectiveness of interspersing PID stress during the day with overnight voltage recovery as a proactive approach to mitigate PID in PSCs. To this end, six substrates, each comprising 12 PSCs, were constructed, resulting in the fabrication of 72 p-i-n PSCs utilizing 3C perovskite with an active area of

0.125 cm^2. All devices maintain a consistent PSC design with an identical material stack: SLG/indium tin oxide (ITO)/nickel oxide (NiO_X)/self-assembling monolayer (SAM)/3C perovskite/lithium fluoride (LiF)/C60/bathocuproine (BCP)/copper (Cu). The perovskite layer was synthesized using the following composition: $Cs_{0.05}FA_{0.85}MA_{0.10}PbI_{2.90}Br_{0.10}$. Additional details are provided in the supporting information.

The PID stress setup was placed in a nitrogen (N_2) environment at room temperature to exclude other unwanted degradation mechanisms such as moisture, oxygen, or temperature, as explained in our previous study [10]. In this setup, PID stress was applied by short-circuiting the PSCs and connecting them to a -1000 V potential while a grounded copper block was pressed onto the glass [10]. The PID-stressed devices were divided overnight into two groups of 24 PSCs: one group was periodically removed from the setup and stored on a shelf, while the voltage stress was inverted to the other group to promote voltage recovery. It is crucial to emphasize that all samples remained in complete darkness throughout the entire experiment. Consequently, the terms "day" and "night" are used solely to simulate practical operating conditions and should be interpreted as indicative of timing rather than actual exposure to sunlight.

Additionally, a third group of 24 PSCs served as the experimental control, remaining stored on a shelf for the entire duration of the experiment without any exposure to voltage stress. It is crucial to highlight that all samples in this experiment were maintained under identical conditions: a controlled N_2 environment, room temperature, complete absence of light, and no encapsulation.

This experiment was conducted over a total duration of 500 hours and comprised 15 cycles. Each cycle consisted of 10 hours of PID stress followed by 12 hours of voltage recovery or storage on the shelf, as illustrated in 1. The experimental protocol was adapted to accommodate laboratory access constraints, particularly during weekends when access was restricted, resulting in samples remaining under continuous voltage recovery or shelf storage conditions. As a result, the experiment accumulated 150 hours of PID stress and 350 hours of storage. This approach allowed for the evaluation of the effects of PID stress combined with recovery/storage periods on the performance and stability of the PSCs.

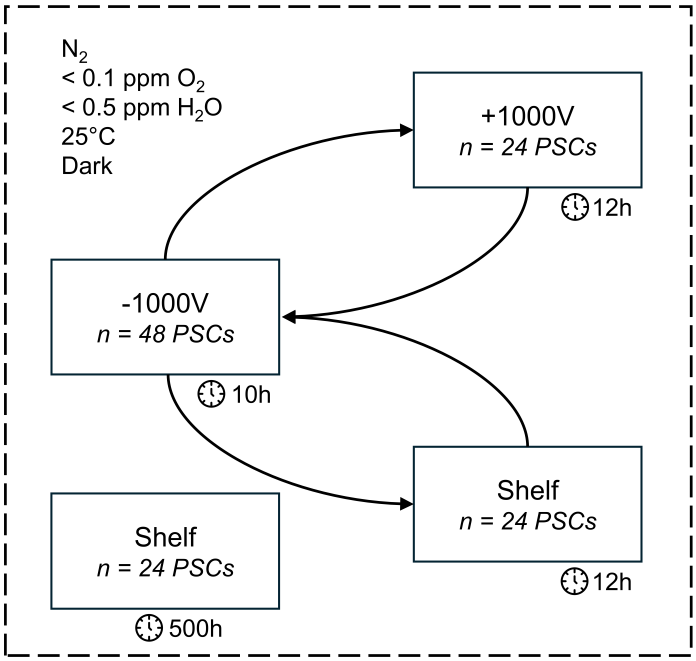

Fig. 1 A graphical representation of the PID cycling procedure: 48 samples underwent 10 hours of PID stress daily. Following this, half of the samples were subjected to a +1000 V reverse voltage stress overnight, while the other half was stored on the shelf under controlled conditions. Additionally, 24 PSCs served as a control group, remaining stored on the shelf under identical conditions throughout the entire experiment without exposure to voltage stress.

In order to gain insights into the degradation mechanism, intermediate characterization was performed using current density-voltage (JV) measurements in a N_2-filled glovebox. All JV measurements were conducted under one sun illumination (i.e., 1000 W/m^2, AM 1.5G) provided by a 450 W xenon lamp (Abet Sun 2000). The temperature of the devices was maintained at 30°C during the measurements using a fan. Prior to device characterization, the illumination intensity was calibrated using a WPVS reference solar cell (type: RS-ID-4) from Fraunhofer ISE. Each JV sweep covered a voltage range using a reverse scan going from 1.3 V to -0.2 V in steps of 0.01 V with a delay of 0.01 s (0.8 V/s). During the first 100 hours of PID stress (i.e., up to 255 hours into the experiment), two JV characterizations were conducted daily. Subsequently, one JV characterization was performed daily until the end of the study. This measurement protocol enables precise tracking of device performance and degradation behavior.

3 Results and discussion

In order to assess whether PID cycling can mitigate the effects of the PID mechanism, intermediate JV measurements were performed throughout the experiment. Figure 2 shows the normalized efficiencies of three groups: control devices, PID stressed devices

with overnight voltage recovery, and PID stressed devices with overnight storage on the shelf, represented by green, grey, and red, respectively.

The graphs clearly indicate that samples subjected to PID stress followed by overnight shelf storage experienced significant degradation over time. After 29 hours of accumulative PID stress and 23 hours of shelf storage, their average normalized efficiency dropped below the 5% stability threshold [21].

By the end of the experiment (i.e., after 150 hours of accumulated PID stress and 350 hours of shelf storage), all samples in this group had degraded to an average normalized efficiency of 79%. In a previous study, continuous PID stress was applied for 300 hours to samples with an identical perovskite stack, yielding an average normalized efficiency of 85% after 150 hours of stress [10]. Comparing these results reveals that the degradation observed in the current experiment is 6% larger.

It is hypothesized that the observed 6% increase in degradation is due to the extended 500-hour duration of the experiment, which provided additional time for the diffusion of migrated Na^+ ions, thereby exacerbating the deterioration of the PSCs' performance. This hypothesis is supported by the observation that degradation continued even when the samples were stored on the shelf. Notably, the experiment duration was 200 hours longer than in our previous study [10]. Consequently, a portion of the 6% efficiency difference may be attributed to shelf instability, as indicated by the 3% efficiency loss observed in the control samples.

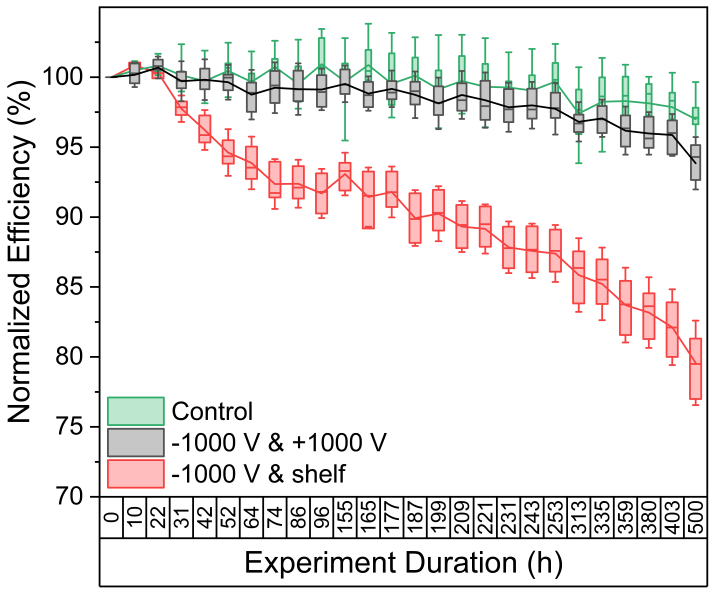

Fig. 2 Normalized efficiency of control devices in green, and PID stressed devices with intermediate voltage recovery and shelf storage in grey and red, respectively.

In contrast, the samples subjected to overnight connection to +1000 V exhibited negligible degradation during the first 253 hours of the experiment (corresponding to 89 hours of accumulated PID stress and 154 hours of voltage recovery). Degradation only became significant towards the end, with the efficiency crossing the 5% stability threshold, yielding an average normalized efficiency of 94% [21]. Although the duration of voltage recovery significantly exceeded the period of PID stress, some degradation was still evident.

Previous studies have demonstrated that applying an inverted voltage (i.e., voltage recovery) following continuous PID stress can significantly restore the performance of PSCs [6, 8–10]. It is suggested that this inverted electric field drives the Na^+ ions out of the perovskite absorber back toward the SLG substrate, as presented by the microstructural analysis from Nakka et al.[9]. In this study, the samples were subjected to PID stress for no longer than 10 hours before initiating the recovery process. Therefore, the authors believe that this limited duration was insufficient for the migrated Na^+ ions to accumulate significantly, as reversing the electric field repelled the ions back into the substrate.

To further elucidate the degradation mechanisms, a detailed analysis of the JV characteristics is performed. Table 1 provides a concise summary of the average values and standard deviations of the key performance metrics, facilitating a comparison of the degradation effects across all PSC groups.

Table 1 Summarizing table depicting the average normalized values of power conversion efficiency (PCE), short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), and fill factor (FF) and standard deviation for 24 PSCs per group, at the end of the experiment.

Storage	PCE	J_{SC}	V_{OC}	FF
Control	0.97 ± 0.02	0.96 ± 0.02	1.03 ± 0.01	0.98 ± 0.02
+1000 V	0.94 ± 0.02	0.95 ± 0.02	1.02 ± 0.01	0.96 ± 0.02
Shelf	0.79 ± 0.03	0.85 ± 0.02	1.02 ± 0.01	0.92 ± 0.02

What stands out from Table 1 is the similarity between the average values of the control devices and the PID-stressed ones with overnight voltage recovery. In both cases, the primary contributors to the power conversion efficiency (PCE) losses were reductions in short-circuit current density (J_{SC}) and fill factor (FF). For the control devices, these decreases can likely be attributed to the natural shelf stability of the samples over time. Notably, the extended duration of this experiment underscores the persistent challenge of achieving long-term stability in PSCs.

The 3% difference in average PCE loss between the control samples and the +1000 V samples is suggested to result from the continuous in and out-migration of Na^+ ions. However, further microstructural analysis is required to gain more precise insights into the underlying degradation mechanisms within the perovskite device.

Similarly, the degradation trends observed in the samples stored on the shelf between PID stress cycles are also consistent with previous findings [10]. For these

samples, the decline in PCE is again mainly driven by a reduction in J_{SC}, with a minor contribution from losses in FF.

Interestingly, all devices, including the control group, exhibited an increase in open-circuit voltage (V_{OC}). Since this phenomenon was observed across all groups, it suggests that the increase in V_{OC} is intrinsic to the perovskite material itself rather than a direct result of PID stress. Additionally, all groups, each consisting of 24 PSCs, demonstrated comparable standard deviations, reflecting a high level of consistency and reproducibility in the experimental results.

While Table 1 provides a detailed summary of the PID-induced changes in key photovoltaic parameters, a more nuanced understanding of the underlying degradation mechanisms will require an examination of the JV characteristics. Figure 3 presents the JV characteristics of both PID-stressed groups at the beginning and end of the experiment, corroborating the data summarized in Table 1, while offering additional insights into the mechanisms of performance degradation. A particularly noteworthy observation is the pronounced reduction in shunt resistance at the end of the experiment, which is especially evident in the samples stored under shelf conditions, as shown in Figures S1 and S2 in the supporting information.

This significant decline in shunt resistance aligns with the findings of Brecl et al. and Zhang et al., who employed 3D time-of-flight secondary ion mass spectroscopy (ToF-SIMS) to visualize the migration pathways of Na^+ ions through perovskite solar cells [7, 12]. Combining this literature with the current findings, it is suggested that the formation of these Na^+ ion pathways could be the primary cause of the observed reduction in shunt resistance, as Na^+ accumulation likely leads to the development of additional leakage channels within the device, exacerbating the degradation of electrical performance.

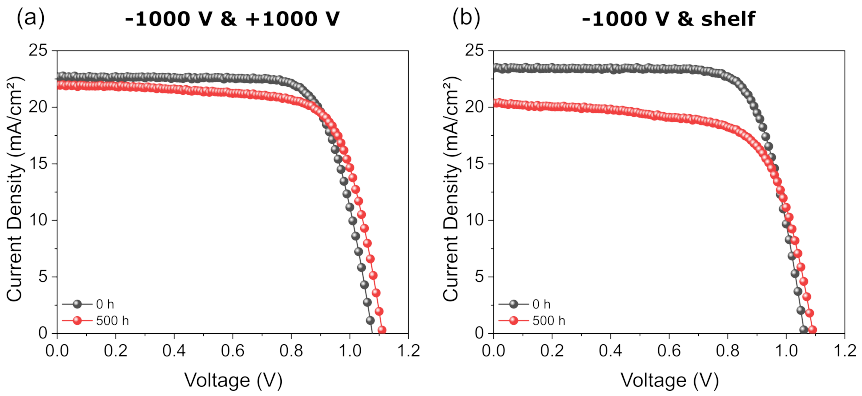

Fig. 3 JV graphs of (a) PID stressed and voltage recovered PSC and (b) PID stressed and shelf-stored PSC in the beginning and at the end of the experiment.

4 Conclusion and outlook

Research on PID-stressed c-Si solar cells has demonstrated that overnight voltage recovery significantly enhances long-term system performance, driving the development of commercial devices designed to utilize this mitigation approach. Motivated by these findings, this study examined the impact of interspersing PID stress with overnight voltage recovery and compared it to the effects of overnight shelf storage. The experiment involved 3C p-i-n PSCs, with 48 devices subjected to PID stress during the day and subsequently divided into two groups: one undergoing overnight voltage recovery and the other stored on the shelf. Additionally, 24 PSCs were maintained as a control group and stored on the shelf under identical environmental conditions without exposure to voltage stress. The experiment consisted of 15 cycles over a total duration of 500 hours, comprising 150 hours of accumulated PID stress and 350 hours of either voltage recovery or shelf storage. Throughout the study, all devices were maintained under inert conditions at room temperature.

The results clearly show that PID continues in shelf-stored samples, with a final average normalized efficiency of 79%, representing a 6% more significant efficiency loss than our previous study, which reported 85% normalized efficiency after 150 hours of continuous PID stress [10].

In contrast, samples subjected to overnight voltage recovery exhibited substantial PID resistance, maintaining an average normalized efficiency of 94% by the end of the experiment. Although the recovery duration exceeded the PID stress duration, the total degradation surpassed the 5% stability threshold [21]. Given the experiment's extended duration of 500 hours, some degradation may relate to intrinsic sample stability, as indicated by the control devices, which reached 97% normalized efficiency at the end of the experiment.

Overall, this experiment, involving 15 cycles on a large number of PSCs evaluated under controlled environmental conditions over an extended duration of 500 hours, demonstrated consistent results with a relatively low standard deviation. Hence, these findings strongly confirm that overnight voltage recovery is a highly effective strategy for mitigating PID in PSCs.

These findings offer valuable insights that could enhance the long-term stability of perovskite devices in practical applications, supporting their sustained performance in real-world environments. Additional research incorporating hysteresis measurements and post-experiment microstructural analysis can expand upon the presented results and provide deeper insights into the underlying mechanisms. Furthermore, since PV panels in practical applications undergo temperature fluctuations between daytime heating and nighttime cooling, and PID is mainly driven by Na^+ diffusion, future research should investigate the impact of temperature variations within this mitigation strategy.

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Declarations

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