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Alternative gate dielectric materials

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The semiconductor industry is facing the challenging task of finding a candidate to replace silicon oxide, which has been the CMOS gate dielectric of choice for more than 50 years. A material with a dielectric constant (k) higher than SiO_2 will allow making the dielectric thicker by a factor of $k/k(SiO_2)$, hence lowering the gate current leakage levels, and this without reduction of the capacitance and thus performance.
The k-value is, however, only one of a list of requirements that includes thermal and chemical stability, a wide bandgap, limited interfacial layer formation, a controllable etch behavior, correct and stable threshold voltage, and a good reliability (i.e. over a 10-year life time).
At present, the semiconductor industry's focus is on HfO_2 and $HfSiO_x$, but parallel to the main stream development of HfO_2 and $HfSiO_x$, material screening of alternate dielectrics continues. The interest in these alternative materials arises from the fact that several issues remain with the Hf-based dielectrics. Among the issues are, targeting the correct threshold voltage, the limited improvement in k-value for $HfSiO_x$, and the necessity of nitridation to stabilize the material and prevent phase separation. In addition, high-mobility substrates such as Germanium or GaAs are of high interest to improve transistor performance, but the Hf-based materials have issues related to negative interactions and stability in combination with these substrates.
There are several considerations that need to be addressed when screening potential high-k dielectrics: The availability and manufacturability of the material (and though a CVD based deposition technique is preferred in the end, initially any deposition technique that provides reasonable quality materials is suitable); the production of high k blanket films that have properties independent of the deposition technique and consistent with the same material deposited on patterned wafers; and the ability to have the material easily integrated into a standard CMOS process flow (i.e. controllable etch process, thermal stability, etc..).
To allow rapid screening of potentially interesting materials, we are exploring the use of the aqueous solution-gel method. Metal oxides are complexed by a chelating agent to eventually form stable aqueous solutions that are spincoated on a silicon substrate with a surface pretreatment of choice.
Since the source material is the metal oxide itself, in theory there are no limitations to the materials that can be tested (and mixtures thereof). Preliminary electrical results for Nd_2O_3, Pr_2O_3, Eu_2O_3, and Sm_2O_3 are promising within in an EOT range of 3 to 8.5 nm (~2nm SiO_2 as starting surface), as shown for Nd_2O_3 in Figure 1. Experiments are ongoing to validate this technique for lower EOT values and different materials.
One class of materials being investigated and reported on are the rare earth scandate materials ($REScO_x$). Results obtained by Pulsed Laser and E-Beam Deposition suggest these materials have a k-value comparable to HfO_2 in combination with a high thermal stability.[1,2]
Further, we have developed a Metal Organic CVD-type (AIXTRON AVD®) process for these oxides using $Dy(mmp)^3$ and $Sc(mmp)^3$ as precursors.[3] Although some issues regarding reactivity and purity of the precursors remain, initial electrical characterization confirms EOT – gate leakage currents to be comparable to HfO_2 (Fig. 2). Thermal stability of the layer was tested by annealing a $DyScO_x$ capacitor at a temperature of 1000°C for 10s. As observed by TEM, the layer is still amorphous after anneal (see Fig.3). Distinct interfacial layer growth was observed and remains to be studied in more detail.

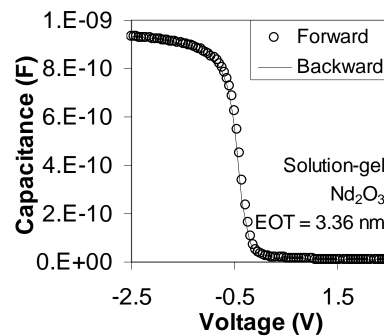

Fig.1 CV-curves (forward and backward trace) of a 12-nm thick Nd_2O_3 layer deposited by the aqueous solution-gel method on ~2nm SiO_2.

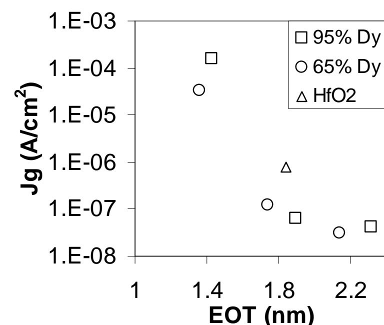

Fig.2 EOT – gate leakage for $DyScO_x$ layers deposited by MOCVD on 1 nm SiO_2. EOT – Jg is shown to be comparable to HfO_2.

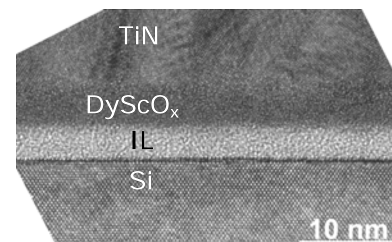

Fig.3 Cross-section TEM of a $DyScO_x$ layer after a 10s, 1000°C anneal. No crystallization of the layer is observed.

References

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[3] S. Van Elshocht et al., J. Electrochem. Soc., in press.

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