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Here I want to thank my family and friends who have been supporting me from a distance. My grandfather often expressed it this way:

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Rainer Petersen,

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to my mother †11.8.88

Nederlandstalige samenvatting

Motivatie voor het doctoraatswerk

Dit doctoraatswerk kan gesitueerd worden in het kader van het betrouwbaarheidsonderzoek van actieve elektronische componenten. Met de verhoogde complexiteit van elektronische schakelingen worden de eisen voor de betrouwbaarheid van de enkelvoudige component steeds strenger. Door de miniaturisering van de elektronica neemt de dichtheid van componenten steeds toe. De introductie van nieuwe technologieën kan leiden tot nieuwe, ongekende falingsmechanismen. Het betrouwbaarheidsgedrag moet op voorrand gekend zijn om een bepaalde levensduur van de elektronische componenten te kunnen garanderen. De betrouwbaarheid kan met hulp van verouderingsexperimenten bestudeerd worden. Tijdens deze testen worden de componenten onder invloed van verhoogde elektrische en thermische belasting versneld verouderd. Men hoopt zo de natuurlijke veroudering op een tijdsschaal van bijvoorbeeld 25 jaar binnen een economisch verantwoorde tijd op te wekken. Enerzijds moet de belasting hoog genoeg zijn om de veroudering voldoende te stimuleren maar anderzijds mag ze niet te hoog zijn om te vermijden dat kunstmatige verschijnselen geintroduceerd worden die onder gewone bedrijfsomstandigheden nooit zouden opgetreden zijn. bovendien is er voor versnelde verouderingsmetingen ook een minimum aan tijd vereist, om een verandering van de elektrische parameters te kunnen detecteren. Traditionele testen nemen dan ook vaak meer dan 2000 uren in beslag. Door de snelle vooruitgang in de microelectronica en de ingekortte productcycli is er vaak niet meer voldoende tijd ter beschikking staat voor traditionele verouderingstesten. Er bestaat dus een grote belangstelling vanuit de nijverheid aan methodes om de betrouwbaarheid van elektronica in zo kort mogelijke tijd op te meten.

De in-situ meettechniek

Een mogelijkheid om de benodigde tijd voor detectie te kunnen verkleinen is de verlaging van de detectiedrempel. Als criterium voor veroudering wordt meestal een degradatie van 10 of 20 percent van de oorspronkelijke waarde van de te meten parameter beschouwd. De benodigde meetnauwkeurigheid om deze degradatie op te sporen is van dezelfde grootteorde. Indien nu de meetnauwkeurigheid opgevoerd wordt, kan onder bepaalde omstandigheden de detectiedrempel verlaagd worden en zo de minimumtijd voor verouderingstesten behoorlijk ingekort worden. De verhoging van de meetnauwkeurigheid op zich is

nog niet voldoende, ook de stresscondities zoals spanning, stroom en temperatuur moeten op en bijzonder goed gedefiniërd worden. Dit kan op meettechnisch vlak bereikt worden door de toepassing van de door het Insituut voor Materiaalonderzoek (IMO) in samenwerking met het Interuniversitair Centrum voor Microelektronica (IMEC) ontwikkelde in-situ meettechniek. Met hulp van de nauwkeurige controle van de verouderingsparameters zoals stroom en temperatuur en het simultaan opmeten van de stressparameters kan de meetprecisie behoorlijk worden opgedreven. Bijkomend kunnen dataverwerkingsalgorithmen toegepast worden om de kwaliteit van de gegevens verder te verhogen. Om het verouderingsgedrag in normale werkingscondities te kunnen voorspellen worden fysisch gefundeerde modellen ontwikkeld en toegepast. Dit moet zorgvuldig gebeuren omdat het gemeten verouderingsgedrag vaak complex is. De in-ditu methode is bijzonder geschikt voor het bestuderen van de initiele fases van het verouderingsproces. De opbouw van reële elektronische systemen is inderdaad zo ingewikkeld, dat meestal meerdere verouderingsmechanismen simultaan optreden. Als men bijvoorbeel de veroudering van een hele versterker zou willen testen, verkrijgt men een samengesteld effect van de degradatie van misschien 30 tot 50 enkelvoudige componenten. De interpretatie van de betrouwbaarheidsgegevens wordt zo uiteraard bemoeilijk of zelfs onmogelijk. Voor het uitvoeren van bestudeerbare betrouwbaarheidstesten is het daarom van groot belang om de voorkeur te geven aan zo eenvoudig mogelijke teststructuren. Een specifiek probleem in verband met het opmeten van de karakteristieken van actieve elektronische componenten is zelfopwarming of Joule-opwarming. Bij het opmeten van weerstandskarakteristieken onder stroombelasting kan zelfopwarming van de component reeds optreden als gevolg van de toegepaste meetstroom. Deze zelfopwarming is een functie van het gedissipeerde vermogen. Door de intrinsieke temperatuursgevoeligheid van de elektrische karakteristieken wordt de meting van de parameters door de zelfopwarming beinvloed. De temperatuur zelf is een bepalende factor voor het verouderingsgedrag en moet zowel voor de planning van een verouderingsexperiment alsook voor de interpretatie van de gegevens bekend zijn. Een reeks diffusiegerelateerde verouderingsverschijnselen worden in dit werk gemodelleerd met hulp van Arrhenius-modellen. Er werd ook een techniek ontwikkeld om de thermische weerstand van de geteste componenten op te meten en zo de kanaal- of junctietemperatuur in functie van het vermogen te kunnen bepalen.

Indeling van dit proefschrift

Dit doctoraatswerk is in vijf hoofdstukken ingedeeld en volgt de tijdslijn van de ontwikkeling en uitbreiding van het meetsysteem voor actieve elektronische componenten.

- Het eerste hoofstuk begint met een beknopte omschrijving van de traditionele benadering voor betrouwbaarheidsmetingen en de algemene overwegingen die tot het ontwerp van de in-situ meetopstelling voor actieve elektronische componenten geleid hebben.

- In hoofdstuk twee wordt het meetprincipe gevalideerd met behulp van metingen op geselekteerde gallium arsenide componenten. In dit stadium van ontwikkeling werden aanpassingen aangebracht aan het in-situ meetsysteem dat voor passieve weerstandsmetingen gebruikt werd. Nadien de haalbaarheid van het concept aangetoont was, werd het concept uitgebreid om een scheiding tussen meet- en stresscondities toe te laten om de nadelige effecten van zelfopwarming op de behaaldde meetprecisoe tegen te gaan. Met de verbeterde in-situ technologie werden resultaten behaald die in goede overeenstemming zijn met gegevens afkomstig van traditionele testen. Met hulp van de nieuwe meetmethode was het namelijk mogelijk, de in een tijdsstip van 60 uren opgetreden veroudering tijdens een in-situ experiment te extrapoleren naar 5000 uren conventionele testtijd.

- Op dat moment vond een andere noodzakelijke uitbreiding van het meetsysteem plaats, namelijk de overgang naar een volledig softwaregestuurd meetsysteem met digitaal gecontroleerde voedingen. Daardoor werd het mogelijk om de meetsequentie aan te passen zonder enige fysische manipulatie aan het meetsysteem uit te voeren. Met dit verbeterd meetsysteem werden metingen op pHEMTs uitgevoerd (hoofdstuk 3). In dit geval werden we op een exemplarische manier met het probleem van interpretatie van complexe verouderingscurves geconfronteerd. De pHEMT technologie vertoont en complexer verouderingsgedrag dan de voorheen bestudeerde MESFET technologie. Er treden hier namelijk twee concurrerende verouderingseffecten op met verschillende activatie-energieën en met verschillende sterkte. De oorzaak voor het afwijkend gedrag van een groep pHEMT's konde met hulp van fysische analyse achterhaald worden. De metingen op pHEMTs vonden

in een meetsysteem plaats waarbij één preparaat per experiment opgemeten kon worden.

- In het laatste hoofdstuk worden metingen op een uitgebreid meetsysteem gepresenteerd waarvan de meetcapaciteit opgevoerd werd naar maximaal 20 componenten. Het simultaan opmeten van merdere componenten in één experimant levert een behoorlijke tijdswinst op en verhoogd de statistieke significantie van de meetresultaten. Deze metingen vonden op heterojunctie bipolaire transistoren (HBTs) plaats. Er werden twee verschillende technologieën HBT's opgemeten, met name aluminium gallium arsenide (AlGaAs) en indium gallium phosphide (InGaP) HBTs. De veroudering van deze componenten is afhankelijk van de stroomdichtheid en de junctietemperatuur. Stroom- en temperatuursafhankelijkheid werden apart bepaald om een levensduurvoorspelling mogelijk te maken. Met de overgang van AlGaAs naar InGaP HBT technologie werd de betrouwbaarheid behoorlijk verbeterd.

Op het einde van dit laatste hoofdstuk stelt zich de vraag, in welke mate de levensduur nog "meetbaar" is zonder terug naar onrealistisch hoge meettijden te gaan. Indien de stress op te componenten op een verantwordde manier verhoogd werd, kan de meettijd in bepaalde gevallen terug verkort worden. Hierbij moet inderdaad op gelet worden, dat geen falingsmechanismen opgewekt worden, die onder normale bedrijfsomstandigheden nooit geactiveerd zouden zijn.

Nieuwe mogelijkheden van de in-situ techniek en onderscheiding t.o.v. traditionele testmethodes

Met de voorgestelde techniek kan de veroudering van actieve elektronische componenten onder stroom en temperatuursstress worden opgemeten. Het meetprocess zelf is volledig geautomatiseerd via software en de gegenereerde gegevens kunnen op ieder tijdsstip verwerkt en geanalyseerd worden. Met behulp van het stuurprogramma kan het verouderingsprofiel op een flexibele manier aangepast worden. Door de modulaire opbouw van het ontwikkeld meetsysteem kan de configuratie van spannings- en stroombronnen gemakkelijk gewijzigd worden. Er zijn in de loop van de ontwikkeling van het meetsysteem bepaalde keuzes gemaakt worden die in de geschikte hoofdstukken nader uitgelegd worden. Zo werd er vroeg geopteerd voor een DC-meet opstelling. De redenen hiervoor worden in hoofdstuk 2 verder uiteengezet. Het opmeten van hoogfrequente parameters in het microgolfregime is

met de in-situ opstelling niet haalbaar zoals in hoofdstuk 2 wordt uitgelegd, maar door complementaire ex-situ karakterisaties vóór en ná het verouderingsexperiment uit te voeren kan het beeld wel aangevuld worden. De meting onder DC-condities zetten de component onder temperatuursbelasting door zelfopwarming. Een methode, om de zelfopwarming tegen te gaan bestaat in het gebruik van extreem korte meetpulsen. De opgemeten MESFET-, HEMT- en HBT-componenten zijn echter van afblokcondensatoren voorzien om oscillaties te voorkomen. De toepassing van korte pulsen was dus om redenen van componentdesign niet mogelijk. Toch biedt deze methode een interessante mogelijkheid, om de problemen rond zelfopwarming tijdens een karakterisatiemeting tegen te gaan. De thermische weerstandsmetingen voor de bepaling van de zelfopwarming zijn niet altijd uitvoerbaar met de ontwikkelde in-situ meetopstelling. Het opmeten van de thermische weerstand van de heterojunctie bipolaire transistoren in hoofdstuk 5 vormt hierbij een uitzondering omdat de metingen in DC-regime konden gebeuren. Ondanks het feit dat de voorgestelde metingen op gallium arsenide componenten uitgevoerd werden, is de ontwikkelde meettechnologie ook op andere materiaalsystemen toepasbaar zoals bijvoorbeeld silicium en indium phosphide.

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Chapter 1: Introduction

1.1 Reliability and complexity

In the 1920s, the broadcast receiver was the first electronic device for the mass market. In those early days of electronics, electronic valves were the only available technology for signal amplifiers. As tubes were expensive, the first receiver designs were kept deliberately simple to avoid cost. Even as late as 1950, standard broadcast receivers counted no more than five electron tubes. Tube failure due to tube filament wear-out was common, but due to the simplicity of design, repair was easily accomplished which has already been stated by Feynman [1]. The low component reliability had thus little impact on the usability of the design. The situation changed completely in 1944 when the first electronic computer, the ENIAC, was designed which was the most complex electronic project realised until then.

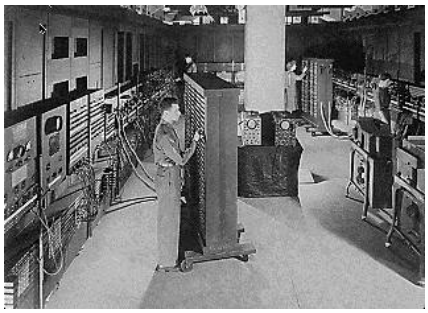

Figure 1.1: ENIAC computer operating room

The ENIAC employed 17.468 vacuum tubes and 1500 relays connected by more than 500.000 solder joints and occupied a surface of 72 m^2 (see figure 1.1). The circuit design could not be simplified without losing the most basic functionality. Based on electronic tube technology, the low component reliability posed a major challenge. At the beginning, it was seriously doubted that it could ever be brought to work for any useful time without failure. In order to obtain a maximum operating time between repair and maintenance intervals, several principles were followed which were already known in the 1940s.

Electronic device failure predominantly occurs at the beginning of component life (early failure). At the time of the ENIAC it was already known that after a period of high *"infant mortality"* a phase follows where devices fail with a constant but

low failure rate until they reach the period of fatigue wear-out at the end (e.g. filament wear out) of the component life. This is the famous *"bathtub curve"* which was empirically deduced from available statistical failure data [2] of mechanical and electric devices. The period of infant mortality could be avoided by screening components for use in high-reliability applications. Consequently, for the construction of the ENIAC only tubes were employed which had already run for a certain period without failure and were still "fresh" enough to provide sufficient useful life time. This procedure is now commonly known as *burn-in* [3].

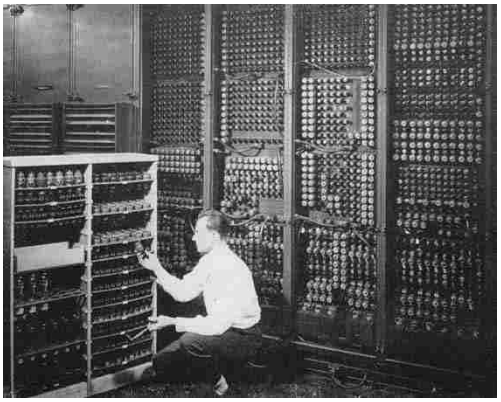

Figure 1.2: ENIAC maintenance and tube replacement

To extend device life, the tubes were operated at only a quarter of their nominal anode voltage reducing current and temperature stress. This principle is now known as *derating*.

As a consequence of countless incremental improvements, the average uptime of the ENIAC increased from a few hours per week in 1944 to finally more than 100 hours when the computer went out of service in 1955 reducing the need for maintenance (see figure 1.2). In the meantime the electronic valve was superseded by the transistor eliminating filament wear as failure source. With the introduction of the IC (integrated circuit) the number of external solder joints was substantially reduced. As these ICs combine the functions of thousands or even millions of transistors, the reliability of each single transistor in the IC must be by several orders magnitudes higher than formerly for discrete devices as replacement is impossible.

To put it short, the world of today would look totally different without the substantial progress towards higher device reliability.

1.2 Reliability and quality

In the preceding section we have employed the term *reliability* quite loosely. From a layman's perception and feeling, reliability is often associated with *quality* . Both terms have strict formal definitions documented in the ISO 9000 standard [4].
Quality is there defined as:

"the totality of features and characteristics of a product or service that bear on its ability to satisfy stated or implied needs".

This definition does not contain an explicit notion of endurance or time. An explicit notion of time is firstly introduced with the term reliability.
The reliability of a product is defined as:

"the probability that a product will perform its intended function for a specified period of time under stated conditions".

In order to work with the aforementioned definitions, we have to define the nominal function of the device and derive a suitable failure criterion. In the physical context, "ageing" describes the time dependent irreversible change of a measurable property of a system. For electronic components, a failure criterion can conveniently be defined by a significant change of an electrical parameter like resistance or capacitance for a passive device or amplification factor for a transistor. Device failure may occur either gradually or catastrophically. Catastrophic failure can not be predicted based on observations of some kind of degradation characteristics as it occurs without announcement. Catastrophic failure behaviour can only be approached by a purely statistical method such as probability. For gradually developing device failure, the degradation characteristics can be described as a continuous, time dependent function. This function is determined by the structure of the device, the stress factors and the nature of the underlying fundamental physical and chemical ageing processes. A comparison between the time-to-failure and the degradation characteristics based approach is given by Lu et.al. [5].
Reliability assessment of electronic devices is performed by life-testing. The device under test is put into operation and its performance monitored over a certain period of time. Under standard operating conditions of electronic devices, the time to

observe a significant parameter degradation is very long and in the range of several years. This renders reliability testing in real time rather impractical. An increase of the stress condition leads to an acceleration of the device ageing which can be used to shorten the necessary test time. The results gained from accelerated testing are interpreted with help of appropriate models which describe the stress dependency of degradation acceleration. Stress parameters are the external factors such as voltage, current, temperature and time. Variation of the stress factors lead to an acceleration or deceleration of the component ageing dependent on the fundamental degradation mechanisms. The achieved acceleration depends on the kind of stress, the kind of device and the active failure mechanisms. Accelerated life testing is nowadays an established tool for reliability assessment in industry. The exact procedures applied in industry are often regarded as company secret so available official documentation is sparse. Reliability prediction is often carried out in accordance to the MIL-standards such as MIL-217 [6]. In the past, some criticism has been raised that the MIL-standards are inappropriate to consumer electronics design [7], MIL-standards are still widely used as a basis for reliability evaluation as there has been no common agreement on any alternative yet. In the last years, several companies or government institutions have developed own realibility evaluation procedures as an extension or derivation based on the original MIL-standard. As standard life tests as established in industry usually take several thousand hours for completion, strong economic pressure is felt to develop test methods which deliver comparable results in shorter time as innovation speed is increasing. For the acceleration of the device degradation, the applied stress levels can not be infinitely increased without introducing artifacts. A possible solution is the application of lower degradation criteria. In order to detect such low degradation levels, the resolution and accuracy of the measurement equipment must at least be one order better than the defined degradation criterion. The development of such an accelerated high resolution test method for active electronic components under thermal and electrical stress is the subject of this thesis.

1.3 The kinetic approach to ageing

Already from the experiments of Edison it was known that the filament lifetime of incandescent lamps depends on the filament temperature. As the temperature increases, more and more atoms are evaporating out of the filament, thinning the filament wire and finally leading to failure. As the filament gets thinner, its resistance increases which slows down the ageing. The degradation of the filament can be slowed down by applying a lower filament voltage at the expense of efficiency. For life test purposes, the ageing can be accelerated in a controlled way by increasing the voltage. For this kind of device, temperature and voltages are potential candidates to be used as stress factors. Employing appropriate lifetime models, the lifetimes at low stress levels can be calculated based on the results based on higher stress levels. Some commonly used lifetime models will be introduced in this section.

1.3.1 The Fick diffusion laws

The wear of a filament wire is governed by the evaporation of wire atoms into the gaseous environment which means a phase change of the wire material. Many ageing processes are governed by the thermally activated physical diffusion of materials. For time-independent concentrations, the diffusion process is described by Fick's first law [8] which has been established in 1855:

$$J_m = -D(T)\frac{\partial C}{\partial x} \tag{1.1}$$

with:

J_m	:	material flux
C	:	concentration
D	:	diffusion coefficient
T	:	absolute temperature (K)

Fick's second law describe the diffusion in case of a time-dependent concentration gradient:

$$\frac{\partial C}{\partial t} = -D\frac{\partial^2 C}{\partial x^2} \tag{1.2}$$

Diffusion provokes changes of the physical composition of the electronic component. Diffusion itself is a purely physical process. It can be accompanied by chemical reactions of phase changes. As the material layers of modern devices are very thin, even microscopic changes of the device composition have significant effects on the device performance. For the initial phases of a diffusion process, the concentration gradient may often be assumed to remain stable. Later in chapter 2 we will make use of Fick's first law regarding the thermally-governed degradation of metal semiconductor field effect transistors (MESFETs).

1.3.2 The Arrhenius relation

In 1889 the Swedish scientist Arrhenius formulated a theory concerning the rate of reaction for diffusion controlled chemical processes in aqueous solutions [9]:

$$D = A \ \exp\left(\frac{E_a}{k_B T}\right) \tag{1.3}$$

with:

E_a	:	activation energy
k_B	:	Boltzmann's constant
D	:	reaction rate
A	:	pre-exponential temperature independent coefficient
T	:	absolute temperature

The acceleration of a diffusion process with temperature can then be expressed as:

$$A_F = \frac{D_2}{D_1} = \exp\left(\frac{E_a}{k_B}\left(\frac{1}{T_2} - \frac{1}{T_1}\right)\right) \tag{1.4}$$

with:

A_F	:	acceleration factor
T_1	:	lower temperature
T_2	:	higher temperature
D_1	:	reaction rate at lower temperature
D_2	:	reaction rate at higher temperature

The activation energy E_a can be interpreted as a threshold energy which must be attained before a chemical reaction occurs. In a gas or fluid or at the interface of solids the energies of the reactants are not equal but distributed around a mean value. Some atoms will have an energy beyond the threshold energy and react. Some chemical reaction will occur below the activation energy but at a much reduced velocity. As the reaction in aqueous solutions is governed by diffusion soon the Arrhenius-formula was applied to a broad range of other primarily diffusion-controlled processes.
For the diffusion of dopants into silicon the activation energy is in the range between $3 \ldots 3.5$ eV for commonly used materials [10] so that at room temperature (where the thermal energy corresponds to ≈ 0.026eV) the diffusion is slowed down by several orders of magnitude but not stopped completely. In gallium arsenide, the corresponding activation energies are lower (in the range between $1.4 \ldots 1.6$ eV) and diffusion-related processes play an important role in the ageing of gallium arsenide based electronic components.

1.3.3 The Einstein diffusion equation

Despite the widespread use of Arrhenius-based degradation models it must be mentioned that device degradation may also be governed by other factors than time and temperature and those mechanisms may occur simultaneously with Arrhenius-type degradation. One important mechanism is the diffusion of charged particles like electrons or ions in an electrostatic field as described by the Einstein equation [11]:

$$J(x) = Z^* \; C(x) \; m \; E(x) + \frac{k_B}{q} T \; m \; \frac{\partial C(x)}{\partial x} \tag{1.5}$$

with:

x	:	distance
J(x)	:	particle flux
E(x)	:	electrostatic field
Z^*	:	effective particle charge
q	:	elementary electron charge
m	:	particle mass
C(x)	:	concentration of particles at location x

1.3.4 The Black equation for electromigration

Mass transport in a solid structure can also be caused by electrical current. An important example of current induced degradation is the process of electromigration. Here the mechanical impulse transferred by the "electron wind" delivers the energy to displace atoms out of the metal structure [12]. Electromigration can be observed in metallic conductors operating at current densities of several kA/cm^2. Such high current densities are common for interconnection metallisations in integrated circuits. Empirically, this process can be described by Black's equation [13]:

$$t_{50} = \frac{A}{j^n} \exp\left(\frac{E_a}{k_B T}\right) \tag{1.6}$$

with:

t_{50}	:	median time to failure
j	:	current density
n	:	current density exponent
A	:	constant

The Black equation is based on empirical grounds and its use is justified as it fits to a multitude of electromigration phenomena. The current exponent in equation 1.6 lies between 1 and 4 depending on the material and the stage of the electromigration process. It does not take into account the existence of different electromigration mechanisms as nucleation or growth related damage.

1.3.5 Limits of kinetics-based modeling

Under real life conditions, concurrent failure mechanisms are likely to occur which renders the analysis of field reliability data, if available, complex. For the setup of life test experiments it is preferred to examine just one degradation mechanism at a time to keep the number of experiments within reasonable limits and the numerical analysis feasible. For each failure mechanism, the application of the appropriate model is necessary. The general aspects and details of accelerated ageing experiments are explained in the book of Nelson [14]. For simple device structures and temperature-induced degradation an analytic approach can be formulated based on

the Arrhenius theory to derive the activation energy from the measured degradation characteristics. For complex device structures several different ageing processes may be present simultaneously which is the more general case. This implies a certain danger regarding the straightforward application of the Arrhenius-theory: In reliability analysis, often a constant activation energy is supposed as well as a constant pre-exponential factor for the degradation of real electronic devices. This is an over-simplification passing beyond the limits of the original Arrhenius theory. In the original paper of Arrhenius, the reaction behaviour for one single activated chemical process in a narrow temperature range is described. When multiple processes with different activation energies are present, the measurement of the activation energy (e.g. with help of an Overhauser-experiment [15]) leads to a non-constant activation energy if measured over a wider interval. Accelerated life testing is often performed at high test temperatures of more than 175 °C [16]. At these high temperatures, the device ageing is governed by processes with high activation energies due to the influence of the exponential term of equation 1.3. Under operating conditions however, the device degradation may be dominated by processes with low activation energies. Extrapolating of results gained from accelerated tests at high temperature to room temperature may lead to a systematic over-estimation of device lifetimes, a criticism which has been articulated by several authors as Jensen et al. [17].

1.4 The contribution of this work

1.4.1 The High Resolution Resistance Measurement Technology (HRRMT)

In this thesis, a novel approach is presented for accelerated ageing testing of active electronic components under thermal and electrical stress. The approach is based on the *in-situ* technique developed at the IMO (Instituut voor Materialonderzoek, Institute for Materials Research) in collaboration with the Interuniversitair MicroElektronica Centrum (Inter-university Micro Electronics Center, IMEC) in 1990. The *in-situ*-method is based on the accurate measurement and control of the device stress parameters as voltage, current and temperature during the stress phase and is subject of a European patent [18]. As the measured device parameter was primarily the electrical resistance of a material system or an electronic component, it became

known as High Resolution Resistance Measurement Technology (HRRMT). This method allowed the in-situ observation of time and stress dependent ageing of passive electronic components and material systems at elevated temperatures in-situ [19][20]. During conventional tests, the devices are tested off-line at room temperature between high-temperature stress intervals. As the room temperature is often poorly defined and the test temperature stability is usually also poor in conventional ageing test benches (± 0.5 °C), temperature induced uncertainty is imposed on the measured electrical parameters due to the temperature dependency of electronic parameters. For small temperature excursions around a set-point temperature, the temperature-induced noise is statistically distributed around a value which would be obtained without the presence of thermal noise. The first step to reduce temperature induced noise is the stabilisation of the ambient temperature within narrow limits. The effect of residual temperature scattering on the measurement of the electronic parameter can significantly be reduced by correlation techniques such as Cook's method [21]. Temperature and electronic property measurement are performed simultaneously to obtain an optimal correlation. The Local Temperature Sensing and Correction Algorithm (LTSCA) is the subject of a European patent [22].
The HRRMT has been applied by Manca [23] to composite materials and passive electronic devices such as capacitors and resistors. Another important application field has been the study of electromigration induced failure of interconnection lines as performed by D'Haeger [24]. The successful application of in-situ testing to passive structures has raised the question of a possible extension of the application range of the method towards active electronic components.

1.4.2 Selection of measurement mode and devices under test

The high current densities applied during electromigration experiments already lead to significant self-heating which also be present during life-testing of active devices under current stress. Although degradation mechanisms active devices exist where self-heating is negligible -one example being the hot-carrier degradation in MOSFETs which is *field* and not *current* driven- the case of current induced self heating is much more general for the operation of active devices. This thesis will therefore concentrate on life testing of active components under current stress.
As a practical application of the newly developed test system for active devices,

components based on gallium arsenide have been chosen. Gallium arsenide is the material of choice for high-frequency applications such as microwave power amplifiers. It is important to mention that the developed measurement technique can also well be applied to electronic components based on other materials.

1.4.3 Verification of test bench design and application to MESFETs

In chapter 2, accelerated life tests on MESFETs are described which are performed with a modified conventional in-situ measurement system. The first life tests were based on standard parameters used in industry as saturation current or pinch-off-voltage (applicable for JFETs, MESFETs). Soon it has been realised that the complex characteristics of active electronic devices can not properly be addressed with the measurement of one parameter at a time. The fundamental degradation mechanism for the MESFET are identified and the obtained degradation characteristics are fitted to an existing model. The measurement capabilities of the in-situ measurement system are extended to measure multiple electrical parameters simultaneously. An additional advantage of this method is the separation of stress and measurement conditions.
The ageing is defined by a stress condition prevailing for more than 95 % of the test time with intermittent additional measurement states for in-situ device characterisation. This test bench concept makes use of dedicated pre-adjusted hardware stress modules connected to the DUT by a software controlled multiplexer unit. For each change of the stress condition, different hardware modules must be disconnected and reconnected to the device under test (DUT). Although this task has been automatised, the measurement process has been complex to handle.

1.4.4 Extension to full software control and application to pHEMTs

In chapter 3, the extension of test bench to full software control will be described. The development of software-programmable stress modules and voltage sources reduces complexity and increases reliability of operation as the devices under test are permanently connected to the digitally controlled power supplies (DPSs). As a result, the number of included stress/measurement states can now freely be adapted

as needed. Life tests with this software-controlled system are performed on GaAs pHEMTs.

1.4.5 Extension of the measurement capabilities and application to HBTs

At this stage of development the test bench system is suited for the measurement of one device at a time (mono-sample-setup). In order to gain statistical confidence on results and to save valuable measurement time, a higher number of devices should be tested simultaneously. Therefore, it is a logic step to extend the mono-sample of the in-situ system to a system that allows the simultaneous testing of multiple devices (multi-sample setup). The problem of multiplexing reappears here as now the multi-meters have to be multiplexed in voltage and current measurement mode. After the transition to multi-sample capability, life tests on heterojunction bipolar transistors (HBTs) have been undertaken. The results of these tests are presented in chapter 4. The measurement of HBTs required further improvements of the test method and the setup.
During life test measurements of HBTs, device self heating is significant as the devices are designed for power applications. A technique has been developed to measure the HBT self-heating with high accuracy because necessary data about the thermal properties of the technology were not available. Further effort has been made for the modeling of the device degradation. As the current densities in the HBTs are very high, the degradation is partially temperature and partially current driven. In order to separate the influences of current and temperature as stress factors, and a degradation model has been developed and a range of measurements have been performed which are also presented in chapter 4.
As a conclusion it can be stated that each device technology has posed special challenges to the HRRMT system which have led to further adaptations and improvements of the test bench system. In all cases, the necessary time for obtaining meaningful life tests results has significantly been reduced compared to standard test procedures and links between the electronic parameter drift and the fundamental physico-chemical ageing processes have been established.

1.5 Conclusions for this chapter

In this chapter, a motivation has been given to understand why progress in electronics is so substantially linked to improving component reliability. The definition of the terms "quality" and "reliability" has been given as reliability forms a central subject of this thesis work. The basic concept of "ageing" has been explained in physical terms. The need for an objective physical "measure" of reliability and ageing has been motivated. Basis of the effort is the prior experience gained at IMO concerning the ageing of passive electronic components. Departing from this knowledge, a measurement method and system for the reliability evaluation of active electronic devices will be designed and realised. Based on this novel method, life tests on gallium arsenide active electronic components will be performed and the results will presented in the following chapters.

1.6 References for this chapter

[1] R. Feynman, *Surely you're joking Mr. Feynman!* (W.W Norton, New York, 1985).

[2] A. Bowker and G.J. Lieberman, *Engineering Statistics*, 2nd ed. (Prentice-Hall, Edgewood Cliffs, NJ, 1972).

[3] F. Jensen and N. E. Petersen, *Burn-In: An Engineering approach to the design an analysis of burn-in procedures* (Wiley, 1982).

[4] *ISO 9000* (ISO International Standards Committee / Technical Committee 176, 1983).

[5] C. J. Lu, W. Q. Meeker and L. A. Escobar, Statistica Sinica **6**, 531 (1996).

[6] D. o. D. Military, Military handbook 217 e; relibility prediction of electronic equipment, 1986.

[7] H. Blanks, Quality and Reliability Engineering International **4**, 227 (1988).

[8] A. E. Fick, Ann. Physik, Leipzig **170**, 59 (1855).

[9] S. Arrhenius, Zeitschrift für Physikalische Chemie Stochiometrie und Verwandtschaftslehre **4**, 226 (1889).

[10] C. Kittel, *Introduction to Solid State Physics*, 7th ed. (Wiley & Sons, New York, 1995).

[11] A. Einstein, *Eine neue Bestimmung der Moleküldimensionen*, PhD thesis, Universität Zürich, 1905.

[12] E. Arzt and W. D. Nix, J. Mater. Res. **6 (4)**, 731 (1991).

[13] J. Black, IEEE Transactions on Electron Devices **ED-16**, 338 (1969).

[14] W. Nelson, *Accelerated testing: statistical models, test plans and data analyses* (Wiley series in probability and mathematical statistics, New York, 1990).

[15] A. Overhauser, Phys. Rev. **90**, 393 (1953).

[16] H. Blanks, Microelectronics Reliability **20**, 297 (1979).

[17] F. Jensen, Quality and Reliability Enginering International **1**, 13 (1985).

[18] L. Stals, L. De Schepper, J. Roggen and W. De Ceuninck, European patent no. 0 395 149 B1 (1990).

[19] W. D. Ceuninck, *Study of structural relaxation of selected amorphous alloys with aid of electrical resistance measurements, original title Studie van structuurrelaxatie in enkele amorfe legeringen met behulp van elektrische weerstandsmetingen, Phd-thesis (Dutch language)*, PhD thesis, LUC, Diepenbeek,Belgium, 1990.

[20] L. D. Schepper, W. De Ceuninck, B. Van Hecke, E. Beyne, L. Stals and J. Roggen, ESTEC proceedings, 12-16 November (1990).

[21] B. C. Cook, Nucl. Instr. and Methods **24**, 256 (1963).

[22] W. D. Ceuninck, L. Stals, L. De Schepper and J. Roggen, European patent no. EP 0 733 909 A1 (1996).

[23] J. Manca, W. De Ceuninck, L. De Schepper, L. Stals, B. Van Hecke, E. Beyne, J. Roggen, M.F. Barker, C.R. Pickering, W.A. Craig and J.C. Gidrol, Proceedings 3rd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF), Schwäbisch-Gmünd (Germany), 5-8 October (1992).

[24] V. D'Haeger, *Study of electromigration of polycrystalline Al metal stripes with help of a high resolution resistance measurement technique (HRRMT), original title 'Studie van elektromigratie in polykristallijne Al-metaalbanen met behulp van een hoge resolutie weerstandsmeettechniek (Dutch language)'*, PhD thesis, LUC, Diepenbeek,Belgium, 1996.

Chapter 2: Development of a basic test bench and application to MESFETs

2.1 Introduction

In this chapter, a basic in-situ measurement system for active devices will be described. This test system will be designed to allow the monitoring of the degradation of different device parameters under thermal and electrical stress. The performance of the test bench will be verified with the help of accelerated life tests on gallium arsenide MESFETs (MEtal Semiconductor Field Effect Transistors). As a result, a measurement accuracy will be obtained which is of the same order as it has previously been established with the in-situ high resolution resistance measurement technique (HRRMT) applied to passive components.

2.2 Departure from the classical setup for passive components

In the classical HRRMT setup, the measured physical property is simply electrical resistance [1]. The resistance of a material system or electronic component can conveniently be measured using the four-point method as illustrated in figure 2.1. A constant current is passed through the device under test via one pair of leads. A separate pair of leads is employed to measure the voltage drop over the DUT without current load eliminating the voltage drop over the current leads. The four-point method has a high immunity against noise. The application of the four-point method is only applicable to two-terminal devices. Active components have at least three-terminals and so the situation described in figure 2.2 applies. The current through the DUT is determined by a controlling signal which can be a current

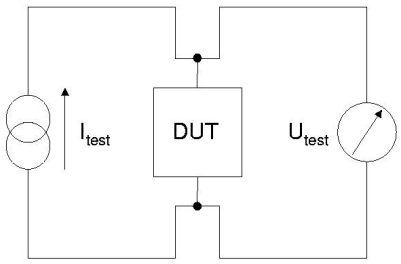

Figure 2.1: four-point method for two-terminal passive components

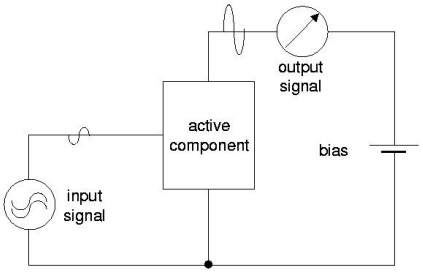

Figure 2.2: biasing of three-terminal active components

(bipolar transistors) or a voltage (field effect transistors). As the electrical power of the signal at the output is higher than the electrical power of the input signal, we get an amplification of the control signal. In figure 2.2 the situation is depicted where the output signal is a current, it can of course also be a voltage. Noise that is present on the controlling input signal is also amplified. This leads to a higher susceptibility to noise for measurements on active components compared to passive devices.

2.2.1 Sampling time and noise

The physical lower limit of the noise level in an electrical circuit is given by the amount of thermal noise (white noise) [2] which is generated by the thermal scattering of electrons in conductors.:

$$U_{noise} = \sqrt{4k_B TBR} \tag{2.1}$$

U_{noise} : noise voltage
k_B : Boltzmann's constant
T : absolute temperature
B : measurement bandwidth
R : resistance

The energy of white noise is distributed over the whole spectrum of frequencies. Following equation 2.1 his would lead to an infinite energy. it is clear that real

noise is never "white". It also follows that the measured energy depends on the frequency bandwidth of the measurement system. As the sampling time is increased, the stochastic part of the noise voltage is averaged out. The measurement accuracy in the presence of thermal noise increases with the square root of the sampling time. As stated at the beginning, this noise level forms the lower physical limit.

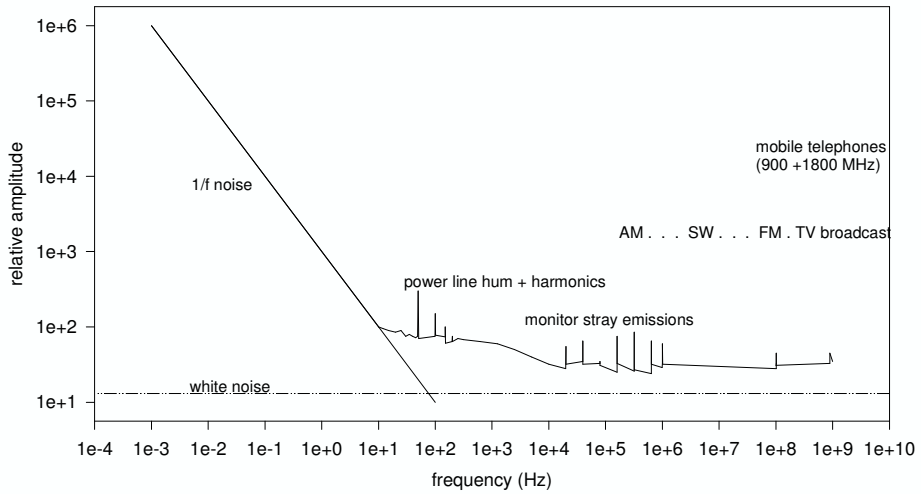

Figure 2.3: approximate external noise source spectrum

In a laboratory environment, there are many other noise sources than thermal noise as indicated in figure 2.3. Electromagnetic interference (EMI) from many external sources contributes to a much higher noise level. These noise emissions propagate through free air and along the power grid. Below 10 Hz, the spectrum is dominated by 1/f noise, a noise mechanism of which the physical nature is not yet completely understood [3]. The contribution of the 1/f noise appears highly exaggerated, as the noise amplitude is expressed in $V/\sqrt{Hz}$. Noise from luminescent lamps and switching power supplies is periodic and synchronous with the power line frequency. This noise can effectively be reduced by applying sampling times which are integer multiples of one power line cycle (1 PLC or 20 ms). For the measurements presented in this chapter, a sampling time of 1 PLC is applied.

Emissions from CRT (Cathode Ray Tube) monitors cover a spectrum from tens of kHz to several MHz. The clock frequency of personal computers is in the range from 100 to 2000 MHz providing a broad noise level. Those high frequencies are easier to block as their penetration is lower.
An other important concern is to provide well-defined grounding and signal return paths to avoid ground loops. For the interested reader, more details on these topics can be found in a book edited by Keithley Corp. [4].

2.2.2 Temperature regulation and temperature noise

The HRRMT is based on the accurate measurement and control of device parameters as voltage, current and temperature during the stress phase and measurement [1]. In conventional life tests, the device degradation is measured off-line at room temperature which is poorly defined. In the in-situ measurement system, the device degradation is measured at the stress temperature which is stabilised within narrow limits. Figure 2.4 gives a schematic overview of the temperature control of the measurement system. The furnace is heated by a resistive heater element and

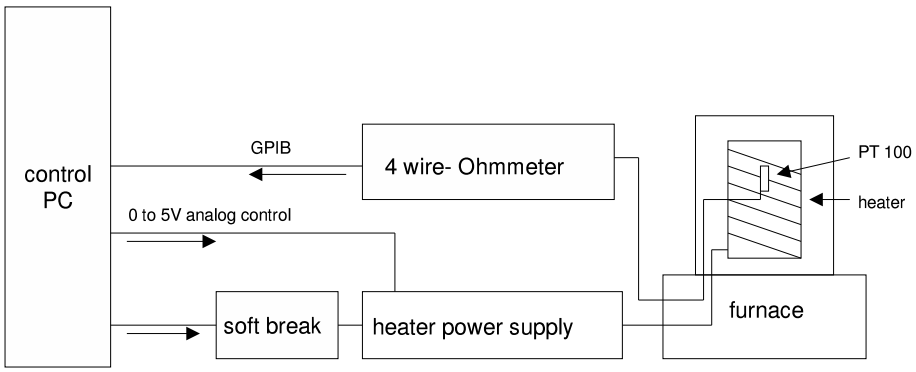

Figure 2.4: block diagram of the temperature control section of the test bench system

its temperature is stabilised using a PID-regulator. PID stands for Proportional-Integral-Differential and are the three parameters determining the response of the regulator to the measured property. These parameters must be adjusted to compensate the properties of the regulated system in order to obtain an optimal regulator

behaviour. Background information about the PID-algorithm and the adjustment of the parameters can be found in text books on electronics like Tietze-Schenk [5] where linear regulating algorithms are extensively treated. For temperature sensing, calibrated and highly stable PT-100 platinum resistors are used. The temperature coefficient for the specific PT 100 sensor type for the temperature range between -125 to 900 °C is given by the Callendar-Van Dusen equation [6]. The coefficients depend on the PT-100 type and the temperature range and can be found in the international standard IEC-751 [7]. Electrical noise is imposed by residual scattering of the ambient temperature due to the temperature dependency of the device parameters. For small excursions around a set-point temperature T_s we can write:

$$p(T) = p(T_s)\,(1 + \alpha(T - T_s)) \tag{2.2}$$

with:

p	:	property
T	:	actual temperature
T_s	:	setpoint temperature
α	:	temperature coefficient

In the HRRMT, temperature-induced noise is already reduced by stabilising the temperature at device level. It can further be minimised by the application of the Local Temperature Sensing and Correction Algorithm [8]. The temperature

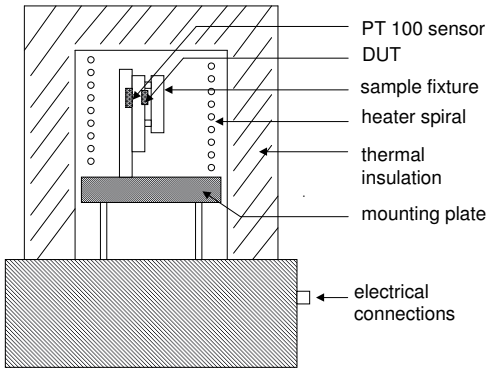

Figure 2.5: gas furnace with temperature sensor mounted closely to the DUT

sensing element is closely mounted to the active zone of the device under test to

provide a good correlation between temperature and measured electrical parameter as shown in figure 2.5. Temperature and property measurement are performed simultaneously. For the application of the correlation the temperature coefficient must not be known *a priori*, as it is a by-result of the correlation algorithm.

2.2.3 Temperature offset by Joule heating

During operation of active electronic components, a significant amount of electric power is converted into heat. As the ageing of the device is defined by the channel or junction temperature, the self-heating during the life test must be determined. The Joule heating problem can be illustrated with the help of an electrical analogy as the RC-model shown in figure 2.6. The contributions of the active zone (junction

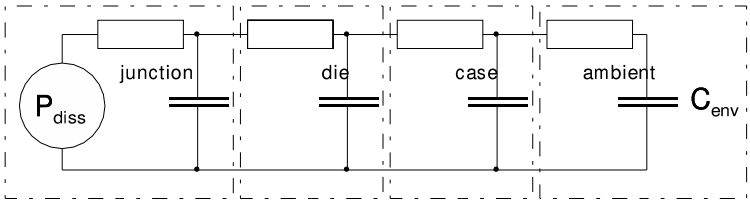

Figure 2.6: RC-chain thermal resistance model

or channel), die, case and ambient thermal resistances and capacities are treated as discrete elements with the heat flowing from the active zone (device junction or channel) to the environment. The active zone is very small compared to the device dimensions and significant device self-heating occurs during operation. For a FET, this zone is the current conducting channel, for a bipolar transistor the base-collector junction. For pulsed operation of active components the thermal impedance is determined by the charging and discharging of the thermal capacities. Under steady state conditions (thermal equilibrium) the thermal capacities can be neglected and we can write:

$$T_{jct} = T_{amb} + P_{diss}(R_{thjc} + R_{thja}) \tag{2.3}$$

with:

T_{jct} : channel or junction temperature

T_{amb} : ambient temperature

P_{diss} : dissipated power
R_{thjc} : thermal resistance from channel to case
R_{thca} : thermal resistance from case to ambient

The thermal resistance is treated as an ohmic (=constant) resistance. This is in fact a simplification as the thermal resistance of semiconductors is temperature dependent as shown in table 2.1. A more elaborate thermal resistance model including temperature dependent thermal resistances can be found in a paper of Veijola et al. [9]. Values for the thermal resistance are often provided by the component manufacturer, otherwise, the thermal resistance must be determined by measurement. In packaged devices, the channel or junction temperature can not be measured directly, but can be determined using the inherent temperature dependence of a suitable electric device parameter. A practical method to determine the thermal resistance of MESFETs has been developed as an auxiliary tool for the in-situ test system [10]. During life-testing a well-defined heat conduction path to the environment must be provided. The DUT can directly be immersed into an inert fluid as fluoridated hydrocarbons or silicon oil. The heat transport is enhanced by stirring the fluid providing a very low temperature gradient inside the furnace volume. Gas furnaces offer superior insulation characteristics and can be applied for low-power devices when a local temperature sensor is provided. A solution combining the advantages of fluid and gas furnace consists in mounting the DUT on a hermetically sealed heat sink. The back side of the heat sink is then immersed into a forced fluid bath. This method as described by Christiaens et al. [11] is especially suited for high-power devices.

2.3 Why gallium arsenide?

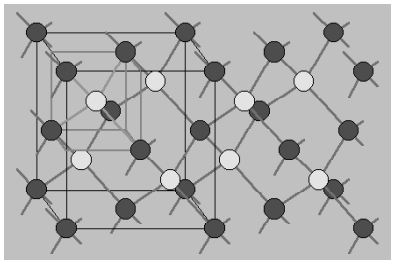

Figure 2.7: face cubic centered (fcc) layer structure of gallium arsenide

Gallium arsenide is a compound semiconductor made of alternating layers of gallium and arsenic with face cubic centered or zincblende structure. Gallium arsenide was first reported by Goldschmidt in 1929 [12] but the purity was low. The electronic properties of gallium arsenide were first reported in 1952 by Welker [13]. Table 2.1 gives an overview of the material properties of gallium arsenide and some other common semiconductors. Gallium arsenide has now some interesting properties for applications in electronics. The higher electron mobility of gallium arsenide compared to silicon translates to a more than three times higher maximum operating frequency of gallium arsenide devices compared to silicon devices with similar geometry. The higher bandgap compared to silicon and germanium means less intrinsic

property	**Ge**	**Si**	**GaAs**
electron mobility (cm^2/Vs)	3900	1500	8500
hole mobility (cm^2/Vs)	1900	450	400
thermal conductivity at 300 K ($W/m^2/K$)	59.9	148	55
thermal conductivity (300-900 K)(T)	$\sim T^{-1.35}$	$\sim T^{-1.49}$	$\sim T^{-1.23}$
electron mobility (T)	$\sim T^{-1.7}$	$\sim T^{-2.4}$	$\sim T^{-1}$
hole mobility (T)	$\sim T^{-2.3}$	$\sim T^{-2.2}$	$\sim T^{-2.1}$
intrinsic carrier concentration (1/Mole)	$2.4 * 10^{13}$	$1.45 * 10^{10}$	$1.79 * 10^{6}$
intrinsic resistivity (Ω)	47	$2.3 * 10^{5}$	$1 * 10^{8}$
energy gap (eV)	0.66	1.12	1.42
dielectric constant (ε_r)	16.0	11.9	13.1
lattice constant (Å)	5.64613	5.43095	5.6533
crystal structure	diamond	diamond	zincblende

Table 2.1: some selected material properties of germanium, silicon and gallium arsenide at room temperature [14]

conductivity of gallium arsenide which allows the operation of gallium arsenide at higher temperatures. Even at room temperature, there is a distinct advantage for gallium arsenide components concerning low noise characteristics. The suitability

of gallium arsenide for microwave applications and the rise in the telecommunications sector during the last years have stimulated the interest in gallium arsenide technology. Despite these advantages of gallium arsenide, there are also some drawbacks. At room temperature, the thermal conductivity of gallium arsenide is only one third compared to silicon. Therefore, GaAs devices will develop more internal heating than silicon components. The situation gets worse at high power dissipation as the thermal conductivity decreases further as device self-heating occurs and temperature increases. Under certain circumstances, the advantage of gallium arsenide of a higher tolerable operating temperature is compromised by internal device heating. For the use of gallium arsenide devices at high power dissipation, the thermal house-holding of the device is quite critical. The combination of electrical device degradation and thermal issues makes gallium arsenide devices an interesting object to study. Here in chapter 2, the reliability of low-power GaAs MESFETs which have been developed for use in space applications will be examined using the in-situ approach [15]. The test bench capability is then extended towards the measurement of multiple degradation parameters during one single experiment. The issues concerning the use of GaAs for power devices will be treated in more detail in chapter 4 concerning heterojunction bipolar transistors (HBTs).

2.4 MESFET operation and failure modes

In a MESFET (MEtal Semiconductor Field Effect Transistor), the current through the conducting channel is controlled by the external potential over the gate. This gate is formed by a metal/semiconductor interface forming a Schottky junction. Under this junction, a depletion zone is formed where no free current carriers are present. The effect of the depletion zone is equivalent to a built-in gate potential φ_b of -0.3 to -0.6 V. The MESFET gate can be positively biased by this value until a significant gate current flows. At zero external gate voltage (U_{GS} = 0 V), the depletion zone under the gate is shallow and the channel is conducting. The channel current at this bias point is known as drain-source saturation current I_{DSS}. When the external gate voltage becomes more negative, the depletion zone reaches further into the channel effectively decreasing its width. The channel current decreases until the channel is closed or "pinched-off". The gate voltage at this bias point is known as pinch-off voltage U_p or "threshold voltage"[1] as the device is at the threshold of conduction. Under standard conditions of operation, the drain/source voltage is positive, the gate/source voltage is negative as indicated in figure 2.8. With increasing drain/source voltage, the drain current first increases linearly as

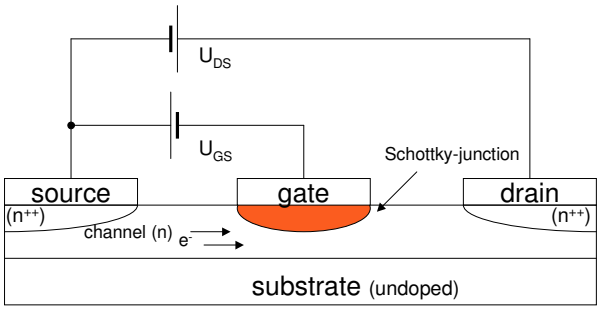

Figure 2.8: MESFET biasing scheme

the channel behaves like an ohmic resistor (linear or "triode" mode). When the magnitude drain/source voltages becomes higher than the pinch-off voltage, the

[1] "Threshold" voltage is commonly used for enhancement type devices (most MOSFETs), while "pinch-off" is used for depletion devices as JFETs and MESFETs.

drain current remains constant as the channel is saturated (saturation or "pentode" mode). The drain current characteristic in saturation mode is given by the following parabolic transfer function:

$$I_D(U_{GS}) = I_{DSS}\left(1 - \frac{U_{GS}}{U_p}\right)^2 \tag{2.4}$$

with:

I_D	:	drain current
I_{DSS}	:	drain-source saturation current
U_{GS}	:	gate-source voltage
U_p	:	pinch-off (threshold) voltage

The tested MESFETs have a gate length of 0.5 μm and are packaged in hermetically

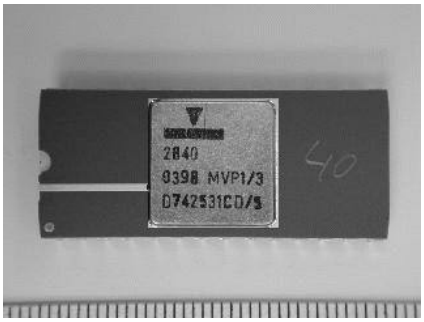

Figure 2.9: MESFET in ceramic DIL-28 package

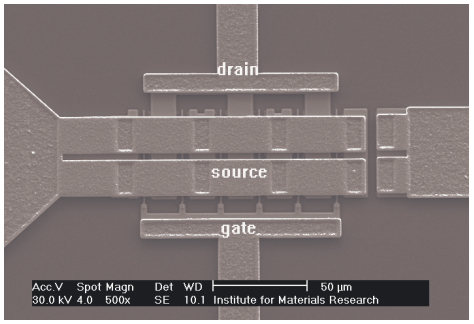

Figure 2.10: SEM top view of MESFET structure

sealed ceramic DIL-28 (DIL: Dual In Line) packages shown in figure 2.9.
Figure 2.10 shows a SEM top view of a device and figure 2.11 gives a schematic overview of the physical origin and location of the typical MESFET failure sites. Surveys of MESFET damage mechanisms have been made by Dumas [16] and Mizuishi [17] et al.. Major damage mechanisms of MESFETs are diffusion-driven. This diffusion may either be thermally or current-induced.
Thermal diffusion related damage may occur at any contact interface of the device. Contact degradation may lead to an increase of the ohmic access resistances of the drain, source or gate contact. Further, diffusion of gate material into the

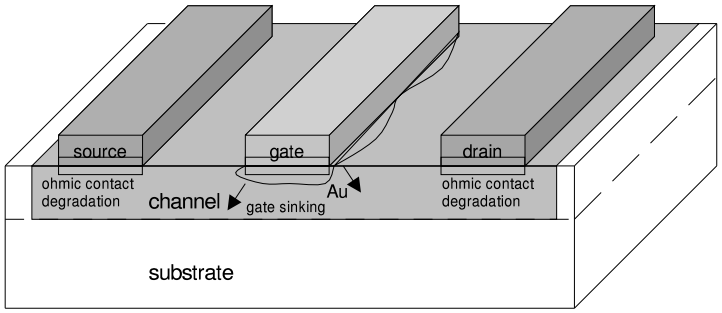

Figure 2.11: location of MESFET defect sites and failure modes

device channel may lead to degradation of the gate Schottky diode and is called gate sinking. This has been observed by Irvin et al. [18] for devices where Au/Al interfaces were present. Gate sinking has been a very serious problem for these early devices. The use of diffusion barriers made from stacks of refractory metals such as titanium-platinum-gold (TiPtAu) lead to much more stable devices. MESFET damage may also be inflicted by current induced diffusion known as ohmic contact electromigration. This failure mechanism is practically eliminated by the use of refractory metals for the ohmic contacts like gold-germanium-nickel (AuGeNi). The current densities necessary for contact electromigration of modern devices will not be reached under standard conditions of operation. Gate electromigration is a current-diffusion induced failure mechanism which may be present for power applications. In power applications, the gate may be positively biased during gate voltage peaks. As the gate/channel interface is small, current densities may be sufficient for electromigration damage. For the low-power MESFETs which will be tested, this degradation mechanism is rather unusual. We will thus concentrate on thermal-diffusion activated failure mechanisms and discuss how the electrical parameters are affected by the physical device damage.

2.4.1 The high-temperature operating test

A method for the detection of thermally driven ageing processes is the High Temperature Operating Life Test (HTOT). The device is electrically biased at its standard operating point in the designed application and put at elevated temperature stress. The High Temperature Operating Life Testis documented in a standard [19] issued by the JEDEC (Joint Electron Device Engineering Council). The time scale for HTOTs on MESFETs is typically between 4000 end 5000 hours. The diffusion affects the gate as well as the source and drain ohmic contacts.

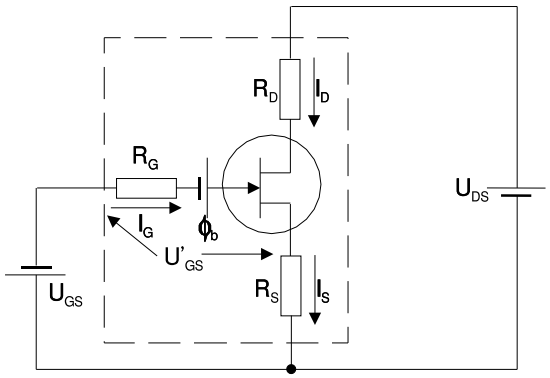

Figure 2.12: parasitic resistances of a MESFET

Figure 2.12 shows an equivalent electrical model of the MESFET to illustrate the correlation between physical changes and change of measured electrical properties. Inside this model resides an "ideal transistor". The gate, drain and source resistances and the gate potential φ_b of the real device are visualised as discrete, extrinsic elements. For the electrical parameters we choose the saturation current I_{DSS} (=open channel) and the pinch-off voltage V_p (=nearly closed channel).

We discuss now which kind of parameter drift can be detected by the selected stress conditions.

gate access resistance

As the gate is reversely biased, the gate current is very small and can normally be neglected. As there is practically no voltage drop over the gate access resistance, we have no detectable change of the gate potential and no influence on neither I_{DSS} nor V_p. Drift of the gate access resistance on the gate current can therefore not be detected with the HTOT.

gate potential (gate sinking)

The effective gate potential is defined by the external gate voltage U_{DS} Schottky junction potential. When gate sinking occurs, the gate is physically moving closer to the device channel. The effective gate potential is therefore becoming more negative. This gate potential shift affects the whole device transfer characteristics as given in equation 2.4. The pinch-off-voltage degrades according to the degradation of the gate potential. We will give now a simple model for gate sinking and an estimation of the diffusion depth of gate material under life test conditions will be given. Further, we will deduce the characteristics of the associated electrical parameter changes. The diffusion of gate material is governed by Fick's first law [20]:

$$J(x) = -D(T)\frac{\partial C}{\partial x} \tag{2.5}$$

with:

J(x)	:	atomic flux at location x
C:	:	concentration of diffusing matter
∂C/∂x	:	concentration gradient
D (T)	:	temperature dependent diffusion coefficient of the gate metal

The time dependence of the concentration gradient is given by Fick's second law:

$$\frac{\partial C(x,t)}{\partial t} = D\frac{\partial^2 C(x,t)}{\partial x^2} \tag{2.6}$$

with:

C(x,t)	:	concentration at location x and time t

We suppose now that the supply of atoms from the surface is inexhaustible and that the atoms are diffusing into an infinite half-plane leading to a spherical diffusion front. Further we neglect the layered structure of the gate. These simplifications are justified for the case that the total damage to the gate structure remains small. The concentration of diffused material related to the surface concentration C_s for one-dimensional diffusion of the Schottky contact into the gate is given by:

$$C(x,t) = C_s \ \mathrm{erfc}\left(\frac{x}{2\sqrt{Dt}}\right) \tag{2.7}$$

with:
erfc() : error function

Equation 2.7 is valid under the assumption of a constant surface concentration. The diffusion coefficient D is dependent from temperature (Arrhenius-process) assuming the form [21]:

$$D(T) = D_0 \ \exp\left(\frac{-E_a}{k_B T}\right) \tag{2.8}$$

By defining the metal front diffusion at depth $X_d(t)$:

$$c(X_d,t) = N \tag{2.9}$$

with:
N : concentration of in-diffused metal atoms

we get:

$$\frac{N}{C_s} = \mathrm{erfc}\left(\frac{X_d}{2\sqrt{Dt}}\right) \tag{2.10}$$

A degenerated condition can be assumed for $N/C_s > 10^{-4}$ as the concentration of in-diffused metal atoms reaches the concentration of donor atoms which typically between 10^{18} and 10^{19} per mole ($6.022*10^{23}$ atoms). The value for the error function argument for that value is:

$$\frac{X_d}{2\sqrt{Dt}} = 2.75 \tag{2.11}$$

Now we get an estimation for the sinking distance of the gate metal into the channel:

$$X_d(t,T) = 5.5\sqrt{D_0}\ \sqrt{t}\ \exp\left(\frac{-E_a}{2k_B T}\right) \tag{2.12}$$

At this point, we have calculated the diffusion depth of material into the channel. Now we have to find an estimation for the drift of the pinch-off gate. The thinning of the channel X_d causes a decrease of the built-in gate potential. This decrease is in first order proportional to the thinning and can be described by:

$$\Delta V_p \approx \frac{qN}{\varepsilon_0 \varepsilon_{GaAs}} X_d \; W \tag{2.13}$$

with:

ε_O : vacuum dielectric constant

ε_{GaAs} : GaAs dielectric constant

For the drift of the gate voltage we can then write:

$$\Delta U_p(t,T) \simeq 5.5 \left(\frac{qnW}{\varepsilon_0 \varepsilon_{GaAs}} \right) \sqrt{D_0} \; \sqrt{t} \; \exp\left(\frac{-E_a}{2k_B T} \right) \tag{2.14}$$

Within the scope of this model, the pinch-off voltage drift is proportional to the square root of time. From literature we get for the initial diffusion coefficient and the activation energy [22]: $D_0 = 5.5{*}10^{-8} m^2/s$ and an activation energy of $E_a = 1.7$ eV. The diffusion depth of Au into the gate channel can now be calculated using equation 2.12: After 4000 hours of accelerated life test at $T_{ch} = 205$ °C, the diffusion depth is about 52 Å, after 240 hours only 13 Å. As the lattice constant of GaAs is 5.65 Å, this corresponds to two atomic layers. The previously made assumptions of a low diffusion with constant diffusion gradient and infinite diffusion source are thus justified. Following Ladbrooke [23], the saturation current I_{DSS} of a MESFET can be described by:

$$I_{DSS}(t,T) \simeq q \; N \; v_{sat} W_G (W_A - X_d) \tag{2.15}$$

with:

q : elementary electron charge

v_{sat} : saturation velocity of electrons in GaAs

W_G : total gate width

W_A : active layer depth

X_d : depletion depth

The active layer corresponds to the effective channel width of the device. Following equation 2.12, the depth of the depletion zone under the Schottky junction depends on the gate sinking. The growing of the depletion zone X_d into the channel is equivalent to a decrease of the intrinsic gate potential φ_b. To obtain a constant drain current, the external gate voltage must compensate this potential decrease. The saturation current is proportional to the channel conductivity and therefore to the channel width ($W_A - X_d$). At t_0 the depletion width X_d is zero so the initial saturation current is:

$$I_{DSS}(t_0, T) = q\ N\ v_{sat} W_G\ W_A \tag{2.16}$$

and the saturation current change becomes then:

$$\Delta I_{DSS}(t, T) = I_{DSS}(t, T) - I_{DSS}(t_0, T) = q\ N\ v_{sat} W_G\ X_d \tag{2.17}$$

The saturation current and the pinch-off voltage decrease proportional to the increase of the depletion depth. As the depletion depth decreases with a square root of time behaviour, so does the saturation current. In case of gate sinking, saturation current and pinch-off voltage degrade with the same square-root of time characteristics.

drain access resistance

An increase of the drain access resistance leads to a decreased drain voltage. As the DUT is operating in saturation mode, there is almost no effect on the drain current. The influence of drain access resistance on either I_{DSS} nor V_p is very small.

source access resistance

The sensitivity against source access resistance increase is much higher: The source current which passes through the source access resistance leads to a decrease of the effective gate-source voltage U'_{GS} of the intrinsic transistor:

$$U'_{GS} = U_{GS} - I'_D R_S \tag{2.18}$$

with:

I'_D : reduced drain current
U'_{GS} : reduced gate/source voltage
R_S : source resistance

For a properly biased MESFET, we can suppose that the source current I_S is equal to the drain current I_D. Departing from equation 2.4, we have to use the effective gate voltage U'_{GS} as defined in equation 2.18:

$$I'_D(U_{GS}) = I_{DSS}\left(1 - \frac{U_{GS} - R_S I'_D}{U_p}\right)^2 \tag{2.19}$$

After some calculations, we get the following expression for the drain current:

$$I'_D = I_{DSS}\left(\left(1 - \frac{U_{GS}}{U_p}\right)^2 + \frac{R_S I'_D}{U_p}\left(2 + \frac{R_S I'_D - 2U_{GS}}{U_p}\right)\right) \tag{2.20}$$

The first term of equation 2.20 is the drain current transfer function of the device without source series resistance. The second is the correction for the source series resistance. The effective drain current decreases roughly proportional to the source current and source resistance. In case of ohmic contact degradation, the resistance may also increase with a square root of time characteristics but there is no correlation between pinch-off voltage and saturation current parameter: The saturation current is highly susceptible to source resistance R_S drift whereas he pinch-off voltage parameter measurement is not affected as the drain current is small. Table 2.2 summarises the dependence of the measured electrical parameters from the different thermally activated degradation mechanisms. The measurement of saturation current and pinch-off voltage allows the detection of the gate potential drift and the change of the source access resistance. Measurements of the degradation of these parameters will be presented in the following sections.

degradation	**dependence U_p**	**dependence I_{DSS}**
ohmic drain contact	low	low
ohmic source contact	low	high (arbitrary)
ohmic gate contact	no	no
gate sinking	high, $\sim \sqrt{t}$	high, $\sim \sqrt{t}$

Table 2.2: failure modes detectable by high temperature operating life test (HTOT)

2.5 Setup of the ageing experiment

The ambient temperature for the tests was 170, 190 °C and 205 °C. These temperatures have also been used for conventional tests from which data were available. It has been preferred to keep the test conditions of the in-situ tests as similar as possible in order to facilitate the comparison of results. The drain voltage is set to 5 V which is well within the electrical limits (7.5 V) of the device technology. With this setup of experiment, the ageing is thus mainly accelerated by temperature.

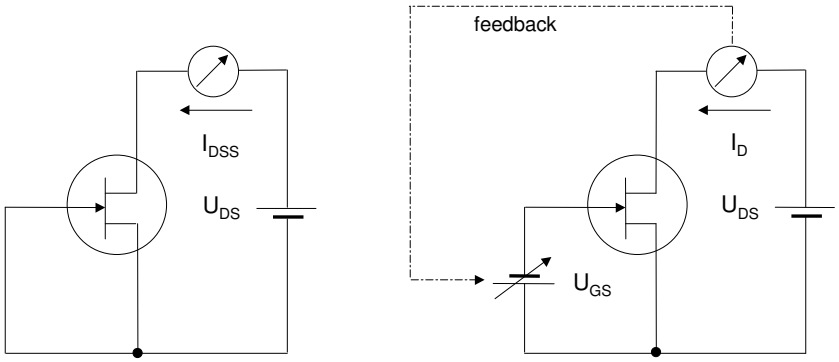

Figure 2.13: left side: two-point saturation current measurement configuration; right side: pinch-off voltage measurement with feedback on U_{GS};$U_{DS} = 5V$

2.5.1 Saturation current

The first parameter which will be measured is the MESFET saturation current. This measurement is simple to set up as it requires only one drain voltage supply and a drain current meter. The setup for the I_{DSS} measurement is shown on the left side of figure 2.13. As gate and source are connected together, the three-terminal MESFET is reduced to a two-terminal device. For this parameter, the measurement setup resembles closely the classical setup for passive components (figure 2.1).

2.5.2 Pinch-off voltage

The second parameter which is examined is the pinch-off voltage. The pinch-off voltage can not be measured directly at zero drain current because the drain current is also zero for *all* more negative voltages than the pinch-off voltage U_p. The pinch-off voltage will be measured at a small drain current which is stabilised (right side of figure 2.13) by a feedback loop on the gate voltage. The current loop method yields a pinch-off voltage with a small positive offset dependent on the drain current. The constant current loop is realised by a dedicated hardware module offering a base stability of a few parts per million (ppm) after warm-up. The setup of the pinch-off voltage measurement is similar to figure 2.2 and therefore more susceptible to noise than the saturation current measurement. Stochastic error currents ΔI_D on the drain current are picked up by the feedback loop and lead to noise on the regulated gate voltage.

$$\Delta U_{GS} = \frac{\Delta I_D}{g_m} \tag{2.21}$$

with:

g_m : transconductance of the device

The application of the constant current loop has the advantage that the dissipated power remains essentially constant as the gate current for a functional FET can be neglected. The device under test remains so at constant channel temperature. For the pinch-off voltage, the power dissipation and therefore the channel temperature offset is very small. However, at higher stress current levels, the device self-heating becomes significant.

2.6 Continuous single-parameter measurements on MESFETs

The measurements presented in the following two sections are performed in continuous mode for a single measurement state. It has to be remarked here that the measured parameter defines simultaneously the stress condition. As an important first result of these introductory measurements we will see that the obtained accuracy is of the same order than it has previously been obtained for passive test

structures. The ambient temperature is set to 170 and 190 °C as those temperatures were used for testing in industry. During these tests, the stress on the device was defined by the measurement parameter. In the frame of these measurements, we will discuss the shortcomings of this approach and propose improvements of the measurement system. Observations made on the degradation of a specific parameter were difficult to compare with results obtained from other stress parameters. During standard tests, the measurement of the parameter drift was performed intermittently. The device ageing was defined by a special stress condition which was applied for the most part of the measurement time. This leads to an extension of the test bench capability to the simultaneous measurement of multiple parameters allowing the separation of stress and measurement conditions which will be presented in section 2.7.

2.6.1 GaAs MESFET pinch-off voltage U_p

The pinch-off voltage is measured at a drain current of 300 μA and a drain voltage of 5 V (see figure 2.14). Under those conditions, the dissipated power (1.5 mW) is very small and the junction temperature is practically the same as the ambient temperature. After 60 hours, a parameter degradation of 0.9 % is observed. The data from a 60 hour accelerated ageing experiment as given in figure 2.14 are fitted to a square root of time function similar to equation 2.14:

$$\frac{U_p(t) - U_p(t_0)}{U_p(t_0)} = a\sqrt{t - t_0} \tag{2.22}$$

with:

t	:	time
t_0	:	time offset
$U_p(t_0)$	:	pinch-off voltage at time t_0
$U_p(t)$	:	pinch-off voltage at time t
a	:	fit parameter

In equation 2.22 an offset of -2.5 hours has to be applied to the measurement time t_0. This step is motivated by the thermal history of the devices. During the foundry process, the device is put several times at high temperatures for the annealing-out of crystal defects. This heat treatment and the warm-up time of the in-situ experiment

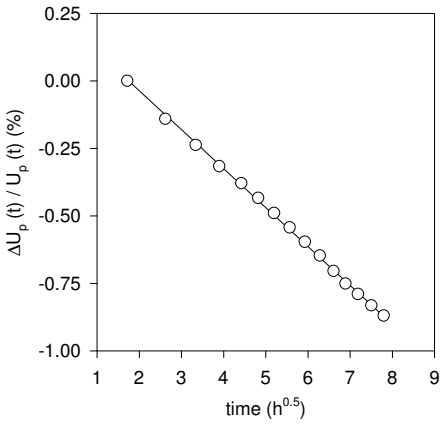

Figure 2.14: open symbols: 60 h in-situ life test data;
solid line: data fitted to equation 2.22

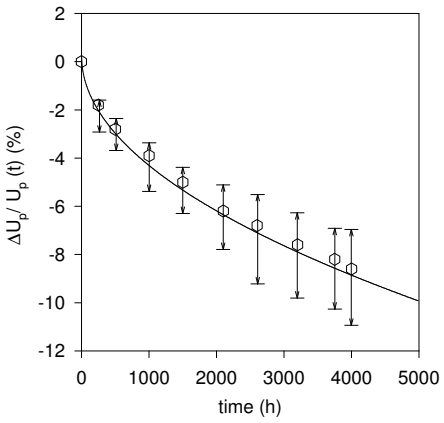

Figure 2.15: open symbols: conventional life test data from 15 devices;
solid line: extrapolation of fit from figure 2.14 to 5000 hours

are equivalent to several hours of thermal stress before life-testing. The degradation of the pinch-off voltage can be fitted to a square root of time scale which translates to a voltage decrease of -4.44 mV/$\sqrt{\text{h}}$ as shown in figure 2.14. The fit based on the 60 hours life test data is then extrapolated to 5000 hours of standard measurement time and can be seen on figure 2.15. The in-situ data fit (straight line) shows good agreement with the standard life test data which represent a mean value of 15 tested devices (open symbols). Due to parameter scattering, the drift of a single device can be 60 % higher or 30 % lower than the median value (see error bars). The conventional life tests data have been available from the component supplier [24].

2.6.2 GaAs MESFET saturation current I_{DSS}

Figure 2.16 shows the degradation at saturation current condition. The device ageing at saturation current is significantly faster compared to the pinch-off condition as can be seen in table 2.3. This difference is caused by the increased device self heating at I_{DSS} condition which induces an additional acceleration of the device ageing. As the device self heating at $I_{DSS}/2$ is 35.5 °C, the temperature offset at

I_{DSS} is at least 71°C as the dissipated power is double as much. This is indeed a low estimate as the thermal resistance is supposed to increase with the channel temperature which leads to a positive feedback. Data for the channel temperature at I_{DSS} have not been available. For all tests presented here, the thermal resistance of the MESFETs has been supposed to remain stable during life test. The acceleration factor from 190 to 205 °C ambient temperature is determined as 1.6 ± 0.07 following equation 1.4. The corresponding activation energy of 0.6 eV is rather low for diffusion related failure. The scattering of the individual device

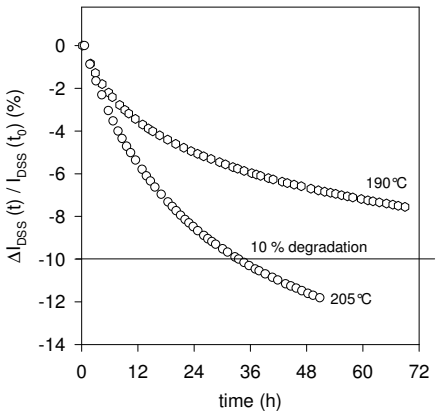

Figure 2.16: I_{DSS} drift at $T_{amb} = 190$ °C and 205 °C

parameters as in figure 2.15 leads to an error margin on the acceleration factor from -55 % to +125 % and to activation energies between 0 and 1.6 eV. In paragraph 2.9, the Overhauser-method will be presented which allows to measure the acceleration factor based on one single device eliminating this source of error. Using this method, an activation energy of (1.73 ± 0.15) eV has been measured. During the ageing experiments, the initial channel temperature was 261 °C ($T_{amb} = 190$ °C) and 276 °C ($T_{amb} = 205$ °C). Fitting the saturation current drift to a square root of time scale yields a less good correlation compared to the pinch-off data as shown in figure 2.17. The device ageing is slower than predicted by the fit which can be explained by the decrease of the channel temperature towards the end of the life test experiment. As the saturation current is decreasing, the Joule-heating

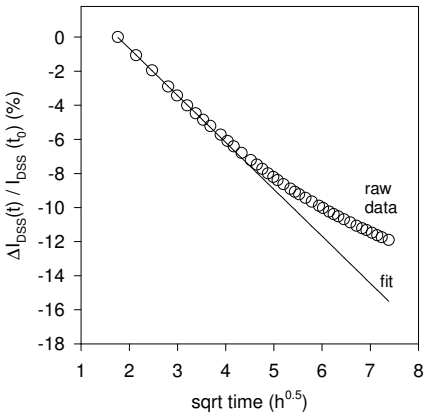

Figure 2.17: I_{DSS} drift at T_{amb} = 190 °C; raw data

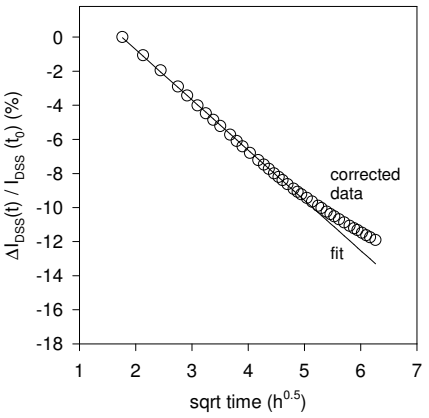

Figure 2.18: I_{DSS} drift at T_{amb} = 190 °C; data corrected for T_{ch} decrease

and therefore the channel temperature decreases. As a consequence, the thermally activated ageing is slowed down. A correction for the temperature decrease has been applied to account for the decreasing channel temperature using the activation energy from the Overhauser-tests which is shown in figure 2.18. The slowing down of the degradation could nearly be compensated and fitted to a square root of time characteristics. The reason for the residual curvature is probably due to an under-estimation of the device self heating.

2.6.3 Comparison of U_p and I_{DSS} drift and standard tests

Table 2.3 shows the degradation rates for pinch-off voltage and saturation current at 190 °C ambient temperature. The saturation current drift is about 9 times faster than the pinch-off voltage. The channel temperature for the saturation current condition and the current density are higher for the saturation current condition than in pinch-off mode of operation. At such different stress conditions, different ageing mechanisms may be activated e.g. field-related effects at pinch-off or current density related failure at saturation current. In the continuous, single parameter measurements the electrical stress condition is defined by the measured parameter.

	$\mathbf{I_{DSS}}$	$\mathbf{U_p}$
48 hours	- 6.65 %	-0.78 %
60 hours	- 7.2 %	-0.90 %

Table 2.3: I_{DSS} and U_p drift at $T_{amb} = 190$ °C

Therefore, saturation current and pinch-off voltage drift can not directly be correlated. In conventional testing, the device under test is stressed at high temperature but the device ageing is measured at room temperature [19]. The device ageing is practically stopped during the measurement of the device characteristics. The drift of the device characteristics is therefore tightly related to the stress condition. The in-situ technique is now extended to allow a similar separation of stress and measurement phases without losing the advantages of the method over conventional tests such as high data density and increased measurement accuracy. The selected stress conditions for the tests are oriented towards conditions used in industry to facilitate the comparison of results: The devices are biased at the nominal bias point for class-a mode operation which is at half saturation current ($I_{DSS}/2$) [5]. The channel temperature offset at half saturation current has been determined with $\simeq 35.5$ °C from data supplied by the device manufacturer.

2.7 Transition to switched state measurements

2.7.1 Adaptations to the test system

In the basic in-situ measurement system, the stress condition is provided by a dedicated hardware stress module permanently connected to the device under test. Now we extend the test system capabilities to the simultaneous measurement of

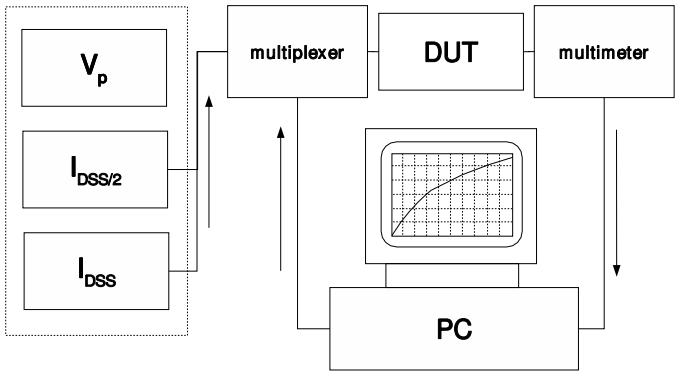

Figure 2.19: schematic of the test bench setup with multiplexing unit

multiple electronic parameters. The transition from a voltage to a current defined stress condition demands connecting and re-connecting of the drain and gate of the DUT in a well-defined order. Otherwise, transient states occur and the device may be damaged. A dedicated multiplexing unit has been developed for this purpose. The connection sequence and timing is stored and executed automatically as the acquisition of the measurement data is performed by a dedicated computer program which has also been developed in the framework of this thesis. On the diagram in figure 2.19, two multiplexer units are indicated, one for switching the stress modules, and the other to allow multiplexing of the multimeters. This hardware setup allows the cycling between several different measurement states as shown in figure 2.20.

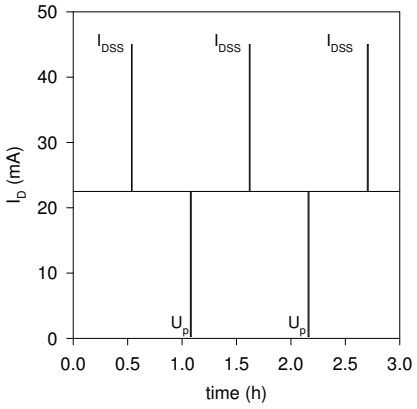

Figure 2.20: MESFET stress/measurement cycle timing setup

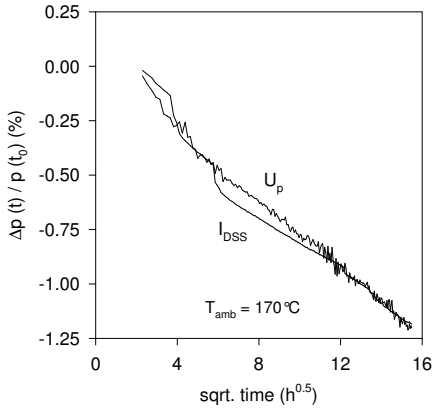

Figure 2.21: correlation between U_p and I_{DSS} parameter drift

The cycle timing is shown in table 2.4. The stress condition is $I_{DSS}/2$ which resembles the stress condition in standard tests. This stress condition prevails for more than 98 % of the measurement time. The additional measurement parameters are pinch-off voltage and saturation current. The measurement of the saturation current is as short as possible in order to minimise thermal over-stress. The effect of thermal overstress on the measurement results be discussed in more detail in section 2.8.

state	**condition**	I_D	**mode**	**time**	**parameter**
1	U_p	300 μA	const. current	30 s	gate voltage
2	$I_{DSS}/2$	22.5 mA	const. current	1925 s	gate voltage
3	I_{DSS}	$\sim$ 45 mA	const. voltage	20 s	drain current
4	$I_{DSS}/2$	22.5 mA	const. current	1925 s	gate voltage

Table 2.4: stress/measurement cycle setup

2.8 Estimation of the effect of thermal excursion on the ageing

For an Arrhenius process, even a symmetric thermal excursion will lead to a net acceleration of the ageing. This effect is due to the exponentially increasing acceleration factor of equation 1.4 as shown in figure 2.23. We calculate now the error on the stress condition of the switched state measurement compared to a hypothetically single-state measurement performed at $I_{DSS}/2$, assumed that $E_a = 1.6$ eV. The total acceleration for the switched cycle measurement can be written as:

$$A_{F\ cyc} = \frac{t_{I_{DSS/2}}}{t_{tot}} A_{F\ IDSS/2} + \frac{t_{Up}}{t_{tot}} A_{F\ Up} + \frac{t_{IDSS}}{t_{tot}} A_{F\ IDSS} \qquad (2.23)$$

with:

A_{Fcyc}	:	acceleration for cycled measurement relative to stress condition
$A_{FI_{DSS}/2}$	:	acceleration at stress condition $I_{DSS}/2$
$A_{FI_{DSS}}$	:	relative acceleration at saturation current
A_{FU_p}	:	relative acceleration at pinch-off voltage
t_{tot}	:	total measurement time
$t_{\text{“level”}}$	:	time at specific stress state “level”

After careful calculation, it turns out that the ageing is accelerated by 8.5 % which is remarkable as the I_{DSS} phase accounts only for 0.5 % of the total stress time. As a consequence, it is of high importance to minimize thermal overstress to the device under test.

2.8.1 Results of the switched state measurements

For the continuous measurements of one single parameter we observed a significant degradation of the saturation current compared to the pinch-off voltage drift, caused by increased Joule heating. Figure 2.21 show the results of a 240 hours accelerated ageing test using the stress/measurement cycle as in table 2.4. The ageing is here defined by the $I_{DSS}/2$ stress condition. It can be observed that the relative drift of saturation current (-1.2 %) and pinch-off voltage (-1.18 %) are nearly equal, the difference being smaller than 2.5 %. As explained in section 2.4.1, the diffusion depth for this short-time test is in the range of one or two atomic layers, one atomic

layer having a thickness of 5.65 Å. 2.5% saturation current degradation means an effective thinning of the channel of the same percentage. The channel thickness of the MESFET is in around 50 nm. This results in an estimate thinning of the channel of 1.25 nm or 12.5 Åwhich is of the same range as predicts by the simple model for gate sinking which has been presented earlier in section 2.4.1. This stadium of gate sinking can not be detected by analytical means as the diffusion depth is too small.

2.9 Determination of the activation energy with the Overhauser method

In order to extrapolate the device life time to normal operating conditions, we need to know the activation energy of the degradation process. The statistical scattering of the electrical device parameters leads to unusable results on the activation energy value as we have seen for the continuous saturation current measurements in section 2.6.2. This difficulty can be eliminated with an Overhauser temperature step stress experiment which allows the measurement of the acceleration based on a single device [25]. Figure 2.22 shows the result of a temperature step stress on

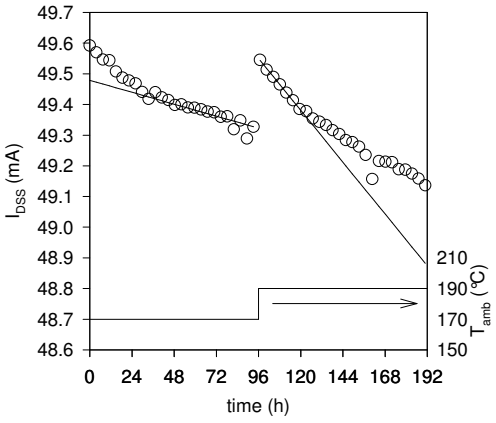

Figure 2.22: Overhauser-experiment on MESFET saturation current drift; data: circles; fit: solid line

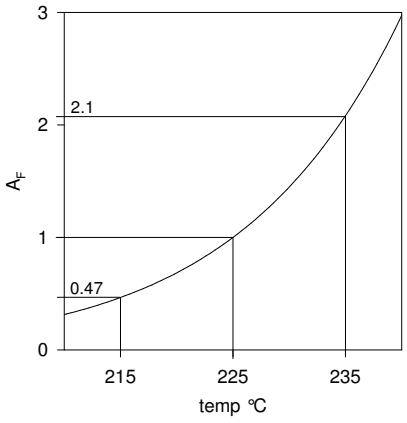

Figure 2.23: relative acceleration factors for $T_{ch} = 225\,°C$ and $E_a = 1.6$ eV

the MESFET saturation current drift. At the beginning, the ambient temperature is switched to 170 °C. After 96 hours, the ambient temperature is switched to 190 °C and the device ageing is accelerated. For the devices under test, the saturation current increases with the temperature. The saturation current is mainly governed by two effects, the decrease of the carrier mobility (see table 2.1 and the decrease of the built-in gate potential. Due to the decrease of the current carrier mobility, the saturation current is expected decrease. This effect is counteracted by the decrease of the gate potential which leads to a lower effective gate voltage and thus a higher drain current. The resulting saturation current temperature characteristics depends on the specific device geometry. The slope D_S of the degradation of the saturation current at the transition time t* for a given temperature T is defined as:

$$D_S(t^*, T) = \left(\frac{dI_{DSS}}{dt} \right) \Bigg|_{t^*, T} \tag{2.24}$$

with:

D_S : degradation slope

The ratio of the slopes at T_1 and T_2 determines the acceleration factor A_F :

$$A_F = \frac{E_a}{k_B T} \exp\left(\frac{1}{T_1} - \frac{1}{T_2} \right) \tag{2.25}$$

with:

T_1 : lower temperature
T_2 : higher temperature
A_F : acceleration factor
E_a : activation energy in electron volt
k_B : Boltzmann's constant

This acceleration factor allows then to calculate the activation energy E_a:

$$E_a = \ln(A_F)\ k_B \left(\frac{1}{T_1} - \frac{1}{T_2} \right)^{-1} \tag{2.26}$$

We get channel temperatures of T_1 = 241 °C and T_2 = 261 °C after correction for Joule heating. Applying equation 2.26 yields an activation energy of (1.73eV ±

0.15) eV which is well in the range reported in literature for gate sinking [26]. Extrapolating the data of figure 2.21, a saturation current degradation of 10 % will be obtained after 16900 hours at T_{ch} = 225 °C. The device life time under standard operating conditions at T_{ch} < 125 °C for this particular failure mechanism is extrapolated to 50000 years of operation.

2.10 Conclusions for this chapter

The feasibility of the in-situ measurement method for the life testing of active electronic components has been demonstrated in this chapter. The parameters for life testing have been in accordance with standard test procedures as established in industry. The measurement setup is basically different for passive two- and active three-terminal devices. As active devices are designed for signal amplification, special care has to be taken concerning the suppression of noise signals in the measurement setup which may lead to electromagnetic interference. This has been achieved by shielding and filtering.

The accuracy of the test bench for active devices attains a degree of accuracy which is comparable to the HRRMT setup for passive components. The high resolution and accuracy allows the extrapolation of the expected device life time based on test results obtained within a few days. This is a significant savings on time and cost compared to the several thousand hours of testing which are required when using conventional techniques.

The test conditions must be selected with respect to the expected ageing mechanism. With help of numerical analysis of the degradation data and physical modelling, gate sinking was identified as dominant physical ageing mechanism for the tested MESFET devices. Modelling device degradation is a necessary tool as the physical degradation can often not be detected by analytical means as the damage zone is only a few atomic layers small.

Measuring electrical parameters under current stress leads to substantial device self heating can not be avoided. In order to obtain a well-defined device temperature, the constant current loop was been developed which allows to keep the dissipated power and therefore the self-heating at a constant level.

For continuous, steady-state measurements, the measured parameter defines simultaneously the electrical stress condition and the amount of device self-heating. Measurements of different electrical parameters at the same ambient temperature are difficult to compare as both current stress and device temperature are different. With the application of the stress/measurement cycles, the device ageing is defined by the stress condition which prevails for the most part of the stress/measurement cycle. The degradation of device parameters is now correlated by this stress condition which facilitates comparison with results from standard tests.

2.11 References for this chapter

[1] L. Stals, L. De Schepper, J. Roggen and W. De Ceuninck, European patent no. 0 395 149 B1 (1990).

[2] H. Nyquist, Phys. Rev. **32** (1928).

[3] A. Shul'man, Sov. Phys. JETP **54**, 420 (1981).

[4] Keithley, editor, *Low-Level Measurements, Precision DC Current, Voltage and Resistance Measurements*, 5 ed. (Keithley Instruments, U.S.A, 1998).

[5] U. Tietze and Ch. Schenk, *Halbleiter-Schaltungstechnik*, tenth ed. (Springer-Verlag, 1993).

[6] H. Callendar, Philosophical Transactions of the Royal Society of London A **178**, 161 (1887).

[7] I. E. C. IEC, IEC 751 Standard for performance for 100 ohm 0.00385 alpha platinum rtds, 1983.

[8] W. D. Ceuninck, L. Stals, L. De Schepper and J. Roggen, European patent no. EP 0 733 909 A1 (1996).

[9] T. Veijola and M. Andersson, Proceedings of ECCTD , 754 (1997), Bupapest, Hungary, August 30 - September 3.

[10] R. Petersen, W. De Ceuninck and L. De Schepper, Proceedings of the 8$^{\text{th}}$ IEEE 2000 High Frequency Postgraduate Student Colloquium , 20 (2000).

[11] F. Christians and E. Beyne, IMEC report for ESA ESTEC Contract No. 8615/90/NL/PM(SC) (1996).

[12] V. Goldschmidt, Trans. Faraday Soc. **25**, 253 (1929).

[13] H. Welker, Zeitschrift für Naturforschung A **7**, 744 (1952).

[14] S. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).

[15] R. Petersen W. De Ceuninck, L. De Schepper and G. Grégoris, Microelectronics Reliability **37**, 1655 (1997).

[16] J. Dumas, (1991), the first step for a technological evaluation.

[17] K. Mzuishi, H. Kurono and Hitoshi Saito, IEEE transactions on electron devices **ED-26** (1979).

[18] J. Irvin and A. Loya, The Bell System Technicam Journal **57**, 2823 (1978), American Telephone and Telegraph Company, October 1978.

[19] JEDEC solid state technology association, JEDEC standard JESD22-A108-B (Revision of JESD22-A108-A), 2000.

[20] A. E. Fick, Ann. Physik, Leipzig **170**, 59 (1855).

[21] S. Arrhenius, Zeitschrift für Physikalische Chemie Stochiometrie und Verwandtschaftslehre **4**, 226 (1889).

[22] A. Benssoussan, P. Coval, W.J. Roesch and T. Rubalcava, IEEE/IRPS , 434 (1994).

[23] P. Ladbrooke, *MMIC design : GaAs FETs and HEMTs* (Artech house, 1989).

[24] Alcatel Espace, *Life test data on pinchoff-voltage and saturation current drift on 0.25 μm MESFET's at 205 and 225 $^\circ C$ channel temperature*, Toulouse, France, 1994, internal report on device reliability.

[25] A. Overhauser, Phys. Rev. **90**, 393 (1953).

[26] A. Christou, editor, *Reliability of Gallium Arsenide MMICs, Design and measurement in electronic engineering* (John Wiley & Sons, 1992).

Chapter 3: Extension to full software control and application to pHEMTs

3.1 Introduction

In chapter 2, the applicability of the in-situ technology has been demonstrated on GaAs MESFETs. This in-situ technique will now be applied to pseudomorphic high electron mobility transistors (pHEMTs). In the basic setup, the setup of the different stress and measurement states demanded dedicated hardware modules which were connected to the DUT by a multiplexing unit. The multiplexing rendered the measurement process complicated and provided a source of hazard to the DUT. A solution was sought to eliminate the need for multiplexing. This lead to the development of digitally controlled voltage/current supply modules. These supply modules allow the device to remain permanently connected to the test setup. These modules can easily be programmed enabling the flexible definition of the measurement conditions by software.

3.1.1 Development of dedicated power supplies

Digital power supplies (DPSs) have been designed which offer the necessary accuracy and stability. Prior to the development of the dedicated power supplies, a range of commercially available digital controlled power supplies was assessed. It was found that these commercial supplies were not suitable for the test bench system due to several reasons: Most commercially available power supplies are of the switched type in order to save cost and to increase the power efficiency. Inside a switched power supply, the output voltage is regulated by switching the input voltage at a variable pulse-width of frequency. The appearance of spurious ripple related to the internal switching frequency imposes a high amount of noise on the output

voltage. Another source of concern are transient voltages. Standard power supplies are designed to deliver constant supply voltages under varying current loads. For use in a test bench, the output voltage must often be switched from one level to an other. While switching commercial power supplies, transient voltage peaks appear as shown in figure 3.1.

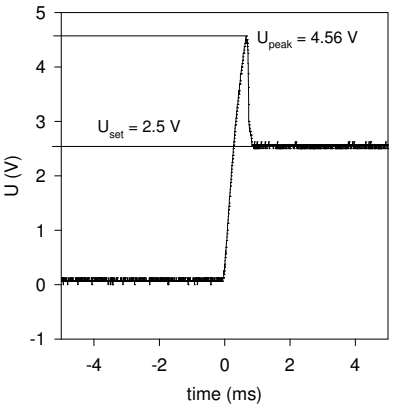

Figure 3.1: transition from 0 to 2.5 V of a commercial power supply

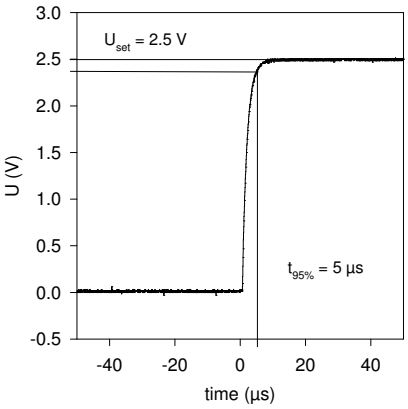

Figure 3.2: transition from 0 to 2.5 V of the digital power supply developed for the in-situ test bench

	sampling time	**pulse shape**	**thermal property**
continuous	< 1 PLC	continuous	thermal balance, hot
slow pulse	100 ns...1 PLC	1 PLC + trigger delay	near thermal balance
fast pulse	< 100ns	> 100 ns	cold

Table 3.1: DC measurement modes and thermal properties

Even if the transient voltage decays in less than 1 ms, such voltage peaks are sufficient to destruct electrically sensitive devices such as MESFETs and pHEMTs. The newly developed test bench power supplies deliver a bipolar voltage which is defined by a digital to analog converter (DAC). This DAC has originally been designed for audio applications and is optimised for fast settling time and low current overshoot. The DAC delivers a current of $\pm$ 1.2 mA. This current is transformed

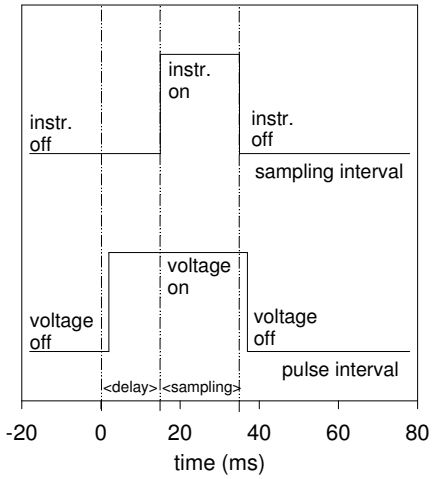

Figure 3.3: timing diagram for slow pulsed measurements

into a voltage by a transconductance amplifier which amplification is adapted to deliver the voltage ranges needed for life testing. The voltage range is ± 12 V for the drain and ± 3 V for the gate voltage. The DAC has a resolution of 20 bit which comes down to 24 μV voltage steps for the drain and 6 μV steps for the gate voltage supply. The worst-case *accuracy* of the DAC is guaranteed to be better than 15.5 bits. This is a substantial advantage compared to commercially available power supplies which offer at best 12 bit resolution (4096 steps). Such small voltage steps are essential for the application of the DPS in the constant current feedback loop. The over-all accuracy of the DPS output voltage depends on several factors as DAC manufacturing tolerances, set-point voltage, transconductance amplifier, ambient temperature and current load. These factors may lead to a significant offset of several ten millivolts if not compensated. The compensation is performed by an automatical offset correction during life test: In constant current mode, the gate voltage is measured by a HP 3458a multimeter with 8 1/2 digits resolution. For the characterisation of the device, this measured gate voltage is used instead of the set voltage. In constant voltage measurement mode, offsets between set voltage

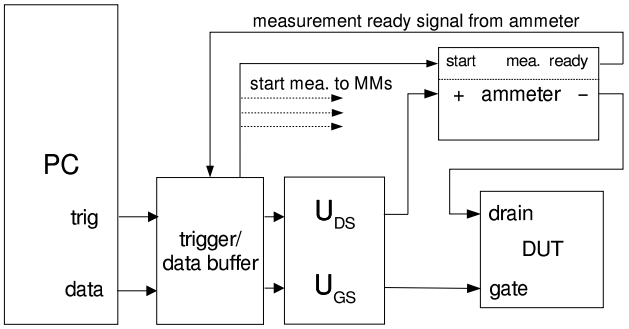

Figure 3.4: signal flow for slow pulsed measurement setup

and measured voltage are compensated by adjusting the PPS voltage to the value closest to the set-point voltage.

The transition characteristics of the DPSs were optimised for short rise time but also for stability under capacitive load. The rise time to 95 % of the preset output voltage of the digital power supply is less than 5 μs as can be seen in figure 3.2. For comparison, the time scale of figure 3.2 is 100 times faster than for figure 3.1. The minimum attainable pulse length of the DPS is 52 μs. Pulsed mode measurements are advantageous to minimise thermal stress on the DUT. However, to achieve a really "cold" measurement with nearly complete suppression of self-heating, the pulse duration must be shorter than 100 ns as shown by Rathmell et al. [1]. In the measurement system, the minimum practical pulse length is defined by the minimum sampling time of the used current meter which is 200 μs. At this pulse length, the device channel is thus already heated up. The measurement with such "slow" pulses (see table 3.1) has however beneficial effects. Between measurement pulses, there is no current stress to the DUT. As the time between pulses is typically much longer than the duration of the measurement pulse, thermal over-stress can be avoided. Figure 3.3 shows the timing diagram for the slow pulse measurement using a pulse length of 1 PLC. After a trigger signal is sent, the voltage is switched immediately. After a pre-set measurement delay of 15 ms, the multi-meters start sampling. This measurement delay is necessary to allow the current meters and the DUT to stabilise. The applied current meters uses an internal compensation circuitry to minimise the "burden voltage". When the sampling is finished, the multi-meters

send a "measurement-ready" signal to the trigger unit which sets the power supplies off. In the former, basic setup the constant drain current measurement modes as pinch-off voltage and $I_{DSS}/2$ were realised by hardware modules providing analog feedback to the gate voltage. This current loop is now realised by a software approach: First, the drain current is measured by the current meter and the measured value is transferred to the personal computer via a GPIB communication link. The measured value is then compared with the set-point value. Depending on the current offset, a new gate voltage is calculated. The calculated gate voltage is transferred to the local memory of the digital power supply and transferred to the DAC synchronous with the measurement trigger signal as shown in figure 3.5. The software contains a simple model of the device characteristics. The software

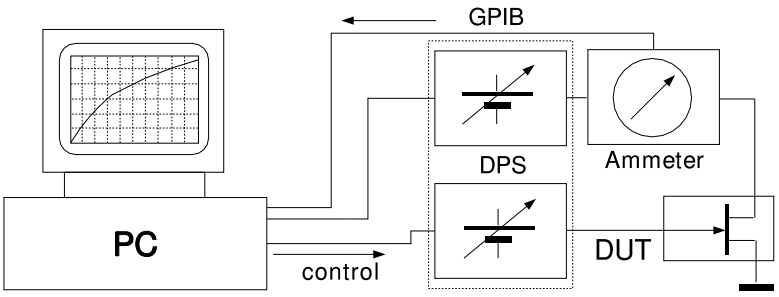

Figure 3.5: schematics of the software drain current loop

model also includes safety limits to prevent device damage. The efficiency of the software current loop depends on the regulation algorithm and execution speed. With standard PC hardware and settings, the loop is executing between 4... 20 times per second.

3.1.2 Adaptations to the device fixture

Due to their high transconductance and transit frequency, pHEMTs are susceptible to the generation of oscillations when biased. At the high operating frequency of the pHEMT, the complex impedance of the cabling can provide the necessary feedback circuitry. The amplitude of the oscillations can be sufficient to destroy the DUT. A

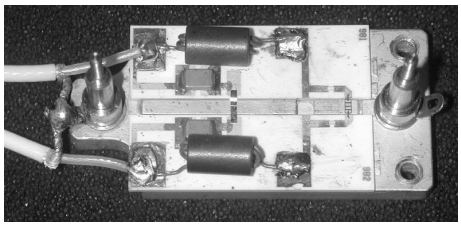

Figure 3.6: coplanar sample holder with rf-blocking filters applied

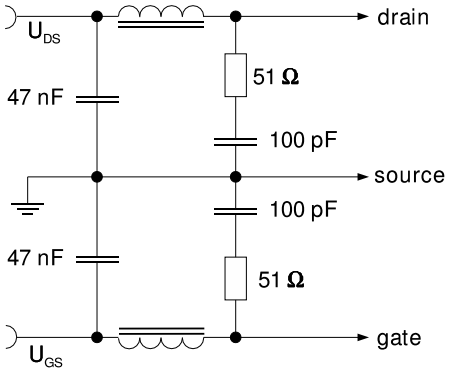

Figure 3.7: low pass filter applied for rf-blocking

special coplanar sample holder is employed to inhibit auto-oscillation. This sample holder contains a cascaded low pass filter network which is located in the direct vicinity of the DUT as can be seen in figure 3.6. The extremely small gate capacitance in the lower fF range makes HEMTs/pHEMTs highly susceptible to damage by electrostatic discharge (ESD). Special precautions have to be taken during handling to avoid that the device is subjected to undefined floating potentials. In order to connect/disconnect the DUT to the measurement equipment, a specific connection sequence has to be respected and soft-grounding should be applied wherever possible.

3.2 HEMT device technology

MESFET and GaAs HEMTs share the same basic principle of operation. The current through a conducting channel is controlled by an external gate voltage.

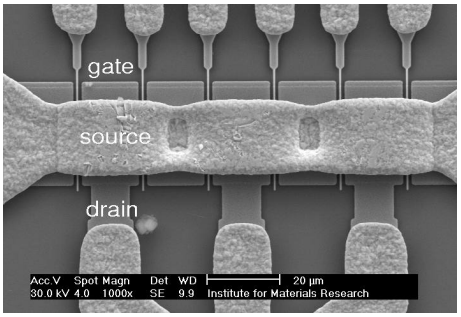

Figure 3.8: top view of the pHEMT structure

Six gate fingers are connected in parallel to allow higher drain current and transconductance as can be seen in figure 3.8. Figure 3.10 shows the basic structure of one gate finger of the actual pHEMT device used for life testing. The technological difference between HEMT and MESFET lies in the structure of the conducting channel. In a MESFET, the electrons are conducted in a n-doped bulk channel created by ion-implanted donor atoms. The channel itself provides thus the necessary charge carriers to support the current.

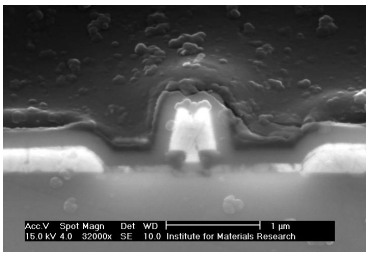

Figure 3.9: cross-section of pHEMT gate (64000x mag.)

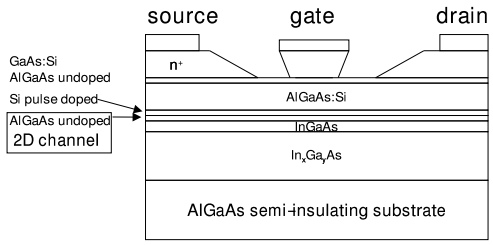

Figure 3.10: basic layer structure of the pHEMTs which have been tested

In a HEMT, the channel is formed at the interface of an epitaxially grown heterostructure. A heterostructure is formed at the junction of two semiconductor materials with different band gaps such as AlGaAs (higher bandgap) and GaAs (lower bandgap). At the heterostructure interface, electrons diffuse from the material with the higher conduction band energy into the material with the lower conduction band energy. The penetration depth of the electrons into the undoped

material is only several nanometers thick depending on the conduction band energy difference and the doping concentration in the donor layer. The channel electrons are thus separated from the donor layer and the conduction takes place in a very thin, quasi two-dimensional zone at the interface inside the undoped material. As no dopant atoms are present which serve as electron scattering centres (Coulomb-scattering) the electron mean free path is increased which results in a reduction of noise compared to the MESFET technology. HEMTs are found in applications where low noise properties are important and the higher wafer costs compared to the MESFET process can be tolerated. One main application range of HEMTs are pre-amplifier stages in microwave receivers. A shortcoming of HEMTs compared to MESFETs is the reduced current carrying capability as the channel is very thin. HEMT and pHEMT are similar except a "pseudo-morphic" electron donor layer. For pHEMTs, InGaAs instead of AlGaAs (thickness typically 5 to 20 nm) is used. The conduction bandgap of InGaAs is higher than the conduction bandgap of AlGaAs. This leads to a higher electron injection efficiency into the channel. The junction of two different semiconductors like GaAs and InGaAs is known as "heterojunction". The crystal lattice constant of InGaAs is only slightly higher (0.587 nm for $In_{.53}Ga_{.47}As$) and for AlGaAs (0.565 nm). InGaAs can be grown directly on GaAs without introducing defects to the crystal lattice but mechanical strain is induced to the thin InGaAs layer. This leads to a tetragonal distortion of the InGaAs lattice as adaptation to the buffer layer as described by Matthews [2]. HEMTs with such a lattice mismatched heterostructure are called pseudo-morphic HEMTS or short, pHEMTs. Table 3.2 gives an overview over the different layers of MESFET, HEMT and pHEMT.

	MESFET	**HEMT**	**pHEMT**
Ohmic contact	n+ GaAs	n+ GaAs	n+ GaAs
Schottky contact	n GaAs	nAlGaAs	nAlGaAs
donor		n+ AlGaAs or Si pulse doping	n+ AlGaAs or Si pulse doping
spacer		undoped AlGaAs	undoped AlGaAs
channel	n+ GaAs	undoped AlGaAs	undoped AlGaAs
buffer	p- GaAs	p- GaAs	p- GaAs

Table 3.2: layer structure of MESFET, HEMT and pHEMT

3.3 HEMT/pHEMT failure modes

Most HEMT/pHEMT failure modes are similar as for MESFET devices as the material composition of the Schottky and Ohmic contacts is the same for the devices under test. Attention must be paid due to the restricted channel dimensions of the HEMT/pHEMT device. To achieve maximum transit frequency, the parasitic capacitances have to be minimised. In addition to the application of a recessed channel -also applied for MESFET devices-, the gate contact is often formed in "T" or mushroom shape to reduce the gate/channel capacitance. This is achieved by under-etching the gate, a delicate process which renders the gate structure fragile and susceptible to ESD (ElectroStatic Discharge) damage. The gate composition of the devices under test is shown on figure 3.9. When gate contact material diffuses deep enough into the channel, this leads to a collapse of the 2D-confinement of the channel. As a result, the HEMT device operates as an ordinary MESFET with electron conduction in the bulk channel. This effect can be detected by an increased low-frequency noise and a lowered transit frequency f_T of the device [3].

parameter	**min. value**	**typ. value**	**max. value**
$\mathbf{I_{DSS}}$	12 mA	25 mA	40 mA
$\mathbf{U_p}$	-0.3 V	-0.7 V	-1 V
$\mathbf{g_m}$		50 mA/V	65 mA/V
$\mathbf{I_{GS}}$		1 μA	5 μA
$\mathbf{U_{DG}}$			5 V
$\mathbf{U_{GS}}$			-5 V
$\mathbf{U_{DS}}$			5 V
$\mathbf{I_D}$			70 mA
$\mathbf{P_{diss}}$			350 mW
$\mathbf{T_{amb}(P_{diss} = 0)}$			150 ° C

Table 3.3: electrical characteristics for the pHEMT devices at room temperature and 2 V drain voltage; I_{GS} = gate-source leakage current

Table 3.3 shows the typical and the maximum ratings for the devices under test at room temperature and 2 V drain voltage [4].

3.4 Design of the ageing experiment

A lot of twelve pseudomorphic HEMTs was submitted to thermo-electrical stress. The stress profile has been chosen according to tests following the industry standards which have been performed by Alcatel Espace. As in the last chapter, data from these conventional tests will be compared with the in-situ results. The selection of electrical and thermal test parameters follows the procedure presented by Saysset et al. [5] for the study of diffusion-related failure mechanisms. The drain voltage has been set to 2 V and a drain current of $I_{DSS}/2$ has been chosen which is the recommended low-noise operating condition for this device. During the $I_{DSS}/2$ stress phase, saturation current (I_{DSS}) and pinch-off voltage (U_p) have been measured intermittently. Table 3.4 shows the stress/measurement cycle setup. This setup is now discussed in greater detail.

1. Measurement state 1 is the device pinch-off voltage. The pinch-off voltage has been measured at 1% of the initial I_{DSS} at room temperature. A time of 40 seconds was allowed to reach thermal equilibrium and to stabilise the drain current.

2. Measurement states 2 and 5 are identical (stress condition $I_{DSS}/2$). This splitting allows the thermal settling of the device between thermal excursions.

3. Measurement state 3 is the same as state 2 with additional measurement of the gate current.

4. The saturation current I_{DSS} (state 4) is measured only once per cycle to avoid thermal over-stress. One single data point is measured to avoid thermal over-stress to the DUT.

5. State 5 is the same as state 2

6. State 6 ($I_{DSS}/2$ at U_{GS} = const.) is introduced to ensure compatibility with the Alcatel standard measurement procedure. The two measurement modes are equivalent as can be looked up in the appendix.

Figure 3.11 shows the measurement cycle timing (solid line) along with the residual temperature excursions caused by power dissipation changes. The times for each state are shown in table 3.4. Those temperature excursions were measured at the

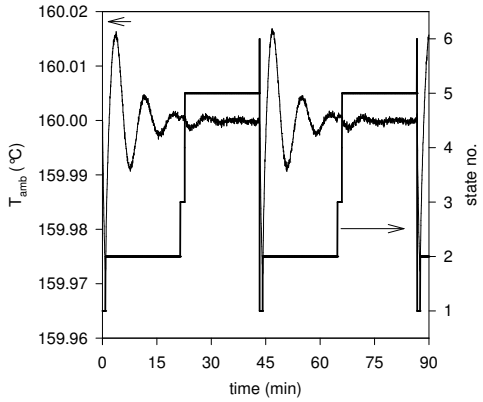

Figure 3.11: measurement cycle timing (solid line) and temperature excursion at $T_{amb} = 190$ °C

state	parameter	meas.	averaging	PLC	total time
1	$\mathbf{U_p(1\%I_{DSS})}$	10	1	1	40 s
2	$\mathbf{I_{DSS}/2}$	500	10	1	1250 s
3	$\mathbf{I_{DSS}/2 + I_G}$ **meas.**	20	10	1	100 s
4	$\mathbf{I_{DSS}}$	1	1	0.01	350μs
5	$\mathbf{I_{DSS}/2}$	500	10	1	1250 s
6	$\mathbf{I_{DSS}/2(U_{GS} = const.)}$	20	1	1	25 s

Table 3.4: stress/measurement cycle setup

case of the device. One group of six samples has been tested at 160 °C, another group at 185 °C ambient temperature. In this temperature range, the pHEMT is still fully operational. The channel temperature limit for HEMT/pHEMTs is about 250 °C, exceeding this temperature causes a (recoverable) collapse of the confinement of the 2D electron gas.

3.5 Observations on the ageing characteristics

The following figures give an overview of the device degradation under thermo-electrical stress in the different measurement states. All pHEMTs show an initial enhancement of the electrical characteristics during the first 24 hours of life test. To facilitate the comparison, the degradation data are plotted on a relative scale.

3.5.1 Degradation at stress condition

Figures 3.12 and 3.13 show the device degradation of the gate voltage U_{GS} at stress condition $I_{DSS}/2$ in constant current mode.

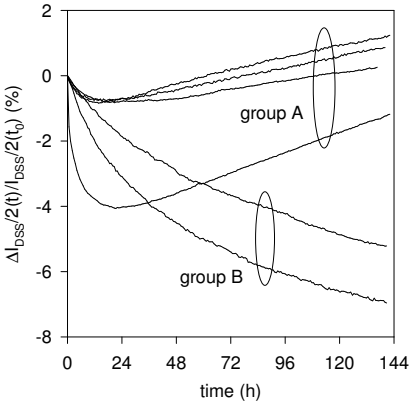

Figure 3.12: $U_{GS}(I_{DSS}/2)$ drift at $T_{amb} = 160$ °C (states 2 and 5)

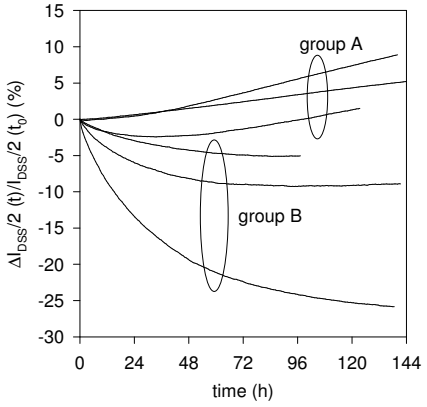

Figure 3.13: $U_{GS}(I_{DSS}/2)$ drift at $T_{amb} = 185$ °C (states 2 and 5)

From their degradation behaviour, the DUTs can be divided into two groups named "A" and "B": The samples of group A show an initial increase of their characteristics. After several hours, a reversal occurs, resulting in a final degradation of the electric parameters. Initial enhancement as well as final degradation for group A samples are well-correlated for all measured parameters I_{DSS}, $I_{DSS}/2$ and $|U_p|$. The samples of group B show a strong monotonic enhancement of their characteristics which is observed for all measured parameters.

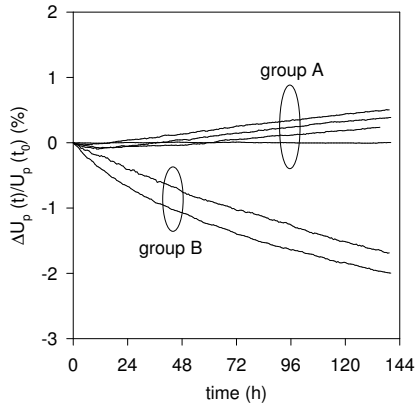

Figure 3.14: $U_p(t)$ ageing at T_{amb} = 160 °C (state 1)

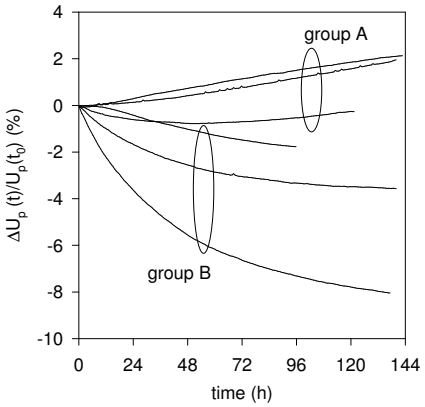

Figure 3.15: $U_p(t)$ ageing at T_{amb} = 185 °C (state 1)

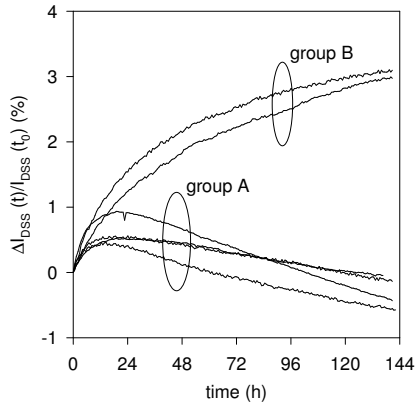

Figure 3.16: $I_{DSS}(t)$ ageing at T_{amb} = 160 °C (state 4)

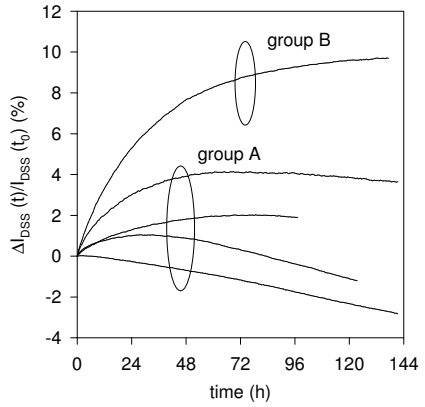

Figure 3.17: $I_{DSS}(t)$ ageing at T_{amb} = 185 °C (state 4)

3.6 Analysis of the degradation measurements

A good correlation is observed for the degradation between the measurement parameters I_{DSS}, $I_{DSS}/2$ and U_p. Figure 3.18 which shows the drift of the gate voltage

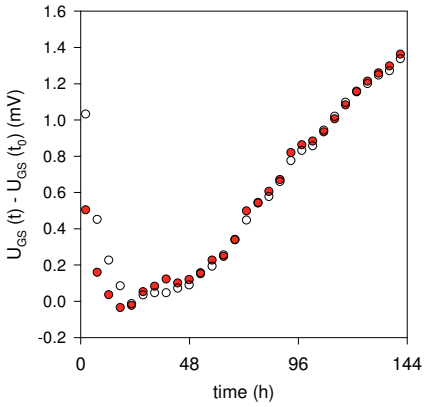

Figure 3.18: gate voltage drift at $I_{DSS}/2$ (open symbols) and U_p (closed symbols)

for the pinch-off voltage and the $I_{DSS}/2$ measurement. This gate voltage drift for the two parameters is the same over the whole test time. From this observation we can conclude that as well the first as the second degradation mechanism is linked to a drift of the effective gate voltage.

For sake of clarity, the figures in the following paragraphs are showing just one exemplary device from group A and one from group B. The observations on the degradation characteristics are also valid for all other devices from the respective group.

The distribution of the devices under test into groups A and B has been made with respect to their degradation characteristics for drain current related parameters. This distinction which may seem somewhat artificial will become clearer at the end of this discussion.

3.6.1 Ageing behaviour of group A devices

The degradation behaviour of the group A devices is composed of two distinct phases.
During the first phase the device performance increases. This performance increase is well-correlated for I_{DSS}, $I_{DSS}/2$ and U_p. This initial phase is finished after 12 to 30 hours at 160 °C ambient temperature and 4 to 8 hours at 185 °C.
During the second phase, the device performance degrades slowly. This second phase is also well-correlated for I_{DSS}, $I_{DSS}/2$ and U_p.
We will discuss the device degradation characteristics now more in detail.

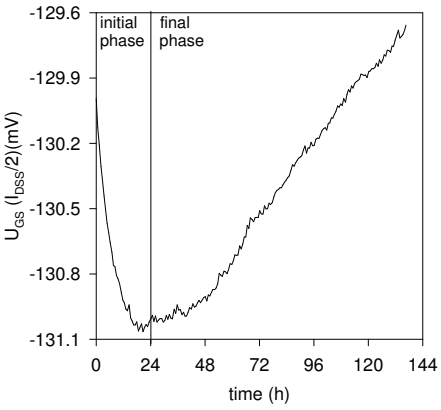

Figure 3.19: $U_{GS}(I_{DSS}/2)(t)$ for a device from group A

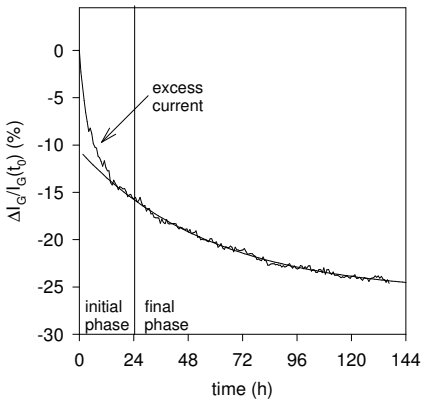

Figure 3.20: gate current drift of a group A device

Figure 3.19 on the left shows the gate voltage drift at stress condition and figure 3.20 on the right shows the gate leakage current for the same period of time.
The gate current characteristic serves here as a sensitive indicator for possible structural defects: at stress condition ($I_{DSS}/2$), the gate Schottky diode is reversibly polarised and the gate current should ideally be small. At the high test temperatures, the gate current is increased compared to room temperature due to the thermionic emission of electrons in the depletion zone. Additional to the thermionic current, leakage currents may occur due to the presence of shallow traps in the vicinity of the gate. These leakage currents can be orders of magnitude higher than the

thermionic current. The gate leakage current for group A devices can be fitted to an annealing function. Annealing processes with a constant rate of anneal λ have a time dependency described by the following equation:

$$I_G = I_G(t_\infty) + a_1 \; e^{\lambda(-t)} \tag{3.1}$$

with:

λ : constant annealing rate

a_1 : fit factor first phase

The gate current characteristic and the fit are shown in figure 3.20. The comparison between the left and the right figures reveals an interesting correlation between gate leakage current drift and the degradation of the drain current related parameters. We observe also two distinct phases. The fit agrees well with the gate current characteristic except for the first 20 hours of life test which coincides with the initial phase of life test. During the initial phase, an excess gate current is present which correlates with the initial enhancement of the device performance which may be attributed to the annealing-out of surface defects. During the second phase, a slowly exponentially decreasing gate current is observed as residual defects deeper in the gate region are annealed out. The occurrence of surface leakage currents does not necessarily affect the degradation of the intrinsic transistor but may lead to a change of the effective gate voltage. The changes in the layer structure of HEMTs during annealing is described by Okubura [6]. Figure 3.21 shows the second phase for the $U_{GS}(I_{DSS}/2)$ of the device ageing for group A. The degradation of the drain current related parameters I_{DSS}, $I_{DSS}/2$ and U_p of the group A devices exhibit a square root of time degradation characteristics which is well-correlated for all parameters. The ageing characteristic is fitted to a square root of time function of the form:

$$U_{GS} = U_{GS}(t_0) + a_2 \sqrt{(t - t_0)} \tag{3.2}$$

with:

a_2 : fit factor second phase

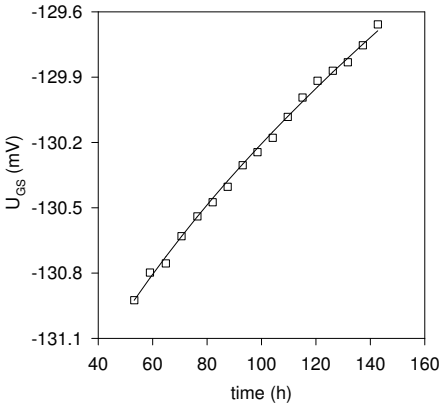

Figure 3.21: square root of time fit of the second degradation characteristics of $U_{GS}(I_{DSS/2})$

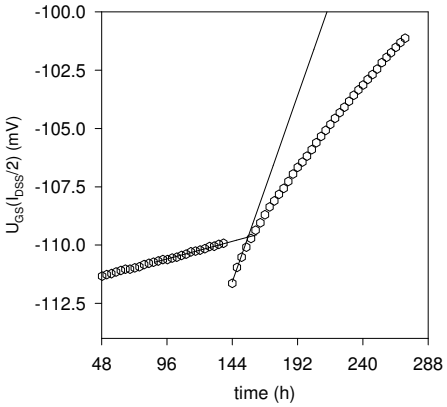

Figure 3.22: Overhauser experiment on final degradation characteristics; measurement state: $U_{GS}(I_{DSS}/2)$

The two distinct ageing characteristics for group A devices is caused by at least two concurrent degradation mechanisms.

- The initial phase of device performance increase has been identified as annealing-out of surface defects which anneal out during the first hours of life test.
- After this initial phase, the device is performance is degraded by gate sinking.

The activation energy for the second degradation mechanism is determined with help of an Overhauser [7] experiment similar as for the MESFET devices in the last chapter: after 144 hours of device ageing at 160 °C ambient temperature (T_{jct} = 175 °C), the temperature is switched to 185 °C (T_{jct} = 200 °C). The resulting acceleration is shown in figure 3.22. The activation energy E_a is 1.72 eV ± 0.15 eV which is the same as for the MESFETs. The tested pHEMTs and MESFETs share the same AuGeNi gate metal layer structure so we may safely assume that gate sinking is present for both device types. By extrapolating equation 3.2 to 10 % device degradation, which is a common failure criterion, we obtain a time to failure of 3000 hours under life test conditions. By extrapolation we get 2400 years of device operation under standard conditions at T_{amb} = 85 °C and I_D = 15mA($\simeq I_{DSS}/2$).

3.6.2 Ageing behaviour of group B devices

The devices from group B show a monotonous increase of their performance for I_{DSS}, $I_{DSS}/2$ and U_p. Figure 3.23 shows the decrease of the gate voltage at pinch-

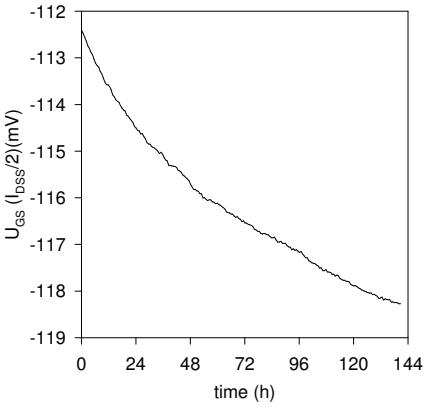

Figure 3.23: $U_{GS}(I_{DSS}/2)$ drift for a device from group B

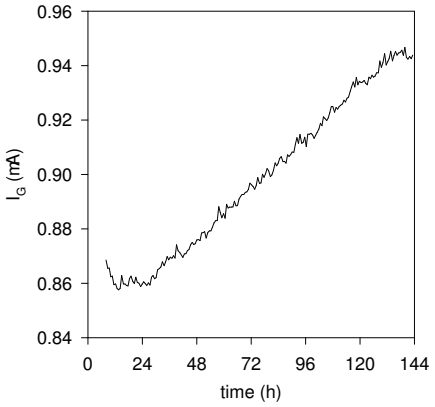

Figure 3.24: gate current drift at $T_{amb} = 160$ °C

off condition and Figure 3.24 the gate current characteristic of a group B device. We observe a monotonous enhancement of the device characteristics in terms of the drain current related parameters I_{DSS}, $I_{DSS}/2$ and U_p. During the first 24 hours, we observe a slight decrease of the gate current which is far less pronounced than for the devices from group A. After 24 hours the gate current start to increases monotonously until the end of life test. This is a clearly different behaviour compared to the devices from group A where the gate current is finally decreasing. To protect the pHEMT from oxygen, a silicon nitride (Si_3N_4) passivation layer is grown on top of the channel. The deposition of this layer is quite critical as the gate electrode is under-etched and may introduce defects in the vicinity of the gate. The developing gate leakage current may be attributed to a damaged passivation layer. A possible contribution by gate sinking, which can be also assumed for group B devices, is masked by the passivation layer damage (see figures 3.12 and 3.13 for $I_{DSS}/2$ current stress). The degradation of group B is clearly different compared to group A which justifies the distinction between the two groups.

3.7 Correlation of in-situ life results with standard life test data

Data from standard life tests were available which have been compared with the in-situ results. All pHEMT devices which were tested with the in-situ method showed at least an initial enhancement of their characteristics which could be attributed to annealing effects. Assuming an activation energy of 0.5 eV for the annealing of trap related defects as described by Saysset [8], the initial parameter improvement is equivalent to approx. 30 hours $I_{DSS}/2$ stress at 160 °C and 14.25 hours at 185 °C ambient temperature. Virgin devices have been used for the in-situ measurements. The devices from the standard test were subjected to burn-in treatment prior to life testing. The specimen used for in-situ testing had no burn-in treatment and the annealing phase is observed during the life test. The burn-in treatment of the pHEMTs for the standard tests consisted of DC-biasing the devices under test at U_{DS} = 2 V and I_D = 12 mA (equivalent to $I_{DSS}/2$ stress) at 125 °C ambient temperature for 96 hours. During burn-in, crystal defects are annealed out leading to an increase of the device performance.

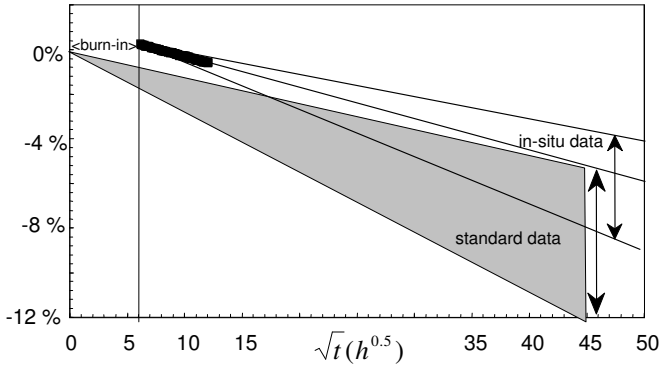

Figure 3.25: comparison of extrapolated in-situ test results (upper triangle) with data from conventional tests (lower triangle)

For the comparison with the standard tests, the initial time t_0 must be re-scaled to take account for the additional stress due to burn-in. Despite the re-scaling, the

samples tested with the in-situ method degrade slower by a factor of about 1.5 as it can be seen in figure 3.25. An important difference between the industry and the in-situ stress condition is the application of constant $I_{DSS}/2$ current stress (as introduced in chapter 2) for the in-situ measurement. During the conventional test, the gate voltage has been adjusted once at the beginning of the life test and the current drift was measured. As the drain current is expected to decrease with test time, this may lead to a slowing down of the ageing during the standard test as the current stress and the self heating are decreasing. The devices should therefore degrade faster in the in-situ setup. The observed slower device degradation can be explained by a lower effective ambient temperature during in-situ life testing: assuming an activation energy of 1.7 eV for the final degradation mechanism, the slower degradation is equivalent to a temperature offset of $-4\,^{\circ}\mathrm{C}$ between the in-situ and the standard test. The lower ambient temperature for the in-situ test is due to the different locations of the temperature sensors in the furnaces for standard and in-situ testing.

In the conventional system, the temperature is controlled by a global sensor placed in the furnace volume. Depending on the amount of device self-heating during testing, the case temperature may be higher by several degrees.

In the in-situ system, a temperature sensor is placed close to the DUT to provide a fast and accurate temperature regulation as indicated in figure 2.5. The DUT case temperature is effectively the reference temperature for the furnace. When the case temperature increases due to self-heating, the temperature regulator compensates by lowering the ambient temperature.

3.8 Conclusions for this chapter

The first design of the measurement system was based on analogue power supply building blocks and offered only limited versatility. Every change of the stress conditions resulted in time-consuming hardware adaptations. The transition to a completely software-controlled in-situ test bench system with dedicated digitally controlled power supplies has been realised in the framework of this chapter. In this phase of development, the test bench system was extended towards full software control of the measurement and data acquisition. Measurements on pHEMTs were performed on this novel test bench. From the technical point of view it is very important that the same performance could be obtained with the novel approach than it has been with the basic setup. With the transition to a completely and freely programmable measurement system, measurement states which had previously to be realised and multiplexed with the help of dedicated hardware modules are now freely definable. A significant amount of flexibility is gained as the modular concept of the test system allows the fast adaptation of voltage and current depending on the device technology to be tested. The appearance of multiple simultaneous degradation mechanisms adds a degree of complexity to the interpretation of the ageing characteristics of the pHEMT devices. We can distinguish two phases during the ageing experiment. The first phase is the enhancement of the device characteristics which can be traced to the initial annealing of defects. For some of the devices, this phase was dominating over the whole time of the life test experiment. The second phase consisted of gate sinking damage as it has also been observed for the MESFET devices which were investigated in the last chapter. Both degradation mechanisms can be detected by their specific degradation characteristics. Due to the presence of these burn-in effects, a minimum test time of around 240 hours was necessary to obtain reliable results. Monitoring device degradation during the ageing experiment allows to find this minimum test time empirically. Since the completion of the MESFET life tests it was obvious that the measurement parameters for life testing under thermo-electrical should span a greater range than covered by standard tests. With the conversion of the in-situ test bench to a fully software controlled system, this possibility has been realised.

3.9 References for this chapter

[1] J. Rathmell, J. Scott, A. Parker and M. Sayed, IEEE Transactions on Microwave Theory and Techniques **44**, 2718 (1996).

[2] J. Matthews and A.E. Blakeslee, Journal of Crystal Growth **27**, 118 (1974).

[3] A. Christou, editor, *Reliability of Gallium Arsenide MMICs, Design and measurement in electronic engineering* (John Wiley & Sons, 1992).

[4] Daimler Benz, *Excerpt from foundry handbook: pHEMT technology CFD-54 C*, 1994.

[5] N. Saysset, *Developpement d'une méthodologie et des techniques d'analyse associées permettant l'évaluation de la qualité et de la fiabilité des transistor 'a haute mobilité électronique*, PhD thesis, Université Bordeaux, 1996.

[6] A. Okubura, K. Tanaka, M. Ogawa, J. Kasahara, T. Haga and Y. Abe, Inst. Phys. Conf. **Ser. No. 112** (1990).

[7] A. Overhauser, Phys. Rev. **90**, 393 (1953).

[8] N. Saysset, N. Labat, A. Touboul and Y. Danto, ESREF proceedings , 389 (1995).

Chapter 4: Extension of the measurement capacity and application to HBTs

4.1 Introduction

In the previous chapters, accelerated ageing tests have been performed on MESFETs and pHEMTs at low to moderate dissipated power. In this chapter, a new technology, the heterojunction bipolar transistor (HBT) will be investigated which is designed for power applications under high power dissipation conditions. The devices under test were manufactured by United Monolithic Semiconductor corporation, based on wafers made by Kopin corporation. In the framework of reliability assessment at Kopin, life tests have been carried out in order to determine the activation energy of the thermal degradation as described in a paper by Pan [1]. The main accent in this chapter will be put on the modelling of the thermal resistance and the current dependence of the device degradation characteristics, although the results of some life tests at elevated temperatures will also be presented.

4.2 HBT device technology

In MESFETs and HEMTs, the current through the conducting channel is formed by electrons, they are *"unipolar"* devices. In the HBT, the current carriers are electrons (n-type) and holes (p-type), therefore it is called *"bipolar"*. The term "heterojunction" refers to the utilisation of junctions made from different semiconducting materials (as silicon/germanium, AlGaAs/InGaAs). The more common bipolar junction transistor (BJT) employs "homojunctions" using the same base material (silicon, germanium) for the p-layer and the n-layer. HBT and BJT share the same principle of operation. Figure 4.1 shows the biasing of an HBT and the electron flow in the device. In an n-p-n HBT, two n-p junctions are joined together

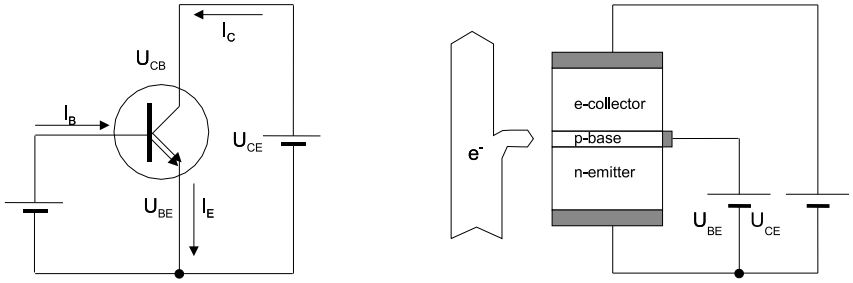

Figure 4.1: HBT biasing (left) and electron flow (right)

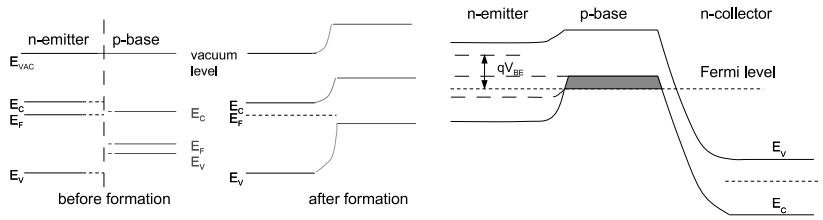

Figure 4.2: left: HBT base/emitter diode junction band structure before and after formation; right: band structure of n-p-n HBT

in opposite direction. Electrons are injected from the emitter into the base, passing through a thin base layer to the positive-biased collector. A small part of the emitted electrons are flowing to the base. The proportion of collector to base current is called current amplification. HBTs exist also as p-n-p devices with holes as current carriers. Due to the higher mobility of electrons (n-type) compared to holes (p-type), the maximum operating frequency of n-p-n HBTs is higher. P-n-p HBTs remain however interesting for the design of efficient complementary amplifiers as demonstrated by Sawdai [2] et al..

For the emitter, a wide bandgap material with a high conduction band energy (AlGaAs, InGaP or InP) is employed to facilitate electron injection into the base and to minimise the back-injection of holes which would lead to a recombination current

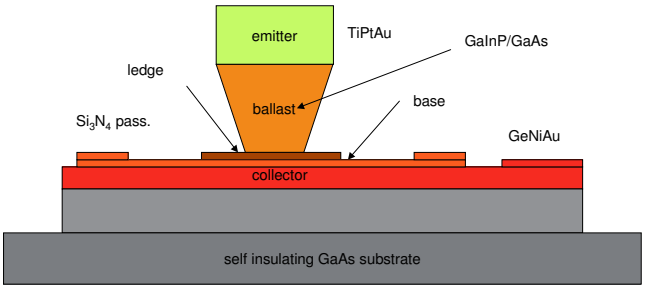

Figure 4.3: schematic of the HBT device structure

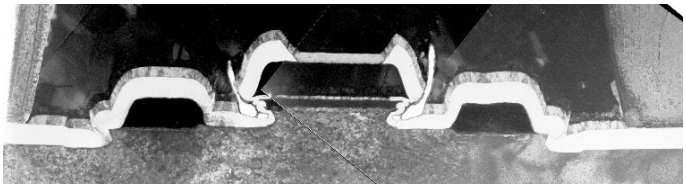

Figure 4.4: SEM cross-section of a virgin AlGaAs HBT emitter finger (without air bridge)

and lower the device efficiency [3]. The base consists of a very thin layer of heavily p-doped material of narrow bandgap width as GaAs or InGaAs. Figure 4.2 shows on the left the electronic band structure of the emitter/base n-p heterojunction before and after formation. The conduction band energy level of the collector is lower than for the emitter to facilitate the absorption of electrons from the base as it can be seen on the right on the same figure. Many materials from the III/V or the II/VI group can be used for heterojunction devices. Common are GaAs/AlGaAs/InGaP for GaAs based devices and Si/Ge for silicon based HBTs. Although Si/Ge HBTs operate at lower frequencies compared GaAs devices, there is a cost advantage as the processing of Si/Ge is compatible with standard manufacturing processes for silicon components.

The conducting channel of MESFETs and HEMTs is horizontal, the HBT has a vertical structure. Figure 4.3 shows the schematic setup and figure 4.4 a SEM cross-section of an HBT emitter structure or "finger". Four emitter fingers are connected in parallel to increase the current handling capacity. The ledge is a thin layer of weakly doped n-type material between base and emitter. The ledge inhibits recombination currents at the edges of the base junction which reduce the current

amplification. HBTs with AlGaAs and InGaP ledges will be tested. The base is heavily doped with carbon which is nearly immobile in GaAs. The small atom size compared to the GaAs crystal lattice allows high doping levels without introducing too much strain to the base. The layer structure of the HBTs can be looked up in table 4.1.

layer	**material**	**grading**	**thickness (nm)**	**doping level**	**type**	**function**
1	$In_yGa_{1-y}As$	y = 0.5	60	$3*10^{19}$	n	emitter contact
2	$In_yGa_{1-y}As$	y = 0 to 0.5	40	$3*10^{19}$	n	emitter contact
3	GaAs		50	$5*10^{18}$	n	emitter
4	$In_xGa_{1-x}P$ /$Al_xGa_{1-x}As$	x = 0.5	30	$1*10^{18}$	n	etch stop
5	GaAs		20	$3*10^{17}$	n	ledge
6	$In_xGa_{1-x}P$ /$Al_xGa_{1-x}As$	x = 0.5	40	$3*10^{17}$	n	ledge
7	GaAs		100	$4*10^{19}$	p	base
8	GaAs		1000	$2*10^{16}$	n	collector
9	GaAs		700	$5*10^{18}$	n	collector contact

Table 4.1: InGaP/AlGaAs HBT layer structure (from top)

On the table we see that the base/emitter junction is graded. Employing a graded base/emitter junction lowers the device turn-on voltage by about 150 mV compared to an abrupt junction. The mechanical length of one emitter finger is 25 μm and the width 7 μm. The effective electrical emitter length is 17 μm and width 3 μm resulting in an emitter surface of 204 μm^2 for a four-finger HBT. The electrical rating of the HBT structures are summarised in table 4.2. The power dissipation

parameter	**min. value**	**typ. value**	**max. value**
$\mathbf{U_{CE}}$		6 V	15 V at $I_C = 0$
$\mathbf{I_C}$		60 mA	125 mA
current density		30 Ka/cm^2	60 Ka/cm^2
beta	50	100	150
$\mathbf{P_{diss}}$		360	720 mW
$\mathbf{T_{amb}(P_{diss} = 0)}$			175 °C

Table 4.2: HBT electrical characteristics

of the HBT is substantially higher than for the MESFET (chapter 2) and pHEMT

devices (chapter 3). Under normal operating conditions (forward active mode), the main part of the power dissipation takes place in the base/collector junction of the device which is a few nanometers thin. The HBTs are packaged in ceramic housings which allow a power dissipation of 2 W while keeping physical dimensions small. The thermal house-holding is critical due to the vertical device structure (figure 4.3). The heat is conducted via the substrate and via the emitter electrode to the environment. The heat conduction path via the substrate is not very efficient as its thermal resistance is rather high. Mechanical thinning of the substrate improves the thermal conductivity but makes the device brittle. For the devices under test, a heat conduction path via the emitter is provided via a thick emitter air bridge as shown in figure 4.5. Figure 4.6 shows on the left a packaged component and on the

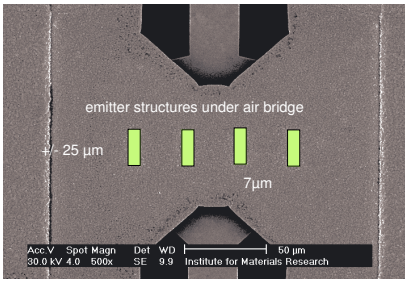

Figure 4.5: HBT emitters under thick air bridge acting as electrical contact and thermal heat sink

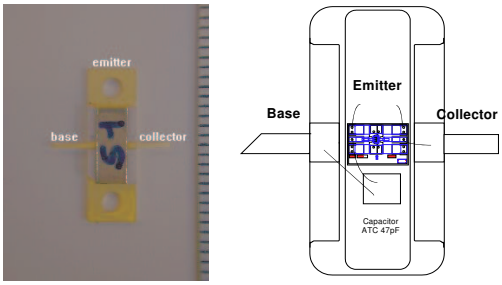

Figure 4.6: HBT in BmH60 ceramic package and schematic of the position of the die

right the position of the die in the package. For life testing a capacitor is applied between base to emitter to prevent oscillations.

4.3 Adaptations to the test system

4.3.1 Extension to multi sample capability

In the in-situ test system, each device has its own dedicated power supply as introduced in the last chapter. Now the system is extended to allow the simultaneous measurement of up to 20 devices. Due to cost constraints, the voltage and current meters are multiplexed to the DUT. The multiplexing imposes some minor restrictions on the measurement timing as only one device can be measured at a time. This drawback is a minor trade-off compared to the increased amount of information which can be obtained in the same time. Figure 4.7 shows the multiplexing

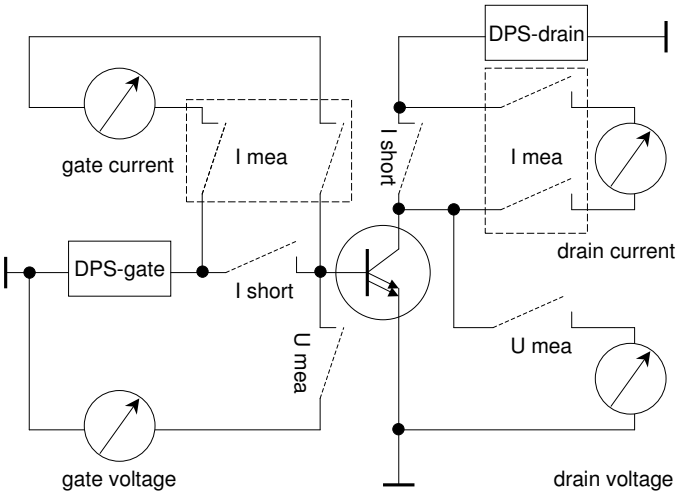

Figure 4.7: multiplexing of voltage and current meters to the DUT shown for one device

circuitry for one DUT. The setup includes two current and two voltage meters. The multiplexing of the current meters is critical as the current path to the DUT must never be open to avoid undefined potentials. Current meters must be shorted when not connected. In the multiplexing circuit, relays are provided to short the gate and drain current meters. These relays are normally closed during multiplexing and current range changes to avoid transient voltage spikes. Source current meters with electrometer input are employed. The electrometer input allows the elimina-

tion of the burden voltage. The multiplexing of the voltage meters is uncritical. The voltage meters are connected parallel to the base and the collector of the DUT so no current path must be opened. Due to the very large input resistance of the voltage meters, the current burden on the DUT can be neglected. The base and collector voltage is measured directly at the DUT to eliminate the voltage drop over the wiring and the series resistance of the sample fixture.

4.3.2 Approximation of current sources with voltage supplies

The in-situ measurement system provides permanently connected voltage sources for biasing. This approach has been chosen to avoid any need for multiplexing voltage/current sources as it was necessary for the MESFET tests with the first in-situ setup as presented in chapter 2. For the regulation of the collector current during the life test we want to use a similar approach as explained in chapter 2 in figure 2.13. As the HBT is a current-controlled device, a current source would be ideally suited for proper biasing of the base. If we connect the gate voltage supply of the in-situ test bench directly to the HBT base, the following effects will occur.

- At room temperature, the base voltage varies between 1.3... 1.6 V for the desired collector current range. The base current is increasing exponentially with the base voltage following equation 4.8. Further, the base voltage is decreasing with temperature as can be seen on figure 4.12 in section 4.5. A temperature increase -as during the warming-up of the furnace- will lead to increased base and collector currents and a probable destruction of the device under test.

- The digital power supplies deliver voltages in equidistant steps. The voltage step size is determined by the 20-bit DA converter and a scaling resistor which sets the voltage output range. The exponential base current increase following equation 4.8 leads then to increasing base current steps. As a result, the characteristics of the constant current loop (see figure 2.13 in chapter 2) will be highly non-linear. These difficulties can be avoided by linearising the current output of the voltage supplies with help of a series resistor. The series resistance has to be chosen depending on the type of device and the current range.

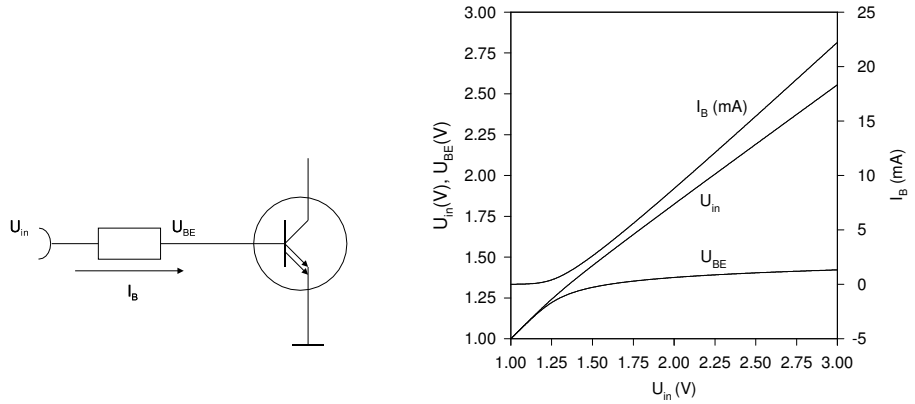

Figure 4.8: approximation of current sources by voltage sources with series resistance

For the accelerated testing and electrical characterisation of HBTs, we need a range of base currents to obtain collector currents between 1 % to 100 % of the maximum ratings. In the test setup for HBTs, a resistor value of 75 Ω converts a DPS output voltage range of 0 to 2 V to a base input currents ranging from 0 to 7.5 mA at room temperature. The effect of the linearisation can be seen in figure 4.8. For base voltages < 1.3 V the base current is very small. The base current is following the base input voltage nearly linearly for input voltages > 1.3 V. The base/emitter voltage, which is also measured in the test setup, U_{BE} is increasing proportionally to the logarithm of the due to equation 4.9. In the test setup, base and collector current are limited by the compliance limits of the current meters. The collector current compliance limit is set to the maximum measured current plus 20 % of headroom for the constant current regulation algorithm.

4.3.3 Approximation of constant power dissipation condition

The measurement system provides measurement of the device under test in constant collector or constant emitter current mode. The dissipated power should be constant during stress to keep the device temperature stable during life testing. In order to approximate the constant power condition, we consider the robustness of the power

dissipation with respect to the collector and emitter current. The emitter current is composed of the base and the collector current (figure 4.1):

$$I_E = I_C + I_B \tag{4.1}$$

with:

I_B	:	base current
I_E	:	emitter current
I_C	:	collector current

The current stress condition is defined in terms of the emitter current density, thus the emitter current must be stabilised. Regarding the junction temperature, the dissipated power should be kept constant. As the current amplification is expected to degrade during life test, this is contradictory with the first demand. In the following paragraphs it is shown that a good compromise is reached when the collector current is stabilised. The relative error on the emitter current however is small enough to be tolerated.
The collector current amplification factor β is defined as the ratio of collector current to the base current:

$$\beta = \frac{I_C}{I_B} \tag{4.2}$$

The ratio of the collector current and the emitter current is expressed in an analog manner:

$$\alpha = \frac{I_C}{I_E} \tag{4.3}$$

The current amplification factors depend from each other as defined by equation 4.1:

$$\frac{\beta}{\beta + 1} = \alpha \tag{4.4}$$

For virgin HBTs at room temperature, β is typically between 40 and 120 so α is slightly less than unity and we can approximate:

$$I_C \simeq I_E \tag{4.5}$$

For highly degraded devices, the emitter current may be substantially higher than the collector current and this approximation may not be accurate enough. This will

be discussed later at the end of this section. The current amplification factors α and β are supposed to degrade during the ageing experiment:

$$\alpha(t) < \alpha(t_0) \tag{4.6}$$

At constant collector current, the base current increases following:

$$I_B(t) = I_B(t_0)\ \frac{\alpha(t_0)}{\alpha(t)} \tag{4.7}$$

Following the Ebers-Moll model [4], the forward current through the base diode of a bipolar transistor is described as:

$$I_B = I_s \exp\left(\frac{U_{BE}}{n_{ideal}\ k_e T}\right) \tag{4.8}$$

with:

I_S	:	quiescent current of the base diode
k_e	:	Boltzmann's constant divided by electron charge
T	:	absolute temperature (K)
n_{ideal}	:	ideality factor
U_{BE}	:	base/emitter voltage

This model contains and "ideality factor" n_{ideal} which is typically between 1 and 3. The reason for the presence of this ideality factor will be discussed later. We are here interested in the dependence of the base/emitter voltage from the input current which is logarithmic:

$$U_{BE} = \ln\left(\frac{I_B}{I_S}\right) n_{ideal}\ k_e T \tag{4.9}$$

In first-order approximation it can be considered as constant as it is only slowly increasing. The electron-current induced power dissipation P_{diss}in a bipolar transistor can be written as:

$$P_{diss} = U_{BE} I_E + U_{CE} I_C \tag{4.10}$$

with:

U_{CE}	:	collector emitter voltage

With decreasing α and at constant emitter current the power dissipation in the device becomes time-dependent as the second term contains the current amplification factor α which decreases with time:

$$P_{diss}(t, I_E = const.) = U_{BE}I_E + U_{CE}I_E\alpha(t) \tag{4.11}$$

with:
t : time

For constant collector current, the power dissipation during test looks like:

$$P_{diss}(t, I_C = const.) = U_{BE}\frac{1}{\alpha(t)I_C} + U_{CE}I_C \tag{4.12}$$

In this case, the base current varies with the inverse of α. As α is slightly less than unity, we can write:

$$\alpha = 1 - \varepsilon \tag{4.13}$$

and:

$$1/\alpha = 1 + \varepsilon \tag{4.14}$$

with:
ε : small positive number

For small variations of ε, the relative variation of the base current is thus of the same magnitude as for α but of opposite sign. Under standard conditions of operation, the contribution of the collector current to the dissipated power is much higher compared to the contribution from the current through the base/emitter diode (second term of equation 4.1):

$$U_{CE}I_C \gg U_{BE}I_B \tag{4.15}$$

The power dissipation and therefore the internal heat generation at constant collector current depends much less dependent on the device ageing than for constant emitter current. Given the following parameters U_{CE} = 8V; U_{BE} = 1.4 V; I_E or I_C = 125 mA; $\beta(t_0) = 100$; $\beta(t_{end}) = 10$, the power dissipation change for a beta degradation from 100 to 10 (-90 %) is shown on table 4.3. The values shown on this

property	$\mathbf{P_{diss}(t_0)}$	$\mathbf{P_{diss}(t_{end})}$	ΔP_{diss}	ΔI_E	ΔI_C
$\mathbf{I_C = 125mA}$	1001.75 mW	1017.5 mW	+1.6 %	+8.911 %	±0 %
$\mathbf{I_E = 125mA}$	991.83 mW	925.02 mW	−6.7 %	±0 %	−8.914 %

Table 4.3: power dissipation change during ageing for constant collector and for constant emitter current

table are calculated using equation 4.12 for the case of constant collector current and 4.11 for the constant emitter current case. As can be seen, the power dissipation change is +1.6 % for the constant I_C method compared to -6.7 % for the constant I_E method. The stabilisation of the collector current is therefore better suited to keep the device temperature constant than the stabilisation of the emitter current. The device degradation depends not only on the temperature, but also on the current density. During the ageing of the device, the current amplification normally degrades. The base current must then be increased to compensate the degradation of the current amplification. The increased emitter current may lead to an accelerated ageing of the base/emitter diode. As this current increase is a second-order effect, its influence on the device degradation characteristics is rather small.

4.4 HBT characteristics

4.4.1 HBT electrical characteristics

Rearranging equation 4.8 for the base current ideality factor n_{ideal} yields:

$$n_{ideal} = \frac{\mathrm{d}((U_{BE}))}{\mathrm{d}(\ln(I_B))} \frac{1}{k_e T} \tag{4.16}$$

In this simple model, the current amplification factor β and the ideality factor n_{ideal} are constant. For real devices, different carrier generation/recombination processes are stimulated with varying bias changing both parameters. An more elaborate model accounting for these dependencies has been established by Gummel and Poon in 1970 [5]. The HBT is characterised by Gummel plots which show the dependence

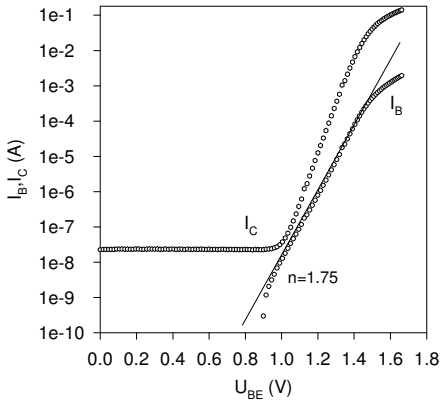

Figure 4.9: Gummel plot of AlGaAs HBT

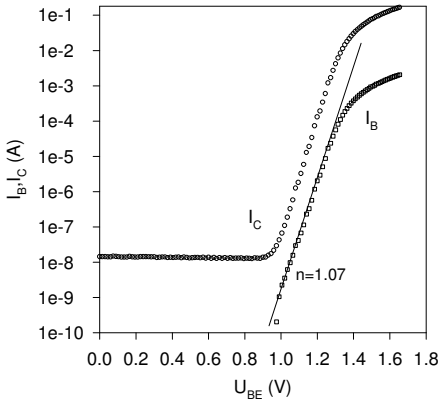

Figure 4.10: Gummel plot of InGaP HBT

of the collector and base currents from the applied base and collector voltages. Figures 4.9 and 4.10 show Gummel plots for an AlGaAs and an InGaP HBT at room temperature. For $U_{BE} < 1$ V, the base current is negative due to a residual leakage current path from the collector to the base. The equivalent leakage resistance is higher than 40 MΩ. For $U_{BE} > 1$ V, the contribution of the collector leakage current becomes negligible compared with the amplified base current. Comparing the Gummel plots of the AlGaAs and InGaP HBT, we see that the AlGaAs device

has a higher base current ideality factor than the InGaP HBT. The ideality factor n_{ideal} should optimally be close to 1. Due to carrier recombination in the base, the base ideality factor is always higher. For base voltages from 1.0 to 1.2 V we get an ideality factor $n_{ideal} = 1.75$ for AlGaAs HBT and $n_{ideal} = 1.07$ for InGaP HBTs. The higher ideality factor for AlGaAs HBTs is an indication for the increased amount of recombination current (n = 2). The base recombination current is related to edge recombination along the emitter ledge. The higher recombination current for the AlGaAs HBTs can be explained by the higher hole energy barrier of 0.43 eV for InGaP compared to 0.25 eV for AlGaAs [6]. The collector current is a pure injection current. The ideality factor for the collector current is close to 1 for both AlGaAs and InGaP devices. The electrical characteristics of a heterojunction bipolar transistor depend on the device junction temperature. Figure 4.11 shows the collector current characteristics of a low-power HBT in function of the collector voltage at constant base voltage. The device is operated in forward active mode with

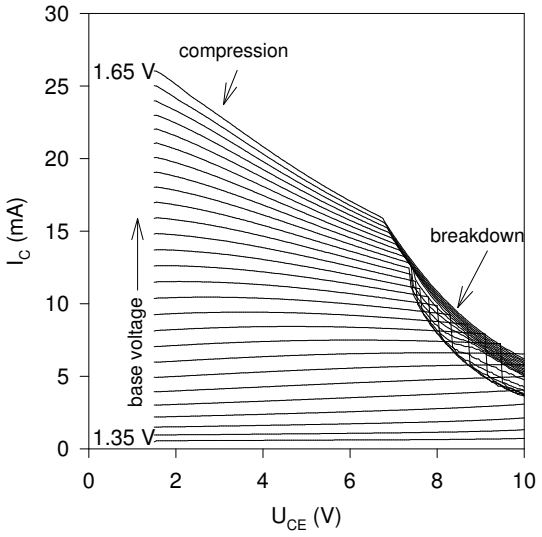

Figure 4.11: $I_C(U_{CE})$ characteristics of a single-finger low-power HBT exhibiting thermal compression and thermal breakdown (current crunch)

$U_{CE} > 1.5$ V. With increasing collector voltage, the dissipated power is increased and the junction temperature rises. At low base voltages, the collector current is nearly independent of the collector voltage. As the base voltage is increased, the collector current shows a significant decrease with increasing collector voltage. This effect is caused by the increased Joule heating of the device and is known as *"thermal compression"*. The thermal compression leads to a decrease of the current amplification of the HBT. When the collector voltage is further increased, the collector current collapses due to *current crowding* : The heat is conducted to the environment via the emitter fingers and the substrate of the device. The temperature in the center of the emitter is higher. The base-emitter voltage in the center is lowered. This leads to a higher base and collector current in the center further increasing the temperature. This effect may be counteracted by a second effect, namely the decrease of the current amplification with temperature. If the second effect is not strong enough, the thermal runaway may lead to catastrophic device failure or device *"burn-out"*.

4.5 Determination of the HBT thermal resistance and junction temperature

The temperature is an important parameter for HBT performance and reliability and the knowledge of the junction temperature is crucial for life testing. The device temperature is important to determine the device ageing and reliability. In the second chapter where MESFETs have been investigated, data on the channel temperature were available from the manufacturer. For the pHEMT devices, self heating could be neglected as the power dissipation was small. For the HBT, data on the thermal resistance were not available as the technology was very recent. As the devices under test were defined for power applications, significant device self heating was to be expected. Based on procedures for thermal resistance measurement of GaAs HBTs as described by Waltrop [7], Dawson [8] and Fuller [9], a refined method has been developed which will be presented in this chapter.

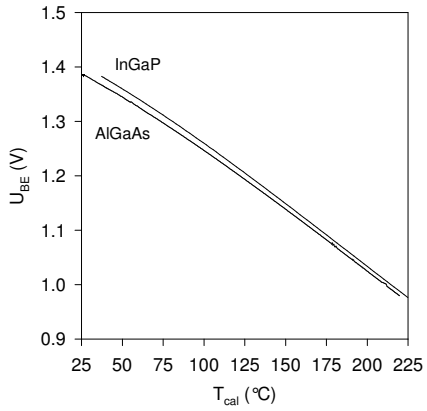

Figure 4.12: $U_{BE}(T)$ at constant I_B = 100 μA for AlGaAs and InGaP HBT

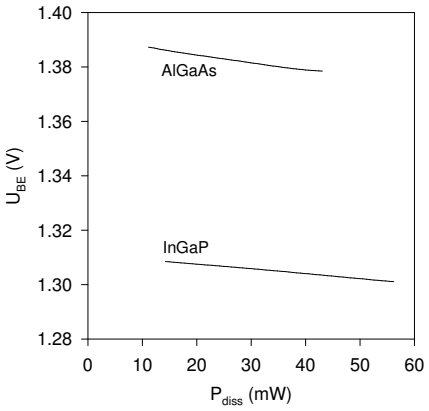

Figure 4.13: $U_{BE}(P)$ for AlGaAs and InGaP HBT at I_B = 100 μA

As the thermal resistance of gallium arsenide is increasing with temperature [10], it can be expected that the thermal resistance of GaAs devices depends also on ambient temperature and dissipated power. Electrical methods for thermal resistance measurement exploit the temperature dependence of a intrinsic electronic device parameter. The base-emitter forward voltage U_{BE} at constant base current

has a highly linear temperature dependence over the measured range of junction temperatures and serves as such a parameter throughout this chapter. Figure 4.12 shows the U_{BE} temperature dependence for AlGaAs and InGaP HBT at 100 μA base current. Above 100 °C, U_{BE} decreases linearly with a slope of -2.18 mV/K for InGaP and -2.1 mV/K for AlGaAs HBTs, the exact values being device dependent. This step serves as temperature calibration. The collector voltage is set to U_{CE} = 2 V. The device is biased in saturation mode, but the dissipated power is still low to minimise self-heating. For now, the temperature increase due to the dissipated power is neglected. Later on, we will correct for this.

Increasing the collector voltage leads to an increase of the dissipated power. The device heats up and the base voltage is decreasing. As result we get the dependence of the base voltage from the dissipated power as shown on figure 4.13 for InGaP and AlGaAs HBTs. With the data from the temperature and power calibration, we can determine the thermal resistance. The maximum obtainable power at low base current is limited. For the power calibration, a high base current would be advantageous but the temperature offset during temperature calibration could not be neglected anymore.

We now present a refinement which allows the determination of the self-heating during temperature calibration. Once this self-heating is known, the real device junction temperature can be determined. In order to achieve this, we make use of an extrapolation technique which consists of six steps:

1. measurement of the temperature calibration
2. measurement of the power calibration curves
3. obtaining $T_{cal}(P_{diss})$ by looking up the calibration temperature values for the power calibration from the temperature calibration data
4. extrapolating from $T(P_{diss} = P_{cal})$ to $T_{cal}(P_{diss} = 0)$ which yields an extrapolated ambient temperature T_{ext}
5. calculating the temperature offset between the extrapolated T_{ext} and the real ambient temperature T_{amb}
6. applying this temperature offset to $T_{cal}(P_{diss})$ to obtain $T_{jct}(P_{diss})$

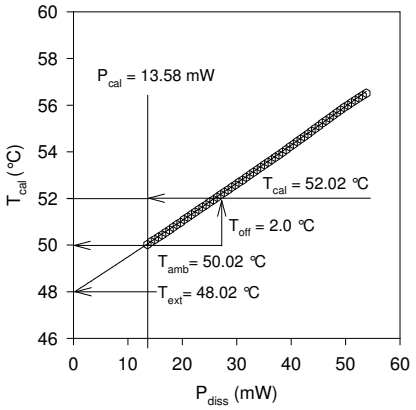

Figure 4.14: $T_{cal}(P_{diss})$ at T_{amb} = 50.02 °C for InGaP HBT

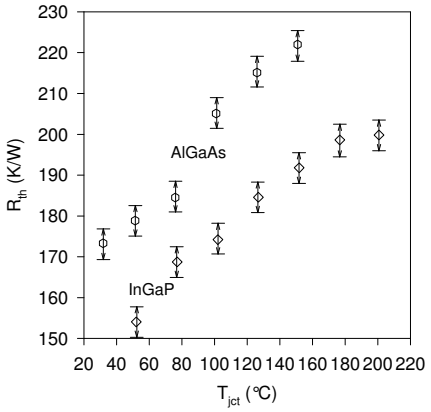

Figure 4.15: $R_{th}(T_{cal})$ of AlGaAs and InGaP HBT; P_{diss} = 20 mW

Figure 4.14 shows the power calibration data of an InGaP HBT at T_{amb} = 50.02 °C. The extrapolation of the junction temperature to zero dissipated power yields a virtual junction (=ambient) temperature of 48.02 °C. We know that at zero dissipated power the junction temperature must be equal to the ambient temperature which is equal to 50.02 °C. We have therefore a junction temperature offset during calibration of 2.0 °C. The difference between extrapolated and measured calibration temperature must be equal to the temperature offset due to self-heating:

$$T_{off} = T_{amb} - T_{ext} \tag{4.17}$$

with:

T_{off} : temperature offset

T_{ext} : extrapolated temperature for zero power dissipation

Now we can calculate the junction temperature:

$$T_{jct} = T_{cal} + T_{off} \tag{4.18}$$

Adding the temperature offset to the calibration temperature yields the junction temperature as shown in figure 4.14.

The thermal resistance has been calculated being 155.3 K/W ±1.5 K/W at a reference power of 20 mW. The power calibration is repeated over a range of ambient temperatures from 25... 150 °C. Calculating the thermal resistance for all ambient temperatures for the same reference power of 20 mW, we obtain the temperature dependence of the thermal resistance for AlGaAs and InGaP device technology as shown on figure 4.15. The junction temperature for any given dissipated power and ambient temperature can now be calculated. Due to the increase of the thermal resistance of gallium arsenide with temperature [10], a rise of the junction temperature due to the internal power dissipation leads to a rise in thermal resistance which induces a further (smaller) rise in junction temperature until the temperature is stable. Calculating the junction temperature using equation 2.3 of chapter 2, leads to a systematic under-estimation of the junction temperature. To correct this, we must include the thermal resistance temperature dependence:

$$T_{jct} = T_{amb} + R_{thja}(T)P_{diss} \tag{4.19}$$

with:

R_{thja} : thermal resistance junction to ambient

The dissipated power is calculated as follows:

$$P_{diss} = U_{CE}I_C + U_{BE}I_B \tag{4.20}$$

with:

U_{BE} : base/emitter voltage
I_B : base current
U_{CE} : collector/emitter voltage
I_C : collector current

The temperature dependence of the thermal resistance GaAs can be described as [10]:

$$R_{th}(T) = R_{th}(T_0)\left(\frac{T}{T_0}\right)^k \tag{4.21}$$

Equations of this form must be solved by iteration for a given ambient temperature and dissipated power. The thermal resistance at T_0 and the thermal resistance

exponent k must be determined by measurement. The iterative algorithm is based on the extrapolation of the measured thermal resistance data as in figure 4.15. The iteration starts with $R_{th}(T_0 = T_{amb})$, calculating the temperature T_1:

$$T_1 = T_0 + P_{diss} R_{th}(T_0) \tag{4.22}$$

As the thermal resistance increases with the device temperature, the application of $R_{th}(T_0)$ leads to an under-estimation of the junction temperature. The next iteration step leads to a first-order correction accounting for the thermal resistance increase:

$$T_i = T_{i-1} + P_{diss} R_{th}\,(T_{i-1}) \tag{4.23}$$

The iteration is then repeated. The corrections becomes smaller with each iteration step. When the difference between subsequent iterations becomes smaller than ε, the solution is regarded to be stable:

$$T_i = T_{i-1} + \varepsilon \tag{4.24}$$

with:

i	:	iterator
T_0	:	initial temperature
T_1	:	temperature at first iteration step
T_{i-1}	:	temperature at iteration step i-1
T_i	:	temperature at iteration step i
k	:	thermal resistance exponent
ε	:	small positive number, e.g. 10^{-6}

For bulk gallium arsenide, the thermal resistance exponent k is 5/4 or 1.25. This value is based on theoretical considerations [10] and has been experimentally verified for homogeneously heated bulk GaAs material in the temperature range between 300 and 900 K. For packaged electronic devices like HBTs, the measured thermal resistance exponent may differ from the theoretical value. The heat distribution inside a real device is highly inhomogeneous and the heat is passed to the environment through layers of different materials, each contributing to the thermal resistance. The value of the thermal resistance exponent for the packaged device is approximated by a numerical fitting procedure.

	AlGaAs		**InGaP**	
$\mathbf{P_{diss}(mW)}$	$\mathbf{T_{jct}}$ **uncorrected**	$\mathbf{T_{jct}}$ **corrected**	$\mathbf{T_{jct}}$ **uncorrected**	$\mathbf{T_{jct}}$ **corrected**
50	109.7	110.0	108.3	108.5
100	119.4	120.8	116.5	117.3
250	148.6	157.0	141.3	146.3
500	197.2	232.5	182.5	202.5

Table 4.4: junction temperatures for AlGaAs and InGaP HBTs corrected for thermal resistance increase

Table 4.4 shows the iteration results for the junction temperature following equation 4.23 for AlGaAs and InGaP technology. The uncorrected junction temperature values are first order approximations as calculated using equation 4.22. The corrected values are solutions of equation 4.23. The increase of the thermal resistance due to thermal feedback is most significant under high power conditions. The presented approach neglects the effects of in-homogeneous current distribution inside the device. Under standard operating conditions however there is good correlation of this electrical method with results from three-dimensional thermal device modelling making use of finite element methods [11].

4.6 Determination of the current acceleration exponent

For the modelling of the HBT ageing kinetics, an extended Arrhenius-model is used to take account for current and temperature related contributions to device ageing. During life tests on laser diodes an exponential current dependency of the ageing characteristics has been observed [12],[13] and has empirically been described by an Arrhenius-type law extended by an exponential term to include current induced degradation:

$$A_F = \left(\frac{j_2}{j_1}\right)^n \exp\left(\left(\frac{E_a}{k_B}\right)\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \tag{4.25}$$

with:

A_F	:	acceleration factor
j_1, j_2	:	current densities
n	:	current density exponent
T_1, T_2	:	temperatures
k_B	:	Boltzmann's constant

The introduction of the current exponent n is motivated by observations on laser diodes and is in the range between 1 and 2. Its exact value depends on the current density and state of degradation of the device. However, laser diodes have a different topology and are operating at higher current densities than HBTs. For the analysis of life test results, the determination of the current acceleration exponent is of crucial importance. For the separation of current and temperature induced device degradation, the device degradation must be measured dependent on the collector current while keeping the device at a constant junction temperature. This can be achieved by adapting the collector voltage appropriately as shown in table 4.5 which

collector voltage	**collector current**
8 V	60 mA
6 V	80 mA
5 V	96 mA
4 V	120 mA

Table 4.5: isopower measurement states for $P_{diss} = 480$ mW

shows the calculated collector voltage and collector current levels. The dissipated power for these measurement states at the collector side is constant at $P_{diss} = 480$ mW, therefore we call those states "isopower" states. The contribution of the base current is neglected here as it is rather small. For the isopower states, the junction temperature is constant. The temperature dependence of the device degradation is eliminated and so the need for determining the activation energy E_a. The current is left as single variable stress factor and equation 4.25 then simplifies as follows delivering the current stress acceleration factor A_C:

$$A_C = \left(\frac{j_1}{j_2}\right)^n \Rightarrow n = \frac{\log(A_F)}{\log(j_1) - \log(j_2)} \tag{4.26}$$

In order to determine the current acceleration factor, the device is set under constant collector current stress until the onset of final beta degradation (phase 4 in figure 4.22) is observed. Then the collector current of the HBT device is switched from collector current I_{C1} to I_{C2} which corresponds to current density j_1 respectively current density $j_2 > j_1$. The collector voltage U_{CE} is simultaneously adapted to keep P_{diss} constant. Due to the increased current density, the degradation is accelerated. After sufficient time, the slope of the degradation curve at high current is determined. Then the collector current density is switched back to j_1 with U_{CE} adjusted accordingly. In the following paragraphs, the determination of the current density exponent is performed using three independent methods.

4.6.1 The "in-situ" approach

The comparison of the degradation slopes at collector current densities j_1, j_2 yields the current acceleration "in-situ". For the application of this method, the slope of the degradation curves has ideally to be determined at the exact transition time t* between the two stress conditions. Figure 4.16 shows the slopes at the two current

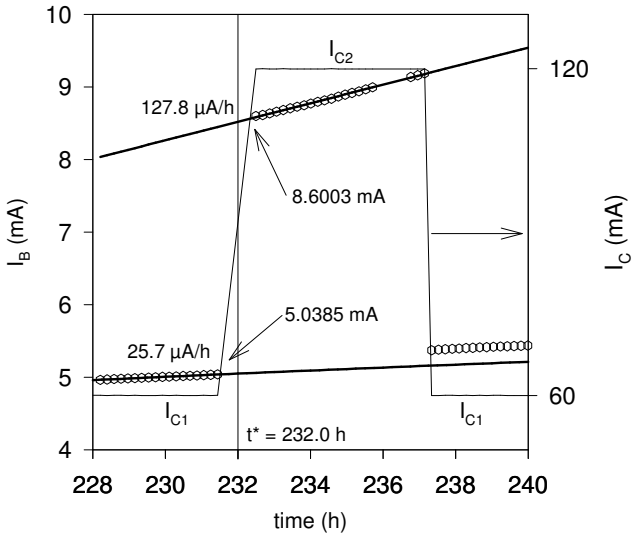

Figure 4.16: determination of the current exponent using the in-situ approach

stress conditions to illustrate the analysis procedure in more detail. The slope at low current level is determined by fitting the data at the left side of the transition point; the slope at high current level is determined by approaching the transition point t* from the right side. The absolute slope of the degradation of the base current with time is then defined as:

$$D_{abs}(t^*) = \left(\frac{dI_B(t^*, I_C)}{dt} \right) \Bigg|_{t^*, I_C} \tag{4.27}$$

with:

D_{abs} : slope of absolute base current degradation

As the degradation at the two different current levels is compared, the slopes must be re-scaled to the relative parameter change D_{rel} as defined by:

$$D_{rel}(t^*, I_C) = \frac{1}{I_B}\frac{dI_B}{dt}\bigg|_{t^*, I_C} \tag{4.28}$$

The current acceleration factor is then defined by:

$$A_C = \frac{D_{rel}(t^*, I_{C2})}{D_{rel}(t^*, I_{C1})} \tag{4.29}$$

and subsequent substitution of 4.28 delivers:

$$A_C = \left(\frac{1}{I_B}\frac{dI_B}{dt}\right)\bigg|_{t^*, I_C 2} \left(\frac{1}{I_B}\frac{dI_B}{dt}\right)^{-1}\bigg|_{t^*, I_C 1} \tag{4.30}$$

The acceleration factor is determined using the data of figure 4.16. Applying equation 4.26 yields a current exponent of n = 1.54 which is within the range indicated for laser diodes [12].

4.6.2 The "off-line" evaluation

This method is called off-line-method because the current acceleration is measured without making use of the high current stress phase degradation data which were obtained at I_{C2}. All data needed for the determination of the current exponent refer to the same current I_{C1}, the need for re-scaling is therefore eliminated. For the off-line method, the same set of data has been used as for the in-situ approach in order to facilitate comparison of results. Before switching the collector current from 60 to 120 mA at $t_1 = 231.4$ h, the base current is measured as . At $t_2 = 237.3$ h the current is switched back to 60 mA. The current degradation observed before switching is extrapolated from t_1 to t_2. This step yields $I_{B,extr} = 5.1588$ mA. Due to the acceleration induced by the high current phase between t_1 and t_2 the measured current $I_B(t_2, I_{C1})$ is with 5.3715 mA significantly higher than $I_{B,extr}(t_2, I_{C1})$ which is extrapolated from the data before I_{C2} was applied (figure 4.17).

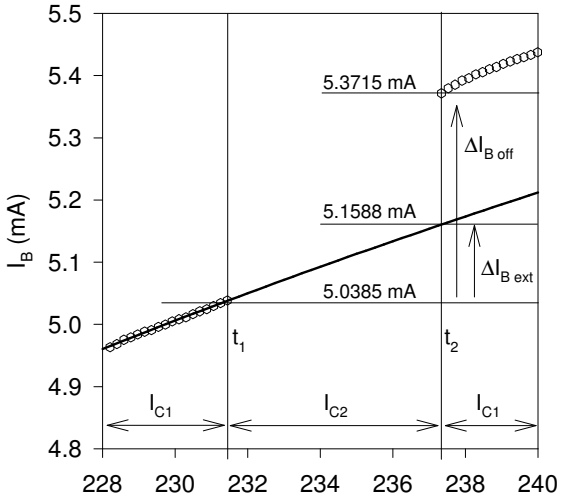

Figure 4.17: determination of the current exponent using the off-line approach

The current acceleration factor A_C can then be calculated:

$$A_C = \frac{\Delta I_{B,off}}{\Delta I_{B,extr}} = \frac{I_B(t_2, I_{C1}) - I_B(t_1, I_{C1})}{I_{B,extr}(t_2, I_{C1}) - I_B(t_1, I_{C1})} \tag{4.31}$$

Equation 4.31 yields a current acceleration factor A_C of 2.77. The current exponent is then calculated using equation 4.25 and the current densities from figure 4.16. The calculation yields a current exponent n = 1.47 which is in good agreement with the result of the "off-line" method where we obtained a current exponent of 1.54. The value for the current exponent for AlGaAs HBTs can therefore be given with $n = 1.5 \pm 0.1$ which is well in the range indicated in the literature for laser diodes ($1 \leq n \leq 2$) [12].

The in-situ approach inhibits an uncertainty as the degradation rates of two different current bias points are compared. This difficulty does not appear using the off-line approach but this approach relies critically on the choice of an appropriate extrapolation function.

4.6.3 The "control parameter" method

A third approach is applied for the measurement of the current acceleration on

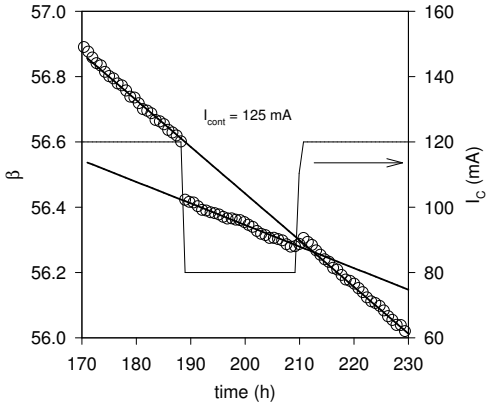

Figure 4.18: β(t) at control current level I_C = 125mA dependent on the stress current (InGaP HBT)

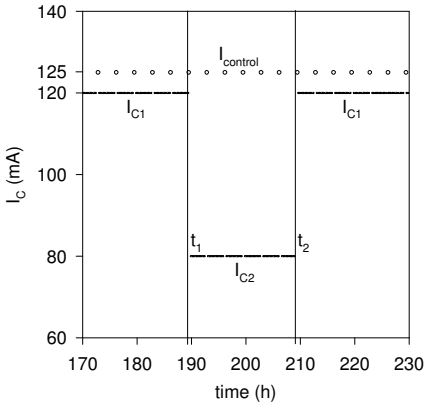

Figure 4.19: measurement timing for stress current (60 and 120 mA) and control current (125 mA) levels

InGaP devices. The ambient temperature is set to 120 °C and the junction temperature approaches 210 °C. The stress currents and the collector voltages are then changed according to table 4.5. Intermittently the device is measured at a predefined isopower measurement current level. The timing of these measurements is shown in figure 4.19. As a result, the degradation is defined by the stress current level but is measured at a constant measurement current level. This eliminates the need for re-scaling. The current acceleration is then determined from the ratio of the slopes of the degradation of the current amplification factor β:

$$A_C = \frac{d\beta(I_{C2})/dt}{d\beta(I_{C1})/dt} \tag{4.32}$$

The current exponent of the InGaP HBT has been determined as $n_{curr} = 1.85 \pm 0.07$ which is higher than for the AlGaAs devices but still within the range given by Ott [12] for laser diodes. Figure 4.18 shows the stress current level (solid line) and the beta degradation at I_C= 125 mA at measurement current level. The collector current must periodically be switched from the stress state to the measurement state.

Although the contribution of the collector current is the same for the isopower levels, there remains a small heat dissipation change due to the contribution of the base-emitter current. This dissipation changes lead to periodic temperature excursions. Figure 4.20 shows the scattering on the HBT case temperature. Due to the

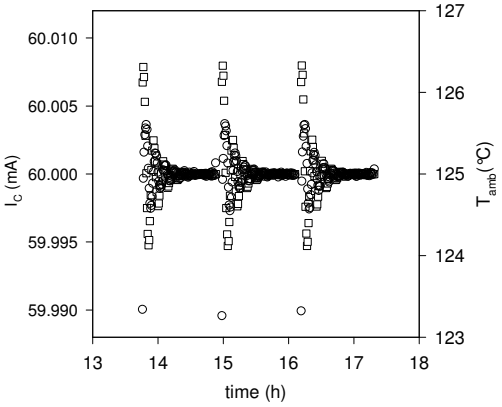

Figure 4.20: temperature (filled symbols) and current (open symbols) excursions

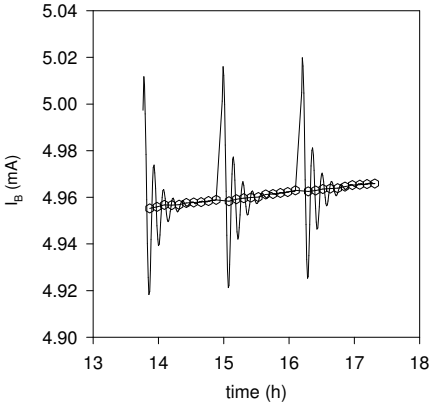

Figure 4.21: base current degradation data before and after LTSCA

temperature dependence of the current amplification, the temperature offset causes a collector current offset which is also shown on the figure. The temperature and current scattering is significantly reduced with help of the local temperature sensing and correction algorithm (LTSCA). The effect of the LTSCA is illustrated in figure 4.21 for the base-emitter current. We observe that the periodic perturbations are eliminated after LTSCA and that the base current is monotonously increasing due to the device degradation. The LTSCA technique has been introduced in paragraph 1.4.1.

4.7 Accelerated life tests on HBTs

4.7.1 Setup of experiment

After the thermal resistance of the HBT technology and the current exponent have been determined, we now take care of the influence of the junction temperature and technology on HBT reliability. Highly Accelerated Stress Tests (HASTs) on AlGaAs and InGaP HBTs on a time scale of 1000 hours will be discussed. As life testing has already been covered in the earlier chapters, so the discussion of the HBT results can be shorter.
Figure 4.22 shows a typical [14] degradation of the current amplification during accelerated life test. The ageing of a HBT can be divided in four phases. During

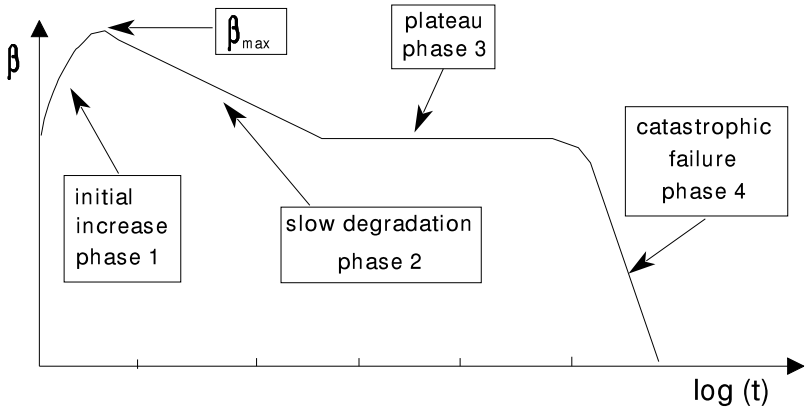

Figure 4.22: model of HBT degradation behaviour

the first hours of life test, an enhancement of the device characteristics takes place (phase 1) which can be attributed to the out-diffusion of hydrogen [15]. After this initial increase, the current amplification factor is decreasing (phase 2) to form a plateau (phase 3). This effect is often related to contamination of the device from out-diffusing of fluorine trapped inside the case during packaging. At the plateau level the device parameters remain stable until catastrophic failure occurs (phase 4). For reliability evaluation, the investigation of this final degradation phase is of main interest.

4.7.2 AlGaAs HBT failure behaviour

AlGaAs HBT are tested at a junction temperature of 205 °C for 1000 hours. The current density of 60 kA/cm^2 is the maximum allowed during operation and is equivalent to 122.4 mA collector current. The junction temperature has been determined using the method described in paragraph 4.5. The current amplification factor beta at constant collector current is continuously monitored. For safety reasons, the base current is limited to 30 mA. As the current amplification is then less than 5, the device is practically completely degraded.

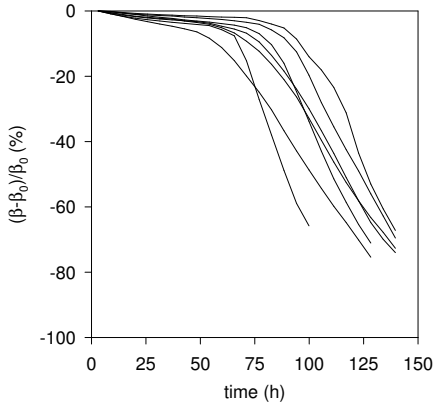

Figure 4.23: beta degradation of AlGaAs HBTs; I_C = 122.4 mA; T_{jct} = 205 °C

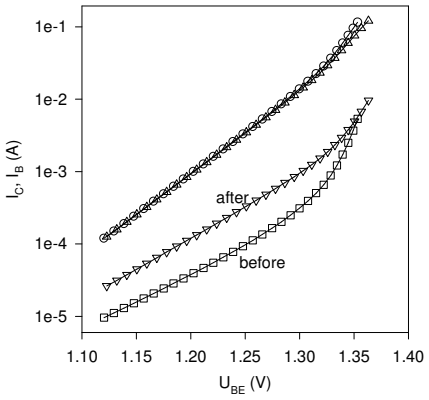

Figure 4.24: Gummel plot of AlGaAs HBT before and after ageing

Figure 4.23 shows the sample degradation at stress condition. Although beta is strongly reduced, the devices remain functional. The time to -20 % degradation is less than 110 hours. This is significantly lower than it has been expected following data from literature [1]. The HBTs degrade immediately without initial burn-in phase (phase 1). The plateau-phase (phase 2) is observed for half of the devices under test. The other samples enter immediately into catastrophic failure (phase 4). After ageing, a strong increase of the base current is observed as it can be seen on the Gummel plot in figure 4.24. The collector current characteristics remain unchanged. The increased base current can be traced to ledge recombination currents.

4.7.3 InGaP HBT failure behaviour

Due to their low reliability, the AlGaAs HBTs have been replaced by HBTs with InGaP ledges. The intrinsic defect density of InGaP is less than for AlGaAs so that there is less ledge recombination current. A substantially higher reliability of HBTs with InGaP ledges compared to HBTs with AlGaAs ledges is also reported by Low [6]. For life testing of InGaP HBTs, higher stress levels must be applied than for the AlGaAs devices to obtain device failures in reasonably short times.

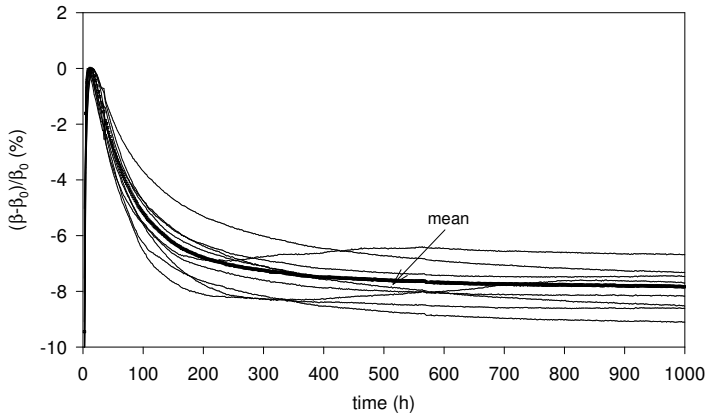

Figure 4.25: results of 1000 hour life test on InGaP devices T_{jct} = 225 °; I_C = 60 kA/cm^2

Figure 4.25 shows the degradation behaviour of InGaP HBT at a junction temperature of 225 °C and 60 kA/cm^2 current stress. In accordance with figure 4.22, all samples show a burn-in effect with initial enhancement of their characteristics (phase 0) with subsequent return close to their initial parameters (phase 1). No device failure was observed within the test time.

4.8 Extended life tests on InGaP HBTs

The life tests at moderate junction temperatures showed no device failure after 1000 hours test time. To explore the limits of the InGaP HBT technology within reasonable time, the stress level must be increased. The current density (60 kA/cm^2 or $I_C = 122.4$ mA) can not be increased without risking current crowding effects which lead to local hot spots in the device [16]. The ambient temperature is increased

T_{amb} °C	T_{jct} °C uncorrected	T_{jct} °C corrected
100	177.8	195.4
125	208.0	224.9
150	237.8	253.9
175	267.2	282.7
180	273.8	288.4
190	284.6	299.8
200	296.1	311.2
210	307.7	322.6
225	324.9	339.5

Table 4.6: junction temperatures for extended life test on InGaP HBTs

step-wise from 100 to 225 °C as shown in table 4.6. The junction temperatures are corrected for the thermal resistance increase as presented in paragraph 4.5. Up to 300 ° junction temperature, the device parameters remain stable without degradation. Above 311 °C we observe an increased ratio of collector to base current. This could be interpreted as an increased current amplification and thus an improvement of the device characteristics. A closer look on the following figure explains this observation which is somewhat contradictory as device degradation has been expected. Figure 4.27 shows the collector current at $U_{BE} = 0$ V. At this bias the transistor is normally turned off, so any collector current is due to leakage. At ambient temperatures higher than 190 °C ($T_{jct} = 300$°C), the collector leakage current increases to 810 μA at $T_{amb} = 225$ °C as shown in figure 4.27. This current contribution is too small to account for the virtual beta increase at stress current level as shown in figure 4.26. The leakage current depends strongly on the device temperature and therefore on the Joule heating. This Joule heating is significantly higher at stress current level than for $U_{BE} = 0$. At this condition, only leakage currents are present so the dissipated power is low and self-heating can be neglected. Additional to

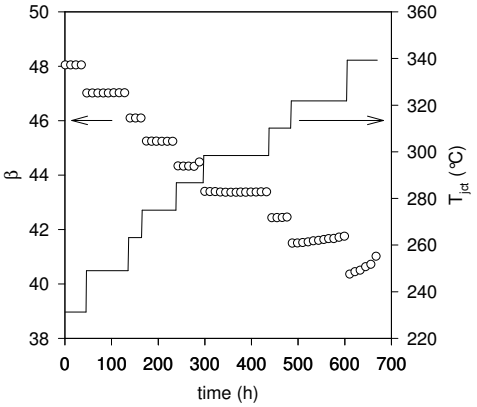

Figure 4.26: beta degradation of InGaP HBT at T_{jct} = 300...339°C

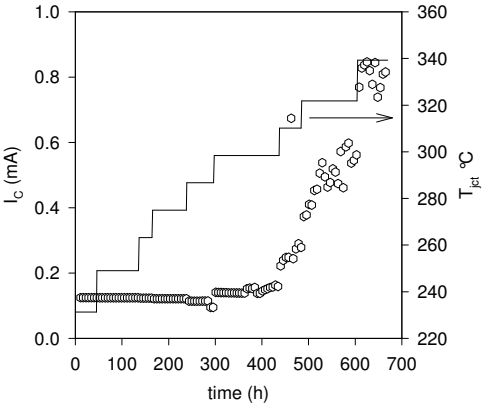

Figure 4.27: collector leakage current at U_{BE}= 0 V; same T_{jct} range

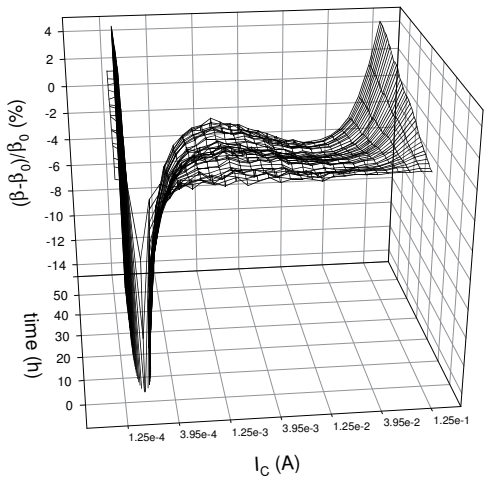

Figure 4.28: beta drift of InGaP HBT at T_{jct} = 311 ° C junction temperature at stress current level

monitoring the degradation at stress current level, the device output characteristics are measured in the collector current interval between 125 μA and 125 mA as indicated in figure 4.28. Interpreting the butterfly-shaped curve, we apply an analogue situation as in figures 4.26 and 4.27. At low collector currents we observe increasing leakage current (negative beta drift values). As the collector current increases, the junction temperature rises. The temperature dependence of reverse leakage currents is proportional to T^3 or even T^4 [17]. The relative contribution of the leakage current is thus significantly increased at high power dissipation. Life testing at highly

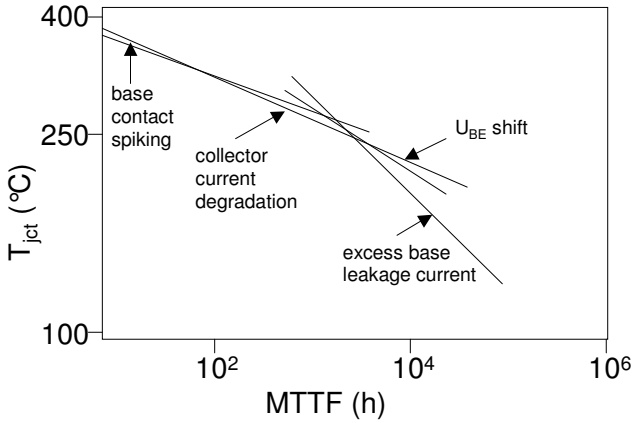

Figure 4.29: HBT damage mechanisms depending on temperature [18]

elevated junction temperatures remains critical: Different failure mechanisms may be activated compared to those reported at moderate temperatures as stated by Henderson et al. [18]: At the end of the high-temperature life testing at 340 °C junction temperature, the base of the DUT has suddenly been shorted. This is an evidence of base/emitter spiking which is a typical failure mechanism occurring at high temperatures as illustrated in figure 4.29. This kind of failure did not occur during testing at moderate junction temperatures (225 °C).

4.9 Conclusions for this chapter

In this chapter, the accent has been less on the performance of in-situ life tests than on the modeling of the device ageing behaviour. The accelerated life tests on the HBT technologies demonstrated the capability of the in-situ test bench to deliver valuable results in less time than needed for conventional tests. In the case of AlGaAs HBTs, the reliability figures allowed conclusive results within a test time of 100 to 200 hours. The electrical parameters of the InGaP devices remained practically unchanged after 1000 hours test time. The transition to higher test temperatures reduced the time to failure to reasonable limits. Due to this increased reliability, the physical limits of life testing have been reached for this device technology. This question is also a matter of device packaging. The tested HBTs were packaged in ceramic cases, but standard plastic packages can be tested only at moderate temperatures without decomposition. As the devices under test were designed for power applications, they had to be tested under high power dissipation. For the modeling of the device degradation, the determination of the junction temperature has been critical. For the HBTs, no thermal resistance data were available from the supplier as the technology itself was very recent. In the frame of this thesis, a refined method for the determination of the device thermal resistance has been developed. For the application of devices for power applications, the temperature dependence of the thermal resistance of the gallium arsenide base material becomes crucial. With the refined thermal resistance measurement method, this temperature and power dependence has been taken into account. Further, the separation of current and temperature driven device ageing has been performed. This has been necessary as data were not available for this device technology in literature. The availability of a freely programmable test system renders the most complex experiments easy to set up. The measurement capability has been extended and the inclusion of full parametric sweeps of the device characteristics promoted the understanding of the complex ageing characteristics of some HBT devices. From the technical point of view, the adaptations to the measurement system and the increase of the measurement capacity is also worth to be mentioned. The power supplies and sample fixtures have been adapted to the current-controlled HBT devices. The test bench system is now capable of measuring 20 devices simultaneously, leading to a significant saving of test time and therefore, cost.

4.10 References for this chapter

[1] N. Pan , R.E. Welser, C.R. Lutz, J. Elliot and J.P. Rodriguez, IEICE Trans. Electron. **Vol E-82-C** (1999).

[2] D. Sawdai, Xiangkun Zhang, Dimitris Pavlidis and Pallab Bhattacharya, 16^{t}h Biennial IEEE/Cornell University Conference on Advanced Concepts in High-Speed Semiconductor Devices and Circuits (Aug. 1997), electronic document.

[3] R. Welser, N. Pan, C.R. Lutz and D.P. Vu, GaAs Mantech Proceedings Digest (1999), electronic document.

[4] J. J. Ebers and J. L. Moll, Proc. IRE **42** (1954).

[5] H. K. Gummel and H. C. Poon, Bell Syst. Tech. J. **Vol. 49**, 827 (1970).

[6] T. Low , C.P. Hutchinson, P.C. Canfield, T.S. Shirley, R.E.Yeats, J.S.C. Chang, G.K. Essilfie, M.K. Culver, W.C. Whiteley, D. C. D'Avanzo, N. Pan, J. Elliot and C. Lutz, GaAs IC symposium (1998), electronic document.

[7] J. Waltrop, K.C. Wang and P.M. Asbeck, IEEE transactions on electron devices **Vol. 39** (1992).

[8] D. Dawson, IEEE transacations on electron devices **Vol. 39** (1992).

[9] N. Fuller, Microwaves and RF , 55 (Feb.1997).

[10] J. Blakemore, Journal of Applied Physics **53(10)**, R123 (1982).

[11] D. Floriot, workpackage for Advanced POwer Subassemblies (APOS)-project (2000).

[12] M. Ott, What's new in electronics **20** (2000).

[13] M. Fukuda, SPIE **vol. 16**, 184 (1992).

[14] S. Sheu, J.J. Liou, C.I. Huang and D.C. Wilson, Annual Proceedings of Reliability Physics **Vol. 34**, 221 (1996).

[15] F. Ren , C. R. Abernathy, S. N. G. Chu, J. R. Lothian and S. J. Pearton, Solid State Electronics **Vol. 38**, 1137 (1995).

[16] T. Johansson, *The transistor, with emphasis on its use for radio frequency telecommunication*, PhD thesis, Linköping University, Sweden, 1998.

[17] J. Liou, S.H. Sheu, C.I. Huang et al., Solid State Electronics **Vol.39**, 415 (1996).

[18] T. Henderson, Microelectronics Reliability **Vol. 39**, 1033 (1999).

Chapter 5: Conclusions

The initial goal of the development of the in-situ test system was the shortening of test times from 4000 hours to a fortnight. Point of dearture was the High Resolution Resistance Measurement technique (HRRMT) which had been developed at the Instituut voor Materiaalonderzoek (Institute of Materials Research, IMO) for the exploration of the ageing of passive material systems. A study of feasibility performed on commercial electronic components showed the applicability of the method to active components as the measurement accuracy was of the same order than it has been achieved with the HRRMT on passive components. The first design of the measurement system was based on analogue voltage and current supplies and offered only limited versatility as every change of the stress conditions resultes in time-consuming hardware adaptations. In-situ accelerated life tests were then successfully demonstrated with MESFET structures which were known to be subject to gate sinking when put under thermal stress. The degradation of the MESFETs for a timescale of 4000 hours could then be forecasted based on an in-situ life-test of 60 hours for a timescale of 4000 hours which corresponds to the duration of conventional tests. With the application of the in-situ method to active electronic components, the issue of device self-heating was encountered. Under standard operating conditions, significant device self heating occurs. As many ageing processed are stimulated by temperature, the channel or junction temperature at life test conditions must be determined. An improved method has been developed to measure the thermal resistance of MESFETs under capacitive load and the method has been applied to MMIC amplifier modules. At this stage the different stress and measurement parameters were still realised by analog supplied which must be multiplexed. This multiplexing rendered the measurement process complex and prone to hazard. With the development of dedicated, digitally controlled power supplies and some necessary triggering and timing circuitry, the test bech system was extended toward full software control. This software controlled measurement system offered much more versatility as stress and measurement profiles could be adapted without effort. This novel test bench has been applied on pHEMT devices. The test profile was

similar to the accelerated life tests on the MESFETs conformal with procedures established in industry. As MESFETs and pHEMTs have many failure mechanisms in common, the results could directly be compared: The more recent HEMTs proved to be much more stable than the MESFET technology. Due to the accuracy of the in-situ test system, the first stages of devices ageing be studies in much greater detail as it had been possible using conventional test techniques. A similar shortening of test times could be achieved but the simultaneous occurrence of multiple detected failure mechanisms added a degree of complexity to the interpretation of results. Despite the significant savings in test time a lower time limit exists depending on the device technology and maturity. After the test on pHEMT devices, the test bench was then extended toward a multi-sample test system capable of measuring up to 20 devices simultaneously. The experience gained on the second incarnation of the test system proved worthwile as now multiplexing of the current meters had to be implemented. This multi-sample in-situ accelerated ageing measurement system was then applied to HBTs. As the HBTs were designed as power devices this meant an increased amount of self-heating during operation. In order to determine the junction temperature of the HBTs dependent on ambient temperature and dissipated power a novel method has been developed to measure the thermal resistance of the device. During the life testing of HBTs a significant progress has been made concerning device reliability: With the transition from AlGaAs to InGaP HBTs the devices showed virtually no degradation under standard test conditions. The time to failure could again be reduced by the application of higer stress levels but raised some questions about the proper interpretation of results. As a general conclusion it can be stated that the aim of the creation of an in-situ test system for the accelerated has been fulfilled. The issue of device self heating has been tackled by the development and application of suitable non-destructive electronic methods for the determination of the device thermal resistance. The increased measurement accuracy and resolution of the novel test system leads to a significant shortening of test times depending on device technology. The realisation of the concept as a completely software-controlled system with modular hardware makes the system applicable to a broad variety of devices and materials.

Chapter 6: Terminology and list of symbols

6.1 Terminology

AC	Alternating Current
accuracy, absolute	A measure of the uncertainty of an instrument reading compared to that of a primary standard having absolute traceability to the National Institute of Standards and Technology. It is expressed in ppm. Accuracy is often separated into gain and offset terms.
accuracy, rated	The limit that errors will not exceed when the instrument is used under specified operating conditions. It is expressed as a percentage (of input or output) plus a number of counts.
af	audio frequency; frequencies between 20 Hz and 20 kHz
bandgap	The amount of energy needed to move an electron in a semiconductor material from the top of the valence band to the bottom of the conduction band.
beta	current amplification factor expressed as $\frac{I_C}{I_B}$
BJT	Bipolar Junction Transistor; an active semiconductor device formed by two P-N junctions whose function is amplification of an electric current. Bipolar transistors are of two types NPN and PNP and have three terminals emitter, base, and collector. Operation of a bipolar transistor depends on the migration of both electrons and holes, in contrast to field-effect transistors (MESFET, HEMT etc.), where only one polarity carrier predominates.

compound semiconductor	A semiconductor material made up of elements from different columns of the periodic table, such as columns III and V or II and VI. III-V semiconductors include gallium arsenide and indium antimonide. II-VI semiconductors include zinc sulfide and cadmium sulfide.
conductance	The ability to conduct electricity. Defined by $\frac{G=R_e(I}{V)}$ where G is the conductance in Siemens, I is the current in Ampéres, and V is the voltage in Volts.
DC	Direct Current
DUT	Device Under Test
dynamic measurement	measurement condition where the device under test is out of thermal or electrical balance with its environment
EMI	Electro Magnetic Interference
FET	Field Effect Transistor, a device consisting of a gate, source, and drain. The voltage applied to the gate controls the conductivity of the channel between the source and drain. Examples of FETs are the MOSFET, JFET, and MESFET.
GaAs	Gallium Arsenide
gate length	Physical distance between source and drain of a field effect transistor measured on the photomask plate. When determined from the actual transistor characteristics, called "effective" gate length.
GPIB	General Purpose Interface Bus. It is an IEEE standard for parallel interfaces.
HAST	Highly Accelerated Storage Test
HBT	Heterojunction Bipolar Transistor
HEMT	High Electron Mobility Transistor; a HEMT is essentially a MESFET where the electrons in the conducting channel are confined in a ultrathin layer so that they form effectively a two-dimensional "electron gas". Electrons propagate without collision between source and drain (ballistic electron transport) which provides a high transient frequency and low noise.

HRRMT	High Resolution Resistance Measurement Technique
HTOT	High Temperature Operating Test
IEEE	Institute of Electrical and Electronics Engineers.
InGaP	Indium Gallium Phosphide
intrinsic semiconductor	A pure semiconductor that has not been doped. Since it is not doped, it is neither n-type nor p-type and electrons and holes carry charge in equal concentrations.
JFET	junction field effect transistor; FET where the gate consists of a p-n junction. JFETs are normally on, so a negative gate/source voltage must be applied to control the drain current.
junction, abrupt	semiconductor junction with abrupt transition from one semiconductor type (material, doping) to another
junction, graded	semiconductor junction in which the material composition is varied continually (Example $Al_xGa_{1-x}As$ where x is varied from 0.5 to 0)
junction, hetero-	junction made up from semiconductor materials with different band gaps
junction, homo-	junction made up from similar semiconductor materials with different doping types
junction, pn-	The interface between n-type and p-type semiconductor material. This structure forms a pn-junction diode.
LTSCA	Local Temperature Sensing and Correction Algorithm
maximum frequency	highest frequency at which an active electronic device exhibits power amplification
MESFET	MEtal Semiconductor Field Effect Transistor; electronic device where the current through a conducting channel is controlled by the electric field of the gate electrode. The gate is formed by a Schottky junction. MESFETs are normally on devices (depletion mode), so a negative gate voltage must be applied.

MOSFET	Metal Oxide Semiconductor Field Effect Transistor; FET where the gate is insulated from the channel by a thin SiO_2 oxide layer which allows positive gate voltages. MOSFETs are available as normally-on (depletion) and normally-off (enhancement) devices.
MTTF	Median Time To Failure; time when half of the device have failed
n-type	The conductivity type of a semiconductor material when the are electrons, hence negative. N-type silicon is doped with dopant atoms from column V of the periodic table, such as phosphorus.
noise	here any undesirable electrical signal from an external source such as an AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, radio transmitters, and others.
non-equilibrium	The condition in a semiconductor device or material when there is still a tendency for its macroscopic properties to change with time.
NPLC	Number of Power Line Cycles; multitude of 20 ms (Europe) or 16.67 ms (US)
ohmic contact	A resistive contact between a semiconductor material and metal. This type of contact exhibits a straight line I-V characteristic with a small value of resistance and does not significantly rectify
p-type	The conductivity type of a semiconductor material when the majority of carriers are holes, hence positive. P-type silicon is doped with dopant atoms from column III of the periodic table, such as boron.
pHEMT	pseudomorphic HEMT; high electron mobility transistor with a pseudomorphic channel

PID-regulator	PID stands for Proportional-Integral-Differential; linear regulating algorithm which supposes that the behaviour of the regulated device can be approximated by a RLC network. E.g. the properties of the furnace system can be approximated by thermal resistance and thermal capacitance.
ppm	parts per million
pseudomorphic	a structure is called pseudomorphic when a crystalline layer is grown on a material with a slightly different crystal lattice size. The size difference is small enough that no open bindings are formed but strain is introduced at the interface of the two layers
REDR	Recombination Enhanced Defect Reaction
resolution	The smallest value of input (or output) signal, other than zero, that can be measured (or sourced) and displayed. Also called sensitivity or minimum resolvable quantity. For data acquisition it means the smallest signal increment that can be detected by a measurement system. It is usually specified in "bits."
response time	For a measuring instrument, the time between application of a step input signal and the indication of its magnitude within a rated accuracy. For a sourcing instrument, the time between a programmed change and the availability of the value at its output terminals. Also known as Settling Time.
rise time	The time required for a signal to change from a small percentage (usually 10%) to a large percentage (usually 90%) of its % peak-to-peak amplitude.
rf	radio frequency; term used for frequencies suitable for communication purposes
sample rate	The rate at which a continuous-time signal is sampled. It is frequently expressed as samples/sec (S/s), kilosamples/sec (kS/s), or Megasamples/sec (MS/s).

Schottky contact	A junction or barrier formed by the direct contact of semiconductor materials with a metal. This type of contact rectifies signals and may also exhibit some resistance.
semiconductor	An element such as silicon or germanium or a compound like GaAs that has an intermediate band gap. Unlike metals that freely conduct and insulators that do not conduct charge, semiconductors selectively conduct charge through the movement of holes and electrons.
steady-state measurement	condition where no change dependent on time occurs; e.g. when the device under test is in thermal and electrical balance with its environment
TCR	temperature coefficient of resistance
temperature coefficient	A change of a measured parameter with a change in temperature.
transconductance	The ratio of the incremental change in the output current of any amplifying circuit or device to the incremental change of input voltage causing it, when the output voltage is held constant.
transient frequency	Inverse of the time needed for current in an active electronic device to travel from source to drain or emitter to collector.
trigger	An event that starts or stops an operation. A trigger can be a specific analog, digital, or software condition.
valence band	The energy levels of the electrons in he outermost shell of the atoms making up a solid material.

6.2 List of Symbols

α	temperature coefficient
a	fit parameter
Å	Ångstrøm, (10^{-10} m)
A	pre-exponential factor (Arrhenius)
A_C	current acceleration factor
A_F	thermal acceleration factor
Al	aluminum
As	arsenic
B	bandwidth (Hz)
C	concentration of particles ($1/m^3$)
C_s	surface concentration ($1/m^3$)
δ	voltage exponent
d	depletion depth (m)
D	reaction rate (1/s)
D_0	constant
D_S	slope of degradation
E_a	activation energy (eV)
E	electrostatic field (V/m)
ε_0	vacuum dielectric constant (8.854 pF/m)
ε_{GaAs}	GaAs dielectric constant (13.1)
ε	dielectric constant
erfc	error function
φ_b	gate potential (V)
γ	humidity exponent
g_m	transconductance (A/V)
Ga	gallium
GaAs	gallium arsenide
Ge	germanium
h	Planck's constant 6.626 10^{-34} Js
I	current (A)
I_B	base current (A)
I_C	collector current (A)

I_D	drain current (A)
I'_D	reduced drain current (A)
I_{DSS}	drain saturation current (A)
I_G	gate current (A)
I_S	diode quiescent current (A)
In	Indium
J	particle flux
j	current density (A/m^2)
k	thermal resistance exponent
J(x)	particle flux ($1/m^2$)
k_B	Boltzmann's constant ($1.38066 * 10^{-23} J/K$)
k_e	Boltzmann's constant divided by electron charge e ($8.5755 * 10^{-5}$ $\frac{J}{KAs}$)
m	particle mass (kg)
n	current exponent
n_{ideal}	ideality factor
n(x)	concentration of particles $1/m^2$
v_{sat}	saturation velocity (m/s)
Ni	nickel
p	property
P	power (W)
P_{diss}	dissipated power (W)
Pt	platinum
q	elementary electron charge (1.602*10^{-19} As)
R	resistance (Ω)
R_G	gate resistance (Ω)
R_D	drain resistance (Ω)
R_S	source resistance (Ω)
R_{gas}	molar gas constant 8.314 J/(mole K)
R_{th}	thermal resistance, (K/W)
R_{thja}	thermal resistance junction to ambient (K/W)
R_{thjc}	thermal resistance junction to case (K/W)
RH	relative humidity
S	surface (m^2)
SiO_2	silicon dioxide (quartz)

t	time (s)
t_{50}	mean time to failure (s)
T	absolute temperature (K)
T_0	initial temperature (°C)
T_{amb}	ambient temperature (°C)
T_{ch}	channel temperature (°C)
T_{jct}	junction temperature (°C)
T_n	temperature at iteration step n (°C)
T_s	setpoint temperature (°C) (°C)
Ti	titanium
U	voltage (V)
U_{BE}	base/emitter voltage (V)
U_{CE}	collector/emitter voltage (V)
U_{CB}	collector/base voltage (V)
U_{GS}	gate/source voltage (V)
U'_{GS}	reduced gate/source voltage (V)
U_{DS}	drain/source voltage (V)
U_{noise}	noise voltage ($V/\sqrt{Hz}$)
U_p	pinch-off voltage (V)
U_{th}	threshold voltage (V)
W	tungsten
W_G	total gate width (m)
W_A	active gate layer width (m)
X_d	diffusion depth (m)
Z^*	effective particle charge (C)