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Solar cells from epitaxial foils: an epifoil epiphany

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Abstract

In this paper we want to share our efforts on how to translate our high-quality epitaxial foils (epifoils) into cell-level performance. After framing our motivation in the introduction, we elaborate our approach at imec using available background on this topic and expected challenges. After presenting our method, consisting of layout, buildup and processing sequence, we share and compare our findings, discuss our characterization methods and add some basic simulations to improve our understanding.
In conclusion, we demonstrated how we could process epitaxial foils into cells, using a completely low-temperature process and keeping the foils attached to a carrier (parent wafer for the frontside, superstrate glass for the rear side) all the way through. Even though there is room for improvement on several aspects (both electrical and optical), in a first attempt this cell integration already resulted in a best open-circuit voltage (Voc) of 695 mV. Based on the loss analysis, the most promising improvements and their potential impact are pointed out.

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Keywords: epitaxial foils; silicone bonding; cell-module integration

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1. Introduction

Worldwide, even despite severe crises inside as well as outside of its business span, photovoltaic (PV) energy production, by far dominated by crystalline silicon-based technology, continuously and steadily grows in importance as a source of renewable energy, due to a number of reasons.

- Considerable effort and investment in the last decades has improved understanding, performance and reliability of this technology and generated an enormous (over)capacity of state-of-the-art production equipment ready for high-volume manufacturing. Altogether this has resulted in significant reductions of production and installation costs.
- In terms of degradation, it is considered highly reliable due to the absence of any moving parts and its proven performance in the field.
- From a society perspective, a growing awareness of environmental aspects and geostrategic dependancies has fueled the demand for renewable energy (in general) that can be produced locally.
    - Considering the speed and ease to deploy and its scalability at system-level, PV modules are very well suited to meet this demand.
    - In view of the scarcity of land area close to humanity's population-dense centers (where the generated energy will be mainly consumed), PV modules can be integrated on top of, or even inside these centers and thus reduce consumption of (scarce) land.
    - Its flexibility and scalability at (sub-)module level allows a least-obtrusive integration, thereby providing additional functionality (electricity-generating capacity) to the existing materials in area-consuming structures (buildings, transportation,...).
    - Local production reduces transmission losses and increases energy autonomy, allowing reduced grid transport (though smart grid adaptation with 2-way transport is required)

As a general motivation for the research in this paper, here we report on an effort to further reduce the consumption of resources for Si wafer fabrication. As method to realize this, we propose to go to thinner wafers, as an obvious choice which also can benefit Voc (assuming sufficiently low surface recombination velocities can be achieved [1]), and epitaxial deposition of silicon directly from silane to avoid the energy-intensive Siemens and Czochralski processes as well as the kerf loss from traditional wafering. Conveniently, thinner wafers also imply lower weight and increased mechanical flexibility, interesting opportunities from the perspective of unobtrusive integration. Going further down this route considering aesthetic aspects, much thinner cells could even be of interest for semi-transparancy purposes, however (of course) at the cost of electrical efficiency.

With this in mind, an approach for the fabrication of Si PV cells/modules based on thin Si wafer material, is being developed and reported by imec. This so-called i2-module concept is illustrated in Fig. 1 [2].

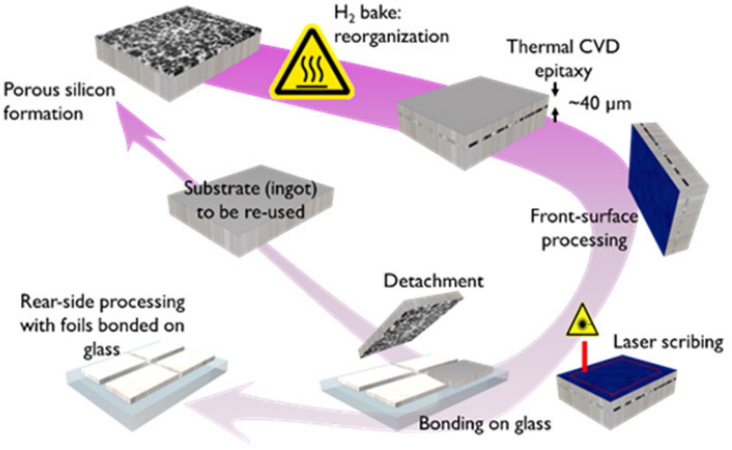

Fig. 1. i2-module concept using epitaxy for fabricating (thin) Si wafer material and cell processing while the foil remains attached to a carrier throughout the process

To fabricate the thin wafer material itself, 2 routes are currently in use at imec, shown in Fig. 2. The first one is based on electrochemical etching of a porous Si layer by anodisation; this is the most interesting one from a commercial point-of-view, as it has the lowest cost potential. The second route involves a lithographically-defined profile, which is more interesting from a quality perspective, as this process is currently better controlled and more reproducible, though at a significantly higher cost. Either stack is then reorganized into a layer structure that can act as a template for epitaxy as well as a release layer during detachment of the foil [3]. In the current work we used the lithography-based (n-type) foils for reasons of availability and reproducibility.

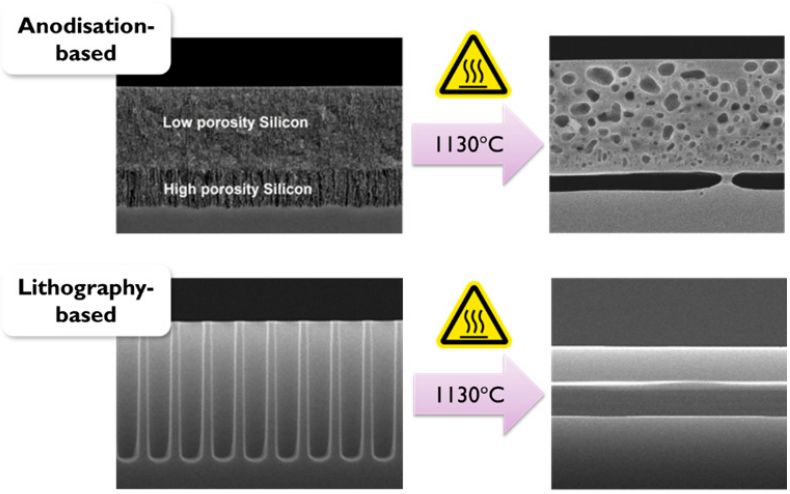

Fig. 2. Preparation of template material for epitaxy for 2 routes being used at imec to obtain (after detachment) thin wafers: based on anodisation (top) and on deep UV lithography (bottom)

After epitaxial thickening, where the thickness can be tuned, the wafers, at this point called epifoils, still have to be processed into cells. Considering the fragility of 40 um thin foils (significantly thinner than standard cells, typically >150 um), the challenge here is to have a high yield in terms of mechanical breakage, as well as maintain the high quality (bulk lifetime) of the epitaxially grown foil.

2. Background and challenges

For these developments, we want to build as much as possible on available experience and knowhow at imec. In this perspective, we have in the past reported on several relevant aspects:

a. A complete IBC cell integration process using thick wafers, where the frontside and a (full-area) diffused emitter at the rearside was first processed standalone, then bonded to glass with shielded silicone, and, most relevantly here, the rearside (emitter passivation and patterning, i/n+-aSi:H BSF deposition and patterning and metallization deposition and patterning) finished while bonded to glass [4]; additionally, also a similar run with a complete IBC cell integration process has been reported, though with a i/p+-aSi:H emitter deposited after bonding instead of a diffused emitter before bonding [5]
b. High lifetimes of passivated epifoils, obtained by anodisation and lithographic patterning, and using a silicone area smaller than the epifoil [3]
c. Influence of presence of silicone on aSi:H passivation, and options to reduce this detrimental impact: either by shielding the silicone from the plasma [6] and performing a material outgassing prior to aSi:H passivation [7], or by capping the exposed silicone surface with a dielectric mask or a crust formed by a plasma treatment [8]

Although combining this experience should already take us a long way, still important challenges remain to be tackled. Here we want to integrate thin epifoils into cells, but simply inserting the available high-lifetime epifoils into the available cell process is not as straightforward as it may seem:

- As we want to minimize handling and processing of standalone epifoils, the frontside has to be processed while the epifoil is still attached to the parent wafer. After extensive testing, however, it was clear that high-temperature (>800°C) diffusion and deposition processes, used in the available cell process (a), are not possible since they result in collapse of the foils and they can then no longer be detached from the parent [9]. This means we have to adapt to an alternative frontside at sufficiently low temperatures.
- The available cell process (a), as well as the obtained highest lifetimes of bonded epifoils (b) involve shielded silicone to minimize the impact of silicone during aSi:H passivation. However, whereas this is still acceptable for processing samples for lifetime testing (b), significant yield issues arise in more complex cell processing with several wet process steps. In particular, the flaps overhanging at the silicone edge are exposed to mechanical stresses from the liquid and additionally trap liquid, that is more difficult to dry. While not so problematic for thick wafers (a), the fragility and flexibility of the thin wafers imply respectively more breakage and drying that is even more difficult. This is illustrated in the scaled drawing in Fig. 3.
- While we have promising results in reducing the detrimental impact of exposed silicone (on the effective lifetime) through capping and plasma treatments (c), these results have been achieved on thick wafers and remain to be confirmed on epifoils.

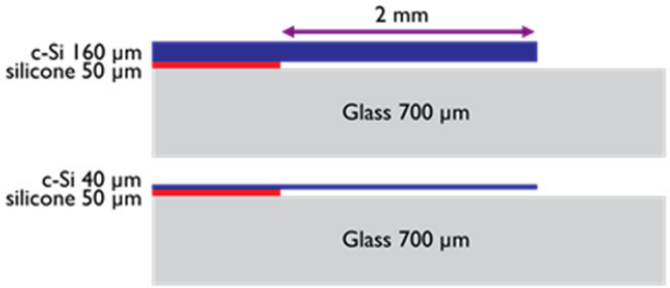

Fig. 3. Thinner wafers increase risk of breakage at fragile edges and increase issues with liquid trapping during wet processing

3. Cell layout, buildup and processing

To cope with the above challenges, we decided to use a blanket structure for the silicone (i.e. a silicone area larger than the epifoil area), implying exposed areas of silicone in the subsequent processing. To cope with this exposed silicone, we apply dielectric mask capping (c) on the one hand, on the other we reduce process complexity by choosing as first attempt a 2-side test structure which avoids the need for patterning at the rear and limits the amount of process steps with the exposed silicone.

Of course 2-sided contacting requires probing access to the front busbar, also after the foils are bonded to glass. Therefore, premade holes in the glass are aligned to the busbars of the cells during bonding. The resulting schematic cross-section is shown in Fig. 4.

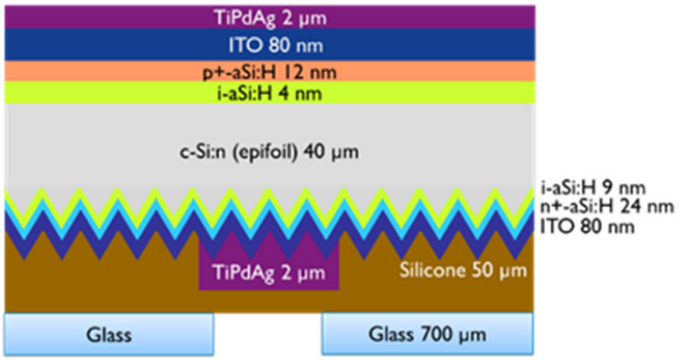

Fig. 4. Schematic cross-section of the cell buildup (not to scale); the front side glass facing the sun is drawn here at the bottom

First the frontside of the foil is processed while it is still attached to the parent wafer. Avoiding high temperatures (see above), the surface is random pyramid textured, and passivated with an i/n+- aSi:H front surface field (FSF). ITO is deposited to act both as antireflection coating (ARC) and conductive layer underneath the TiPdAg finger grid evaporated through a shadowmask. After this the foil is detached from the parent wafer: lasercutting defines the area of the foil to be released. Then the foil is bonded with a silicone area larger than the foil, and the rear side is processed. For this a stack of aSi:H/SiO2/aSi:H is first deposited on the silicone as capping layer; the wafer itself is shielded from this deposition by a shadowmask. Then an i/p+-aSi:H emitter stack is deposited, followed by ITO and TiPdAg, all covering the full area. After a final anneal the different cells defined by the frontside metallization are separated mechanically by wafer sawing. The process is shown schematically in Fig. 5.

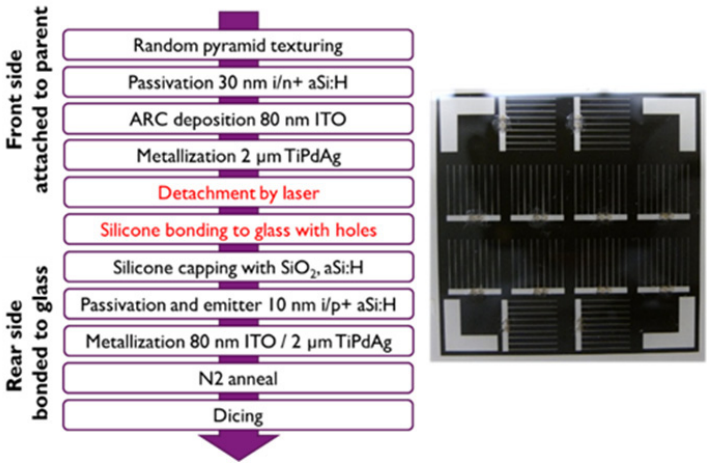

Fig. 5. Used process sequence for cell integration of the epifoils (left); front view of the resulting (12) cells before dicing (right), note the holes in the glass to contact the busbars on the front

Worth mentioning here is that throughout the whole process, the temperatures to which the foil is exposed is well below 300°C. This reduced thermal budget compared to conventional cells with diffusion and even firing steps at the end will result in reduced thermomechanical stresses and a smaller ecological footprint [10].

As much worth mentioning, though less beneficial, is that we have observed nonuniformities in the frontside metallization (deposited through shadowmask), in particular significant variations in finger width, and sometimes (air) bubbles escaping from the silicone at the edges of the foil and at the holes in the glass during ultra-low vacuum deposition steps (aSi:H, ITO, TiPdAg). Both of these will likely impact both the quality and spread in performance of the resulting cells as well as the stability and reproducibility of the process.

4. Results and characterization

The resulting performance of the cells is shown in Table 1, and compared to several state-of-the-art results. At first glance it is clear that we have a high open-circuit voltage (Voc), though a low overall efficiency (eta) due to a moderate fill factor (FF) and low short-circuit current density (Jsc). The higher Voc can be explained by the higher Voc potential of heterojunction used in our process, compared to the homojunctions in [4] and [11]; for [12] it is not clear what type of junction has been used. The losses in Voc, FF and Jsc are analysed in a breakdown in the following paragraphs.

Table 1. Performance of the fabricated cells and comparison to state-of-the-art references

Sample result	Thickness [µm]	Bonded	High-temperature	Size [cm²]	Active [cm²]	V_{oc} [mV]	FF [%]	J_{sc} [mA/cm²]	Eta [%]
AVERAGE (7 cells)	40	Y	N	1.1x1.1	1.1x1.0	689 ±5	69.3 ±5.6	23.9 ±0.6	11.4 ±1.0
BEST	40	Y	N	1.1x1.1	1.1x1.0	695	73.4	24.0	12.2
[4] (IMEC)	160	Y	Partly	2.5x2.5	2.0x2.0	652	75.2	37.2	18.2
[11] (ISFH)	43	N	Y	2.5x2.5	2.0x2.0	650	77.6	37.8	19.1
[12] (SOLEXEL)	40	Y	??	15.6x15.6	15.6x15.6	683	78.9	38.3	20.6

4.1. Open-circuit voltage Voc

To assess and interprete our results, and draw the correct conclusions from it, we want to make the link between Voc and lifetime in the cells. For this, we use the following approach:

- The Voc is defined by doping and injection level (Δp):

$$V_{oc} = \frac{kT}{q} \ln \frac{(N_D + \Delta p)\Delta p}{n_i^2} \tag{1}$$

- The injection level determines the effective lifetime, if the generation rate is known:

$$G_L = \frac{\Delta p}{\tau_{eff}} \tag{2}$$

- Combining these equations, the injection level can act as link between the effective lifetime and Voc. This results in the graph shown in Fig. 6. For this simulation we assumed a doping level (N_D) of 1e16 cm-3, and a generation rate (GL) of 4.55e19 cm-3s-1, obtained by calculations using Cuevas' QSS model [13].

This means for the measured Voc of around 695 mV, the effective lifetime of the foil would be around 70 us. This is much lower than previously achieved effective lifetimes in epifoils, reaching above 300 us [3]. If we could reproduce this effective lifetime in the cell, the same graph predicts a Voc of over 740 mV.

The cause for these lower effective lifetimes becomes clear when we look at the dark I-V curves of the cells, where we observe non-ideal behaviour due to a significant increase in J02 and n2.

In our case, this increase is attributed to a number of causes:

- The influence of edge recombination, significant due to small areas after dicing
- A not-yet-optimized i/p+ aSi:H emitter deposition
- Some remaining influences of the exposed silicones in this deposition

These aspects were all different in the case of the previously obtained high lifetimes, where the foil size was larger than the silicone area, an optimized i/n+-aSi:H passivation was applied and silicone was capped with a different mask.

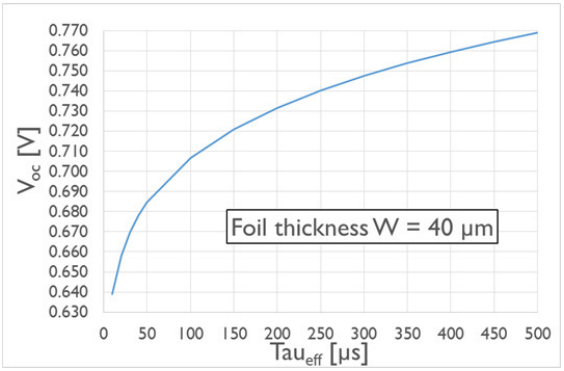

Fig. 6. Impact of effective lifetime on Voc, for 40 um thick Si foils

4.2. Fill factor FF

Looking more closely at the FF, its breakdown for the best cell is shown in Table 2. The series resistance here causes ~4% FF loss, the main contribution coming from the contact resistance in the i/p+-aSi:H/metal stack . There is also a limited contribution of shunt resistance in the FF loss, ~1%, however a significant portion of FF loss is still present if we look at the remaining gap with FFJ01. This we attribute, similarly as above for the Voc, to the observed increased J02 values [14].

Table 2. Breakdown of FF losses

Sample result	FF [%]	R_s [Ohm.cm²]	FF-R_s [%]	R_{sh} [Ohm.cm²]	FF-R_s-R_{sh} [%]	FF_{J01} [%]
BEST	73.4	1.5	77.8	2900	78.4	84.6

4.3. Short-circuit current density Jsc

The Jsc losses are indicated in Fig. 7. The table shows a low Jsc of 24 mA/cm2. However, due to the small non-standard size of the cells, there is some uncertainty in the reference calibration, and edge recombination will reduce the current. Additionally, the cells are shaded by a ~10% busbar area. To avoid these effects, we can determine Jsc from spectral response measurements with a limited opening slit, by scaling and integrating the (measured) external quantum efficiency (EQE) with the AM1.5g spectrum. This results in a Jsc of 30 mA/cm2.

Sample result	Size [cm²]	Active [cm²]	Jsc_IV [mA/cm²]	Jsc_SR [mA/cm²]
BEST	1.1x1.1	1.1x1.0	24.0	30.0

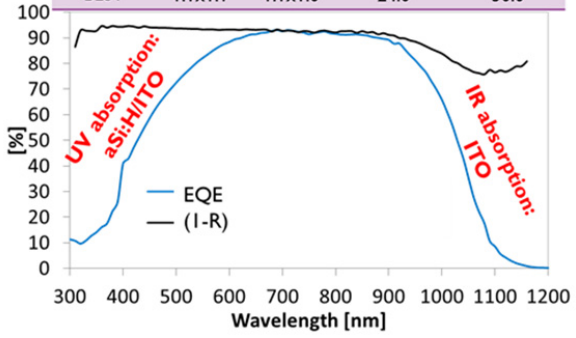

Fig. 7. Breakdown of Jsc losses: Jsc_IV and Jsc_SR respectively give the value measured by light IV measurement and derived by spectral response measurement (top table); parasitic absorption losses can be determined from comparison between EQE and (1-R) (bottom graph)

In Fig. 7 we also plot (1-R). Assuming there is no transmission (which is the case since we have a fully metallized area at the rear), this represents the light absorbed in the stack. Comparing both curves, the difference between them can be attributed to parasitic absorption [15].

The main suspects for parasitic absorption are the aSi:H and ITO layers, considering typical k values [16]. To better distinguish this parasitic absorption in the different layers however, and spot potential improvements, we ran some basic optical simulations, assuming flat cells, and compared the results with reflectance measurements on flat cells with the same buildup. The results are shown in Figure 8 and Table 3. In terms of validation, comparing (1-R) with the simulated total stack absorption indicates a relatively good match. The remaining differences we attribute to:

- Fingers were not taken into account for the simulation: this implies the measured reflectance will be higher than what is simulated (300-400nm and 650-750nm)
- Concerning ITO the calculations were done with k-values before annealing. Since we know this ITO exhibits an increased parasitic absorption after annealing, we can expect higher parasitic absorption in the measurement than in the simulation (500-600nm and 1050-1200nm)

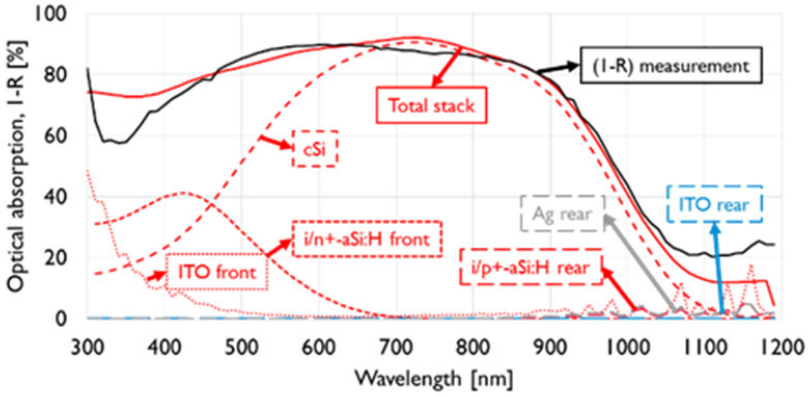

Fig. 8. Optical simulation indicating spectral per-layer-absorption for bonded flat cells, with comparison to measured value for (1-R)

Table 3. AM1.5g-weighted absorption (left) and extrapolation to current (assuming collection efficiency of 100%, right)

Layer	Absorption [%]	Simulated Current [mA/cm^2]
ITO front	2.5	1.0
i/n+-aSi:H front	7.5	3.1
cSi	59.9	24.7
i/p+-aSi:H rear	8×10^{-8}	3×10^{-9}
ITO rear	0.5	0.2
Ag rear	0.6	0.3
Overall	70.9	

Based on this simulation, most of the parasitic absorption is taking place in the front i/n+-aSi:H (33 nm thick), causing 3.1 mA/cm2 Jsc loss. Using this simulation to check the impact of reducing the thickness of this layer, Figure 9 shows that we can e.g. halve this loss by halving the thickness. Considering this simulation is valid for a flat surface, even more improvement can be expected from a textured surface, as parasitic absorption will be increased with an increased incoupling of light. An alternative option could be to use a different stack which exhibits less absorption while still allowing a good surface passivation. A promising candidate for this involves e.g. AlOx for passivation and SiNx as anti-reflective coating.

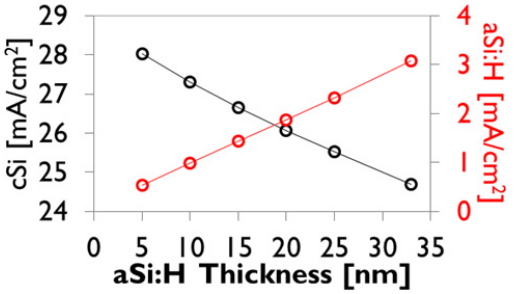

Fig. 9. Simulation for flat cells indicating impact of the thickness of the front i/n+-aSi:H on Jsc loss due to parasitic absorption in that layer

5. Conclusions and outlook

In this paper we demonstrated a potential cell process for epitaxially grown foils, using a completely low-temperature process and keeping the foils attached to a carrier (parent wafer for the frontside, superstrate glass for the rear side) all the way through. Though there is room for improvement on several aspects (both electrical and optical), in a first attempt this cell integration already resulted in a best open-circuit voltage (Voc) of 695 mV.

Based on the loss analysis, potential improvements become clear:

- Improved capping of the silicone can push Voc values, theoretically to over 740 mV if lifetimes in the epifoil demonstrated in the past can be maintained in the cell
- Increasing the cell size can reduce edge recombination influences (J02 effect on Voc, FF and Jsc)
- Decreasing the frontside parasitic absorption, e.g. by decreasing the aSi:H thickness will boost the current

Combining these improvements, we can see a nice potential for larger IBC devices with improved capping and decreased parasitic absorption, and where the frontside absorption can be even further reduced by removing shading losses from finger/busbar grid and replacing the optically absorbing ITO with a (low-temperature) SiNx ARC. Such a layout is shown schematically in Figure 10.

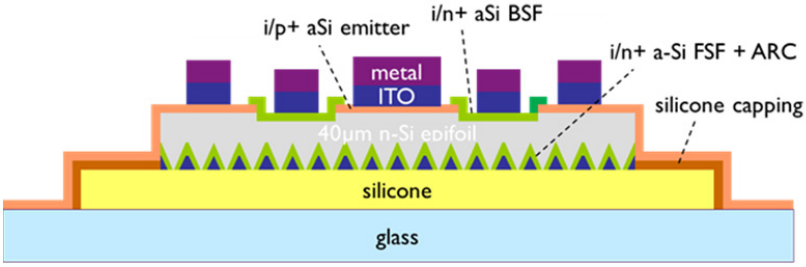

Fig. 10. Layout of IBC structure incorporating potential improvements.

Acknowledgements

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