Evidence for source side injection hot carrier effects on lateral DMOS transistors

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Abstract

The hot carrier degradation behavior of lateral integrated DMOS transistors is studied in detail with a state-of-the-art, high-resolution measurement equipment. It has been demonstrated that two degradation mechanisms are present: electron mobility reduction due to interface trap formation and injection and trapping of hot electrons at the source side of the channel. It will be shown that the Source Side Injection mechanism gives rise to rather moderate changes of the linear drain current ($I_{d,lin}$) but significant changes of the saturation drain current ($I_{d,sat}$) and the threshold voltage (V_t).

1. Introduction

For many smart-power applications, the capability of handling high drain voltages and high current levels needs to be combined with standard low voltage CMOS logic cells. Lateral DMOS transistors (LDMOS) are the devices of choice and their electrical behavior is well documented. Unlike for standard CMOS transistors, high voltage MOS transistors exhibit an electric field and carrier temperature distribution which is a complex function of Vds and Vgs, the device process and layout parameters. As a result, the physical degradation mechanisms in lateral DMOS devices are not fully understood [1], [3]. In this paper, we present a hot carrier degradation study of LDMOS devices from a 0.7 μm based Smart Power technology. We demonstrate that different degradation mechanisms occur under these stress conditions and give evidence of an important Source Side Injection (SSI) effect, which leads to relatively fast degradation of a number of device parameters. In the first section the devices and experiments are described. The next section discusses the experimental results and gives clear evidence for the existence of a source-side injection degradation component. Finally in the last section we draw some conclusions.

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2. Devices and measurements

The devices used in the present study are lateral DMOS transistors processed in a 0.7 µm CMOS based smart power technology [1]. The devices have a field oxide in the drift region. The channel implant is self-aligned to the poly gate. The gate oxide thickness is 42 nm, V_t=2.4V, V_{bd}=54V and the specific on-resistance R_{on} is 90 mΩ*mm^2. Hot carrier stress experiments are carried out on packaged samples using a special designed chamber with a temperature stability of 0.03 °C [2]. With this set-up, high drain voltages up to V_d=40V and high gate voltages up to V_g=15V are applied in order to accelerate the hot carrier degradation. Linear drain current ($I_{d,lin}$, measured at Vg=12V, Vd=0.5V), saturation drain current ($I_{d,sat}$, measured at Vg=5V, Vd=30V), and the extrapolated threshold voltage (V_t) have been monitored continuously to analyze the physical degradation mechanisms.

3. Results and Discussion

The degradation parameters of two identical LDMOS transistors stressed at Vds=40V and Vgs=15V are shown in Fig.1. The linear drain current ($I_{d,lin}$) decreases with time and saturates. The saturation drain current ($I_{d,sat}$), however, shows a much larger drift, which is also reflected in a large shift of the threshold voltage (V_t) in the order of 1-2V. Also a large statistical spread for the $I_{d,sat}$ and V_t parameters is observed. I_d-V_g characteristics are plotted in Fig.2 (upper plot) before and after stress at V_{ds}=40V and V_{gs}=15V. At low V_g, where the current is dominated by the channel part of the DMOS transistor, we observe a clear horizontal shift of the curves. As a result, a large drift of $I_{d,sat}$ and a large V_t shift can be detected. At high V_g, where the current is dominated by the drift region of the DMOS transistor, a drop in current can be observed as well. I_d-V_g characteristics before and after stress at V_{ds}=40V and V_{gs}=9V (Fig.2, lower plot) do not show the horizontal shift of the transfer characteristic but still a decrease of the current in the high Vg-range. Out of these experimental observations, it is evident that two different degradation mechanisms occur in the LDMOS transistor [3].

The first mechanism is due to interface state generation and mobility reduction, which is normally observed under hot carrier degradation conditions. As a consequence, the current decreases and the impact generation will decrease. The creation of new interface

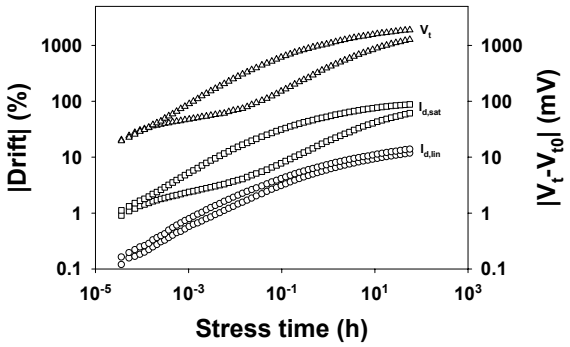

Fig. 1. Linear and saturation drain current during stress of two LDMOS transistors at V_d=40V and V_g=15V.

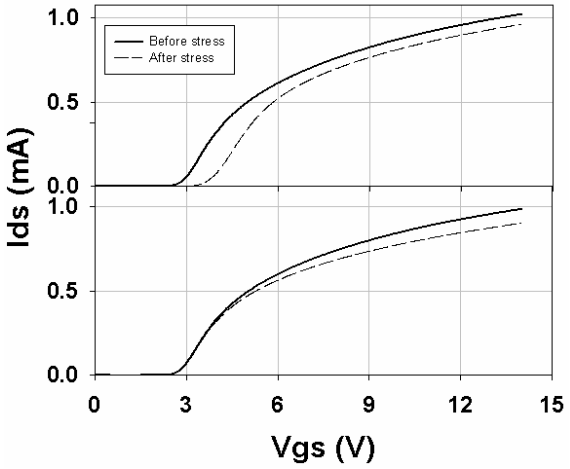

Fig. 2. Full line: I_d-V_g (V_d=0.5V) curve before stress at V_d=40V and V_g=15V (upper plot) and stress at V_d=40V and V_g=9V (lower plot). Segmented line: I_d-V_g (V_d=0.5V) curve after 200hours stress at V_d=40V and V_g=15V (upper plot) and stress at V_d=40V and V_g=9V (lower plot).

traps is reduced and the effect of the traps on the current distribution is diminished. As such, a certain equilibrium condition is reached and the degradation mechanism saturates [3]. However, experiments do not reveal whether this happens in the channel or in the drift region. Charge Pumping (CP) measurements are ongoing to resolve this issue.

The second degradation mechanism obviously strongly influences the $I_{d,sat}$ and V_t behaviour but is not detected on $I_{d,lin}$ measured at high Vg. A positive horizontal shift of I_d-V_g (Fig.2) is indicative for negative charge generation at the source side of the channel. Both parameters show a large spread between

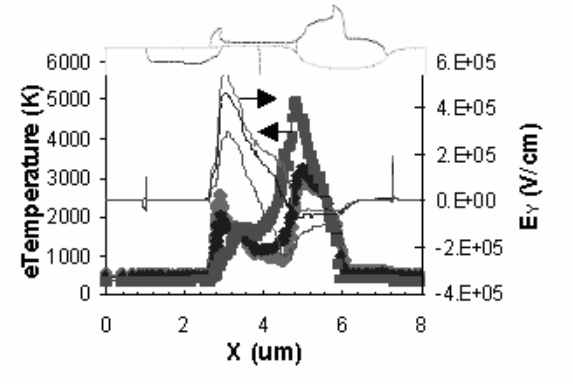

Fig. 3. Hydrodynamic TCAD simulations showing the perpendicular electric field and the electron temperature at the silicon surface, for different Vgs (Vds=40V: Vgs=6V (grey), 12V (black) and 15V (light grey).

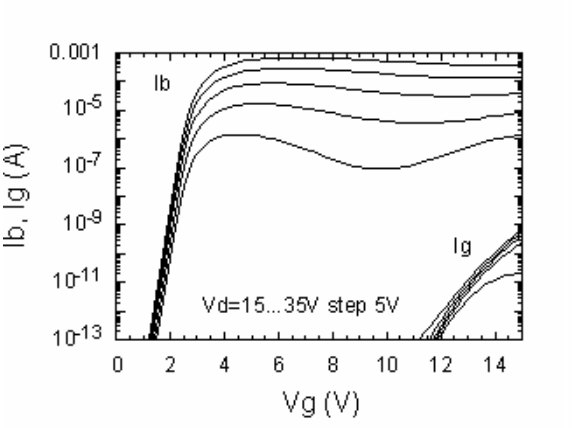

Fig. 4. Substrate and gate currents as a function of gate voltage for various drain voltages (15, 20, 30 and 35 V). At high gate voltages clear evidence for electron injection is found. The substrate current is strongly dependent on the drain voltage, but the gate current is only dependent on the gate voltage.

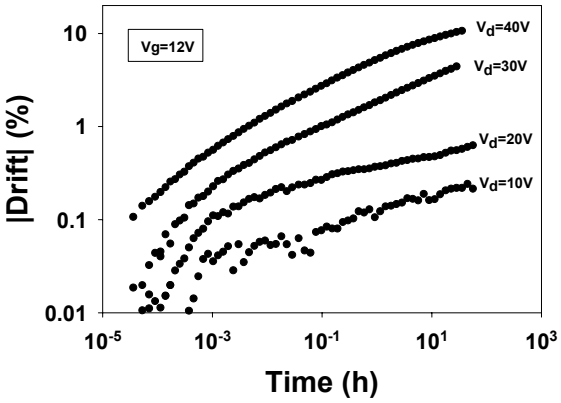

Fig. 5. Linear drain current degradation at drain voltage stress between V_d=40V and V_d=10 and at constant gate voltage V_g=12V.

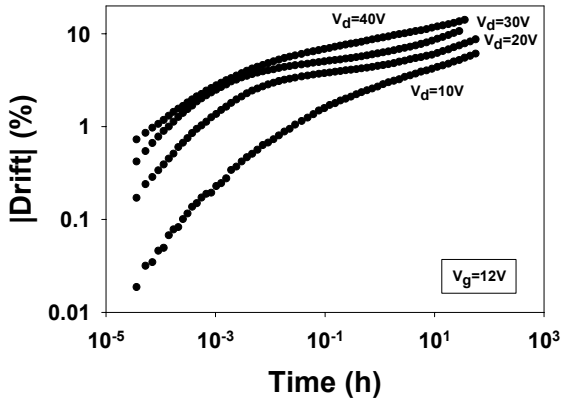

Fig. 6. Saturation drain current degradation at drain voltage stress between V_d=40V and V_d=10V and at constant gate voltage V_g=12V.

the two different measurements. All these effects can be explained by hot electron injection and trapping at the source side of the device, also known as Source Side Injection (SSI) [4]. TCAD simulations further support this idea. Fig. 3 shows the electric field and the electron temperature at the silicon surface for different Vg values (V_d=40V). An electric field peak at the source of the transistor is clearly present at high V_g. The electron temperature has two maxima, one at the source side of the channel, the other at the birds beak tip. Further evidence is also found by measuring the gate current of the device as shown on Fig. 4. A clear electron current is measured at the gate for the conditions where the large V_t-shift is observed.

In order to verify this further, measurements have been performed at drain voltage stress down to V_d=10V and at gate voltage stress down to V_g=3V in order to isolate the SSI. The linear drain current $I_{d,lin}$ degradation (Fig.5), which is most sensitive to damage in the drift region of the device, shows the exponential dependence on drain voltage, expected for the normal hot carrier degradation mechanism. However, $I_{d,sat}$ and V_t, which are more susceptible to SSI, show a very high drift, which is relatively insensitive to the drain

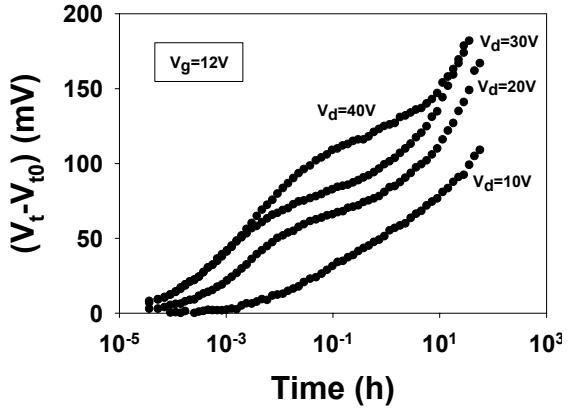

Fig. 7. Threshold voltage shift at drain voltage stress between V_d=40V and V_d=10V and at constant gate voltage V_g=12V.

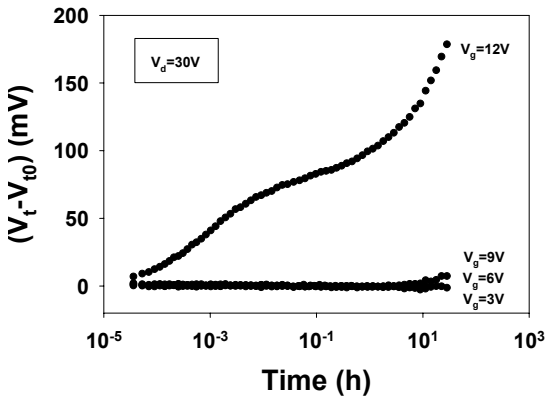

Fig. 8. Threshold voltage shift at gate voltage stress between V_g=3V and V_g=12V and at constant drain voltage V_d=30V.

voltage, as can be seen in Fig.6 and Fig.7. In contrast, the shift in Vt is clearly determined by the gate voltage and the vertical electric field, as shown on Fig.8, which is typical for a SSI mechanism. This is again confirmed by the gate current measured at high Vg, which is relatively insensitive to the drain voltage, but depends much stronger to the gate voltage (Fig. 6).

4. Conclusions

In this paper, the hot carrier degradation behavior of lateral integrated DMOS transistors has been investigated. Two degradation mechanisms have been identified: mobility degradation and Source Side Injection (SSI). Due to the first mechanism the drift of linear drain current ($I_{d,lin}$) increases with increasing drain voltage and tends to saturate for longer times. The SSI mechanism gives rise to larger V_t shifts and large $I_{d,sat}$ drift with a large statistical spread among different devices [1],[2].

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