Master's Thesis Engineering Technology

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Towards Software-Defined Radio on Configurable Hardware

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INTRODUCTION

Thanks to the significant growth in electronic smart devices the past decade, a relatively new concept has appeared, the Internet of Things (IoT). It allows objects to exchange data over the internet without the need for user interaction. According to Gartner [1], there will be a total of 20.4 billion connected 'things' by 2020, one more useful and life-saving than the other. To make sure that all these devices are capable of communicating with each other, the need for multi-protocol gateways, which act as 'translators', rises.

PROBLEM STATEMENT

Problems an IoT gateway processor might face are:

- not flexible enough when adding a node which is based on a different protocol that is not supported by the gateway,
- when the amount of data exceeds the performance, a new processor has to be implemented. This leads to an entirely new architecture for the gateway.

OBJECTIVES

Further exploring the role of Field Programmable Gate Arrays (FPGA) within Software Defined Radios (SDR) and how they can be used to create an IoT multi-protocol gateway. Individual objectives are:

- Literature study,
- Study bladeRF x115 depicted in Figure 1,
- Create 6LoWPAN repeater,
- Simulink ZigBee physical layer transceiver,
- HDL ZigBee modulator simulation.

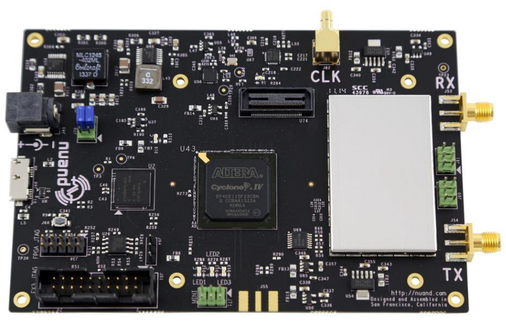

Figure 1. BladeRF x115 board

METHODS & MATERIALS

Message Repeater

- Adapt the architecture of bladeRF's Cyclone IV FPGA
- Sample FIFOs are connected to each other and control signals are rerouted as depicted in Figure 2
- Test repeater by sending a repetitive 6LoWPAN message using a Zolertia Z1 node

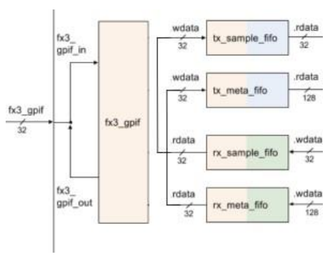

Figure 2. Zoom of message repeater architecture

Simulink Simulation

- Four different ZigBee physical layer modulator systems as depicted in Figure 3
- Communication system toolbox
- Calculate BER values with and without Direct-Sequence Spread Spectrum and Maximum Likelihood Estimator to determine quality

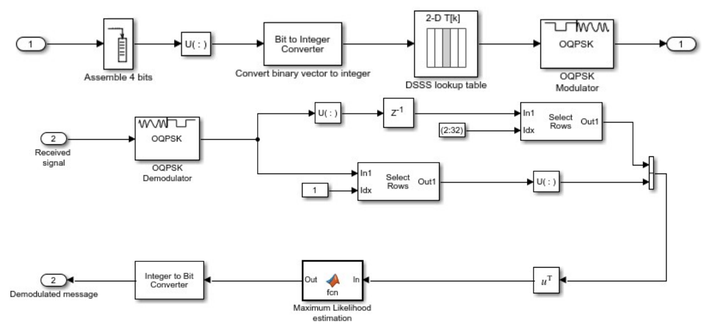

Figure 3. Simulink transceiver system (top is transmitter, bottom is receiver)

HDL simulation

- Based on Simulink results
- Xilinx ISE WeBPACK
- VHDL diagram depicted in Figure 4
- Determine values in pulse shaping block as sample rate is rounded plural of symbol rate (62,5 ksymbols/s)

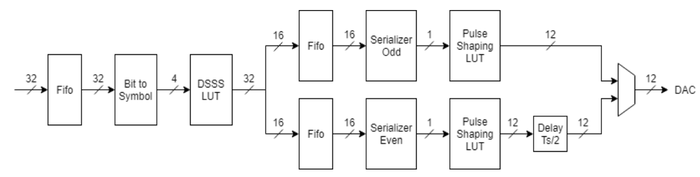

Figure 4. Diagram of VHDL ZigBee modulator

RESULTS & CONCLUSION

- 6LoWPAN repeater works despite interference of external sources
- HDL simulation is able to generate 12-bit signed half sine samples based on 32-bit inputs sequences after 14 system clock cycles despite introducing delays as depicted in Figure 5
- Concluding from all the tests, FPGAs will play an important role within SDRs as they enable parallel processing (hardware acceleration). More data can be processed within fewer clock cycles.

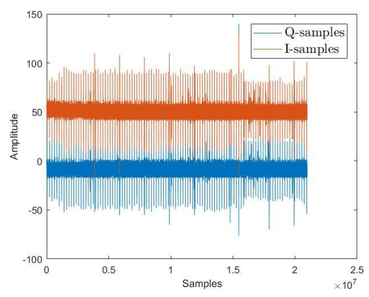

Figure 3. I- and Q-samples received and retransmitted by message repeater

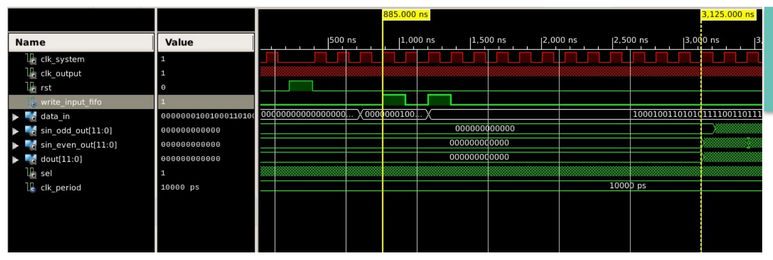

Figure 4. HDL simulation results

REFERENCES

[1] Gartner Says 8.4 Billion Connected "Things" Will Be in Use in 2017, Up 31 Percent From 2016. Feb. 2017. url: https://www.gartner.com/newsroom/id/3598917 (visited on 11/29/2017).

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