A mission profile-based reliability analysis framework for photovoltaic DC-DC converters

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Abstract

Reliability of DC-DC converters is important in photovoltaic (PV) applications like building integrated PV systems, where the module-level converter may be stressed significantly. Understanding and predicting the most life-limiting components with accurate degradation models in such systems enable the design for reliability. In this paper, a mission profile-based reliability analysis framework for PV DC-DC converters is proposed where the inputs and models of the framework can be adjusted according to the converter topology, the components and the failure mechanisms under investigation. The framework is demonstrated by comparing the influence of two yearly mission profiles on the solder joint degradation of a MOSFET in an interleaved boost converter. This is done by using an electro-thermal circuit simulation in PLECS and a finite element MOSFET model in COMSOL. This framework allows for exploring more accurate models or even simplifying parts with low sensitivity in order to obtain a thorough understanding of their accuracy and to determine the overall converter reliability.

1. Introduction

Building integrated photovoltaics (BIPV) are becoming more popular, where module-level DC-DC converters are employed. Under varying operation conditions, the DC-DC converter may be stressed significantly, which over time leads to failures. Typical lifetime of facade building elements is 50-75 years [1], meaning that the converters in BIPV systems should be designed to avoid frequent replacements—the power converter should be reliable. Degradation models of the most reliability-critical components (e.g., power devices) provide insights in the overall reliability of the converter. By considering the mission profile, they also determine whether the converter can be over- or under-dimensioned and potentially reduce the entire cost. In this regard, reliability modelling and analysis are of importance. The reliability modelling of electronic components has evolved towards a more physics-based approach to better understand and counteract the failures [2]. A flexible framework is needed to investigate the influence of different mission profiles and/or different physics-based models on the calculated lifetime of the components as well as the entire converter system.

2. Framework structure

In this paper, a reliability framework, based on [3], is proposed which allows any input or (sub)component-model to be exchanged by alternates or improved versions depending on applications, topologies, components and/or failure mechanism(s). The flowchart of the framework is shown in Fig. 1. In this paper, the methodology is demonstrated on the case study of an interleaved boost converter for BIPV systems. More specifically, the influence of two one-year mission profiles from Denmark and Arizona on the material degradation of the solder joint of the MOSFET is investigated, as it is known to be strongly affected by thermal cycling [4]. This means that the stress profile of the solder joint, which in this case only consists of thermomechanical stress due to the coefficient of thermal expansion (CTE) mismatch, becomes of interest. This profile is obtained by using an electro-thermal circuit simulation in PLECS that translates a mission profile (i.e., the irradiance and ambient temperature profiles for the converter system) to the thermal stress profile of the MOSFET.

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It should be noted that a steady-state look-up table is used to lower the computation time which is required for a long-term simulation (e.g., one-year profile). A finite element MOSFET model in COMSOL is then used to further translate the temperature profile to a local solder joint stress profile. Lastly, the time for crack initiation of the solder joint is calculated by using the cumulative damage model in COMSOL, which is based on the solder material's stress-cycle (S-N) curve following the diagram in Fig. 1.

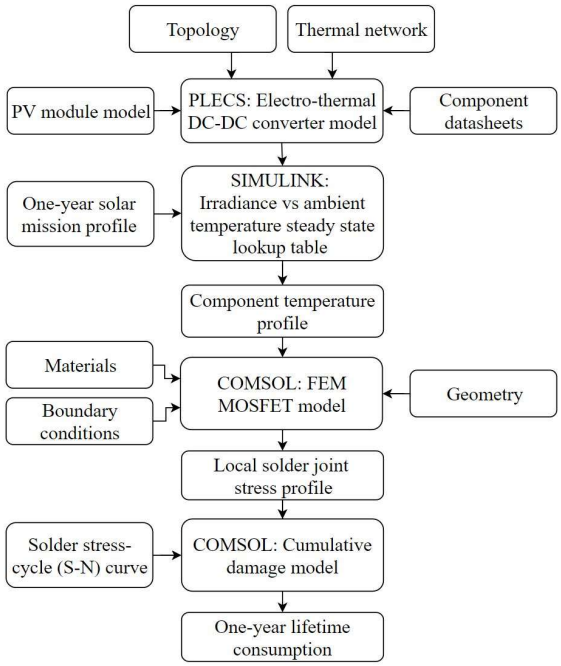

Fig. 1. Flowchart of the mission profile-based reliability analysis framework applied to the DC-DC converter.

3. Electro-thermal model

3.1 Electrical model

Isolated and non-isolated high step-up converters can be used in BIPV applications. Reviews on non-isolated topologies can be found in [5, 6]. In previous work, a cascaded interleaved boost converter and an isolated full-bridge converter using wide-bandgap (WBG) devices was proposed and experimentally tested [7, 8, 9]. However, the overall efficiency was considered very low and the component temperature increases very high. In this paper, another topology is studied, being an isolated interleaved boost converter, as depicted in Fig. 2. It is a current-fed converter that was derived via the duality principle from a voltage-fed half-bridge [10]. The converter was successfully applied for PV applications in [11]. Notably, in this paper, the converter is operated in the continuous conduction mode and the gain is given as

$$G = \frac{V_{out}}{V_{in}} = \frac{2n}{1-\delta} \tag{1}$$

with n being the transformer turns ratio and δ being the duty cycle. According to Eq. (1), it can be noticed that the normal boost gain is multiplied by the transformer turns ratio, enabling high step-up conversion ratios, which may be required in the BIPV application. The factor of 2 is a consequence of the voltage doubler rectifier that is used in the output. Another advantage is that the gate signals of the switches are phase-shifted by half the switching period T_s, leading to an effective ripple current reduction in the input side. The main disadvantage of this converter is that two inductors and a transformer are used, making it rather bulky compared to, for example, the switched capacitor or flying capacitor boost converters [12, 13]. The key parameters of the DC-DC converter are summarized in Table 1.

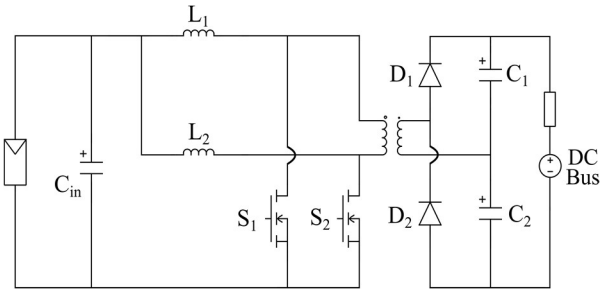

Fig. 2. Topology of an isolated interleaved boost converter.

Table 1
Parameters of the interleaved isolated boost converter

Component	Type	Value
Input capacitor C_{in}	KEMET C475M1R2C7186	100 V 5 x 4.7 µF
MOSFET S_1, S_2	TOSHIBA TPH3R70APL	100 V R_{on} = 3.1 mΩ
Inductor L_1, L_2	BOURNS SRP2313AA-470M	14 A 47 µH
Diode D_1, D_2	ST STTH12R06	600 V V_f = 1.4 V
Output capacitor C_1, C_2	EPCOS B32672P5105K000	520 V 4 x 1 µF

A PV module of KC200GT from Kyocera Solar is adopted as the input. It is based on the single-diode model, considering the temperature-dependent

behaviour, as described in [14]. Nevertheless, this input can be interchanged by more advanced PV module models that can include the effect of shading etc. [15]. An internal current control loop was designed with a proportional gain K_p of 0.015 and an integral gain K_i of 102.2. The reference for the PI current controller comes from an MPPT Perturb and observe (P&O) algorithm that runs at a simulated frequency of 300 Hz.

3.2 Thermal model

The thermal model is based on several assumptions regarding geometry, boundary conditions for temperature and heat transfer [16, 17]. Firstly, the converter is soldered on a printed circuit board (PCB) consisting of FR-4 material with the following dimensions: 150 x 100 x 1.6 mm. This PCB is mounted in a 3-mm thick plexiglass box of 150 x 100 x 30 mm. The component exchanges heat through the thermal vias of the PCB (conductive) [18] and through the internal air (convective). Moreover, it is assumed that both mediums have a uniform temperature throughout their respective volumes. A lumped thermal network, shown in Fig. 3, which excludes thermal capacitances, is used in order to eliminate transients and acquire the steady state with minimal computation time.

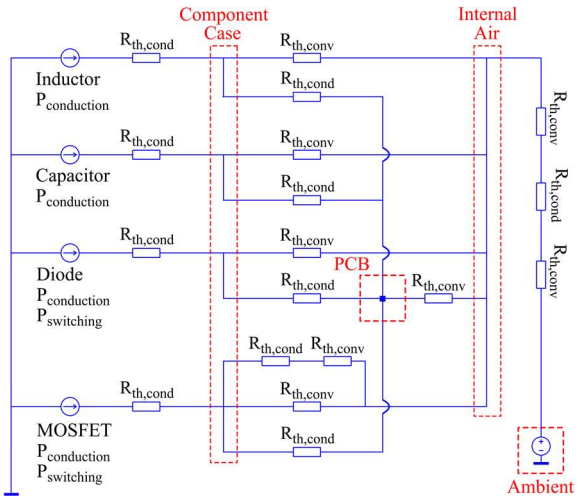

Fig. 3. Lumped thermal network for every component type used in the interleaved boost converter.

The conductive thermal resistance $R_{th,cond}$ is either calculated by using the thermal conductivity of the material or extracted from the component datasheet. The convective thermal resistance $R_{th,conv}$ is calculated using the heat transfer coefficient of still air which has been over-dimensioned from the generally accepted value of 10 W/m^{2}K to 11 W/m^{2}K to include radiative heat transfer effects [18]. Notably, the temperature-dependent or the degradation-dependent behaviour of these values is currently not integrated into the model. Table 2 displays the respective thermal resistances calculated or extracted from the datasheet for every component's conductive and convective path as well as for the PCB and the housing.

Table 2
Thermal resistances for the heat transfer of the converter's components, PCB and housing calculated (c) from material parameters or extracted (e) from the respective datasheets

Thermal resistance	Value	Unit
MOSFET Junction to Case (e)	0.88	K/W
MOSFET Case to Internal Air (e)	49	K/W
MOSFET Case to Heat Sink (c)	1	K/W
MOSFET Heat Sink to Internal Air (e)	4	K/W
Rectifier Junction to Case (e)	1.7	K/W
Rectifier Case to Internal Air (c)	259	K/W
Inductor Core to Case (c)	1.2	K/W
Inductor Case to Internal Air (c)	56	K/W
Capacitor Hotspot to Case (c)	3.3	K/W
Capacitor Case to Internal Air (c)	254	K/W
Component to PCB (16 Vias) (c)	16.3	K/W
PCB to Internal Air (c)	3.3	K/W
Internal Air to Housing (c)	2	K/W
Housing to Ambient (c)	2.4	K/W

The heat exchanged in the thermal network is mainly generated by the conduction losses in the parasitic resistances of the converter components. These include the inductor DC resistance (DCR), the capacitor equivalent series resistance (ESR), the rectifier on-resistance (R_{on}) and the MOSFET drain-source on-resistance ($R_{(ds)on}$). The latter two also generate heat in the form of switching losses, which have been calculated according to [19, 20] with the rise and fall time of the MOSFET being t_{rise} and t_{fall}, and the reverse recovery charge Q_{rr} of the rectifier.

3.3 Electro-thermal coupling

As discussed previously, the heat from the converter is generated by the electrical losses of its components from either switching or conduction through their parasitic resistances. The on-state resistances have, for the switching devices, the functionality in PLECS to be temperature-dependent in the thermal domain. It means that their values will change according to the corresponding component junction temperature. However, this functionality

currently works only in one direction meaning that the electrical behaviour remains unaffected when a component temperature changes. This can be implemented manually in PLECS by using a thermal feedback loop, as shown in Fig. 4. The component temperature is measured and sent into a 1-D lookup table that contains its parasitic resistance temperature-dependent behaviour. The resistance value is then interpolated or extrapolated and sent to a variable series resistor. These feedback loops have been used for the conduction losses of every component and are evaluated for every switching period. The converter capacitances and inductances can also be made temperature-dependent using the same methodology but a sensitivity analysis should be performed first to estimate their impact on the converter performance and the model computation time.

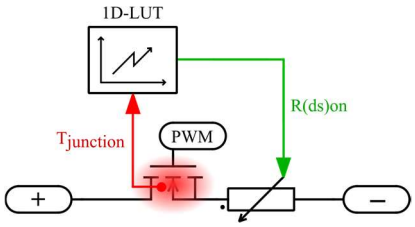

Fig. 4. Thermal feedback loop for a MOSFET on-state resistance in PLECS.

4. Steady state DC-DC converter lookup table

The electro-thermal model is then used to generate a lookup table in Simulink containing various component temperatures, voltages, currents and losses which can serve as boundary conditions in (sub)component degradation models. This lookup table approach reduces the computation time when considering a long-term mission profile but disables the implementation of parameter degradation.

One-year mission profiles from Denmark and Arizona, as shown in Fig. 5, with a sampling rate of 5-min/sample are used as the input for the reliability assessment. It is then translated to the temperature of the converter PCB, internal air and MOSFET case temperature, of which the latter is shown for both mission profiles in Fig. 5c and Fig. 5d, respectively. The temperature profiles will then form the boundary conditions of the finite element MOSFET model.

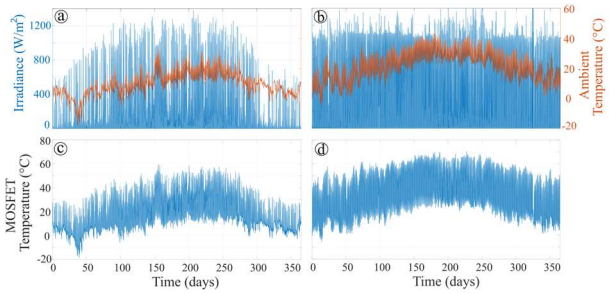

Fig. 5. Loading of the converter: one-year mission profile of (a) Denmark and (b) Arizona, and the MOSFET case temperature of (c) Denmark and (d) Arizona.

5. Finite elements MOSFET solder joint model

5.1 Model structure

The finite element COMSOL model of the MOSFET, based on a commercial device, is shown in Fig. 6. As mentioned previously, the MOSFET is placed on a 1.6-mm thick PCB consisting of FR-4 material and 16 copper thermal vias with a parasitic air layer in-between. The case is made of an epoxy resin with the bottom part consisting of a copper conduction pad. The leads are made of aluminium and are soldered to the PCB copper conduction paths with 60Sn-40Pb solder material. As seen in Fig. 6, only a quarter of the MOSFET is modelled, as two symmetry planes are introduced to reduce the computation time.

The resultant thermal profiles are used to simulate the effect of the converter housing and the surrounding components on the solder joint. Every connecting surface in the model is transferring heat conductively while every open surface of the model can transfer heat both convectively and radiatively. It was decided not to model the MOSFET silicon die and bond wires, as the thermal resistance to the case was already available from its datasheet and used in the electro-thermal model.

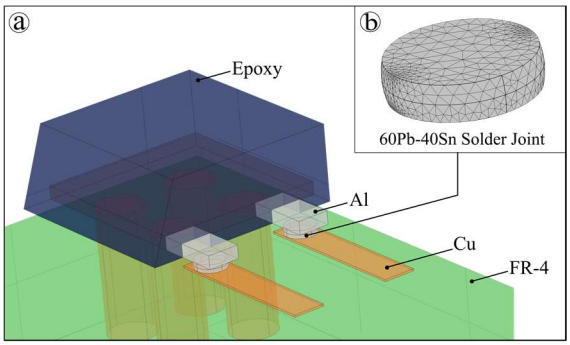

Fig. 6. Finite element MOSFET model in COMSOL.

5.2 Fatigue modelling

A local stress profile is acquired after performing a time-dependent study of the FEM model consisting of the combined influence of the temperature profiles of the internal air, the PCB and the MOSFET case on the thermal expansion of the solder joint. This profile will be used as an input for a fatigue study that calculates the total damage induced on the solder joint by the mission profile. This study utilizes the COMSOL fatigue module, which includes several damage models. For mission profiles consisting of cycles with different amplitudes and mean values, the rainflow counting algorithm [20] [21] is used [22] to count the total amount of stress cycles that occur on the solder joint during the one-year mission profile with their respective amplitudes, mean values and durations. Afterwards, the tool utilizes the solder material S-N curve, which represents the relation of a certain stress cycle amplitude with the number of cycles to failure, to calculate the damage per cycle. This S-N curve was obtained from [23]. Notably, the degradation-dependent behaviour is not included in the material constitutive model for efficient computation. Lastly, the calculated damage is accumulated following the Palmgren-Miner rule [24], which gives the amount of lifetime (in percentage) consumed during the one-year profiles.

5.3 Results

According to the results in Fig. 7, the amount of lifetime consumed by the one-year profiles on the solder joint, as depicted in Fig. 6b, can be evaluated considering its geometry. A maximum lifetime consumption surface value of 11% in Fig. 7a and 23% in Fig. 7b is observed. These surfaces and their values indicate the location and the time required for crack initiation in the solder joints of the MOSFET after being stressed by the mission profiles of Denmark and Arizona, respectively. In that case, the lifetime can be extrapolated to 9.1 and 4.3 years, respectively. A crack propagation model is required in order to determine the remaining useful lifetime of the entire solder joint but this falls out of the scope of this paper. It should be noted that the stress created due to the CTE mismatch in the solder material is dependent on the geometry incorporated in the model. Discrete jumps in geometry can lead to overestimations of the local principal stress which in turn will affect the S-N curve input. The final step of the methodology is therefore dependent on the combination of the chosen S-N curve, which depends on the geometry and the dimensions of the solder joint model. The latter is not always provided which can lead to unrepresentative lifetime. In future work, a more accurate result can be acquired by optimizing the mesh and the geometry of the solder joint to more closely resemble the practical S-N curve. This will also significantly increase the computation time of the model. Alternatively, an S-N curve can be experimentally measured for a certain type and size of solder joint but this can become very time consuming. Alternative lifetime models to translate the local stress profile to the amount of lifetime consumed will be evaluated in future publications.

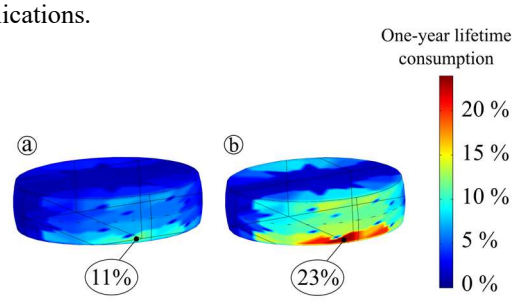

Fig. 7. One-year lifetime consumption surface plot of a 60Sn-40Pb solder joint from a MOSFET in (a) Denmark and (b) Arizona.

6. Conclusion

The reliability analysis framework has been demonstrated on an isolated interleaved boost converter designed for BIPV applications in this paper. An electro-thermal model in PLECS and a finite element fatigue model in COMSOL were used to investigate the influence of two yearly mission profiles on the degradation of the MOSFET solder joint. The resulting time for crack initiation in this solder joint was 9.1 and 4.3 years for the mission profiles of Denmark and Arizona, respectively. However, the obtained results are dependent on the combination of the chosen S-N curve and the geometry of the modelled solder joint. Future work will include obtaining experimental results to validate the framework and exploring alternative lifetime models in order to better translate the local stress profile to the amount of lifetime consumed.

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