Practical Considerations for Designing Reliable DC/DC Converters, Applied to a BIPV Case

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Abstract: State-of-the-art reliability assessment typically starts from a given circuit topology, for which the most suitable components are selected using a Physics of Failure analysis. This paper, however, addresses the topology selection stage, which is the foundation in designing reliable converters. Based on an overview of the reliability performance of different components, a methodology is presented as a guideline for comparing topologies to one another. The focus is directed at practical consequences associated with certain designs. Furthermore, an overview is provided on the latest developments in component technology reliability improvements. The developed methodology is mainly intended for demanding applications, where long lifetimes are required or elevated ambient temperatures are present. After the topology selection, an overview of possibilities is given that allows further increasing converter availability. Finally, the methodology is applied to the design of module level converters for building integrated photovoltaics, which is a high temperature application with a high desired lifetime. A prototype and experimental results are presented.

Keywords: PV; BIPV; LVDC; DC/DC module-level converters

1. Introduction

Reliability in power electronics applications is a subject with growing interest. In the past, converter reliability was calculated using black box reliability models, assuming constant failure rates [1–4]. One of the most popular standards for this was the American Military Standard MIL217-F [5] but other industrial standards such as Telcordia SR-332 [6] and Siemens SN29500 exist as well. The large discrepancy between calculated and actual lifetime, estimated from field returns, has turned research towards the Design for Reliability (DfR) approach [7–10], based on Physics of Failure (PoF) models. Furthermore, handbook models such as MIL217-F have been discontinued and are thus not applicable for new components and new packages, e.g., for emerging technologies such as GaN and SiC transistors.

One could say that handbook-based modeling is an engineering approach to the reliability problem. The problem is highly simplified by assuming a constant failure rate, which is extrapolated from accelerated stress tests. The failure rate calculations were straightforward and relatively easy, although lacking in accuracy. In contrast, DfR is an iterative design process which employs PoF models that deliver more reliable results for specific failure mechanisms as they are based on constitutive material models [11]. However, the computation of the simulations is often high as it requires detailed material models and dimensions of the used components. Furthermore, an estimate of a relevant mission profile is needed.

The reliability of the entire converter system is estimated by modeling and comparing specific failure mechanisms of the most failure-sensitive components, which mostly are the active switches and the capacitors [12–15]. In order to simulate these failure mechanisms accurately in the system, the appropriate thermal boundary conditions for the PoF models need to be determined for a specific mission profile. This includes the electro-thermal modeling of the PCB with its components and housing. The accuracy of the thermal part greatly depends on the conductive, convective and radiative thermal resistances of every component which can either be extracted from the respective datasheets or calculated. The accuracy of the electrical part depends on the implementation of parasitics such as the equivalent series resistance or insulation resistance of a capacitor. All of these parameters can additionally be varied with temperature or degrade in time, making the accuracy of the electro-thermal modeling as important as the accuracy of the constitutive material models used in the PoF models [16].

Even in DfR guided designs, the circuit topology selection is mainly driven by cost and efficiency of the considered solutions. Reliability is only considered afterwards and this puts restrictions on the actual implementation, such as the used components or the cooling performance. For applications that are demanding in terms of lifetime or intended to work at elevated temperatures, we propose prioritizing reliability above costs and efficiency when selecting a circuit topology. This topology selection is mainly of interest for DC/DC applications, as circuit designers have the freedom to choose from a variety of topologies such as buck, boost, buck-boost, cúk, zeta, flyback, forward, push-pull, half bridge and full bridge converters and their derivatives. In contrast, for DC/AC applications, the preferred and most commonly used circuit topology for motor drives is a voltage-fed three-phase inverter of which the design is never questioned.

From the large choice of DC/DC converters, a power electronics designer might find it difficult to single out the most reliable topology for a specific application. The correct answer can be found in a DfR approach, as mentioned above, evaluated for all different topologies. On a practical note, this is a cumbersome task that requires the design of multiple converters, with the appropriate components for every topology. Assuming that the engineer possesses the necessary PoF models and that the mission profile includes all of the relevant component information, this task might take several weeks or months for completion. By then, no converter has actually been built or experimentally tested.

This paper provides insights in converter selection for demanding applications by providing a heuristic methodology that highlights the consequences of certain design choices. The purpose is threefold: First, an overview of state of the art technology solutions for reliability improvement are given. Second, based on typical reliability problems that arise in the field, a set of guidelines is presented that can be used for a quick selection of a converter topology. Third, specific design choices that further improve reliability are given. The purpose of the paper is not to replace the PoF approach but to help designers in the correct selection of converter topologies by providing an overview of practical design considerations. After selecting a circuit topology, it is still required to estimate the lifetime using PoF models of the most critical components.

The methodology is of main interest for applications with high temperatures and limited cooling possibilities that can be found in for example the oil and gas industry or automotive applications. Also mission-critical applications, where repair or maintenance is difficult or undesired and that require a

long lifetime, are envisioned. These can for example be found in aerospace but also on earth in façade Building Integrated PhotoVoltaics (BIPV) applications. BIPV is an interesting technology to reduce the net energy demand of high-rise buildings, where the amount of roof surface is too small to place regular PV modules. The façade can then be used to place PV modules to become a distributed generator. In BIPV, converters are integrated in the framework of a building façade and no maintenance or repair can be done without dismantling the façade [17,18]. The converters have to remain in place and functional for a period of at least 25 years and preferably even longer. In this paper, the methodology will be applied to BIPV Module-Level Converters (MLCs).

The paper is structured as follows: In Section 2 the reliability concerns of individual components are listed, guided by illustrative examples of state-of-the-art components. Section 3 presents other possibilities to further increase converter availability. Section 4 develops a heuristic, practically useful methodology for topology assessment and component selection. Section 5 discusses the BIPV case and presents an experimental prototype and Section 6 formulates the conclusions.

2. Reliability Criteria for Topology Assessment

Reliability is only one aspect of a converter design and its importance needs to be weighted against other criteria such as cost, efficiency and power density of the converters. The purpose of this section is to provide guidelines in order to select reliable converter topologies for a certain application. As every circuit topology is essentially made of transistors, diodes, capacitors and inductors, the starting point is the reliability of those building blocks. In [19], a similar high reliability design approach was proposed: Minimize the system complexity, minimize the stress level and select the best available materials. However, in high temperature applications, minimizing the temperature stress can be very challenging when no active cooling is considered.

2.1. Lowest Component Count

From a reliability perspective, a power electronics circuit can be seen as a series reliability block diagram. One component failure will inevitably lead to a converter failure. The special case of redundant converters, which can be seen as a combination of series and parallel blocks, is treated in Section 3.1. A circuit with fewer components is inherently more reliable and this applies to both the power stage as the signal stage.

An interesting evolution is depicted in Figure 1 where the evolution of driver circuits is presented. In the past, a driver was a circuit that was completely consisting of discrete components, such as the example shown in Figure 1a. Presently, several companies offer commercial driver ICs, Figure 1b, with extra functionalities such as under-voltage lockout, desaturation protection and shoot-through protection (in case of half bridge gate drivers). Furthermore, only a minimum amount of external components is required. This also reduces the total amount of solder joints, which can be a reason of concern in high temperature applications, for example BIPV [16]. A recent development which is taking place for GaN transistors is the integration of the driver together with the switch in the same package, see Figure 1c. This is mainly to reduce the parasitic inductance in the drive loop which ensures minimal overshoot at maximum switching speed, such that the full potential of GaN can be achieved. This evolution is not only beneficial to reduce the total amount of components, solder joints and costs but also to further reduce the chance of design errors.

Most driver ICs have galvanic isolation between the signal (input) and power (output) stage. The isolation barrier can be achieved in an optical, inductive or capacitive manner. Long-term reliability problems have been reported in the literature for optical isolators, due to degradation of the LED [20–22]. High junction temperatures inside the LED optocoupler lead to a decrease of the diffusion current,

which determines the light output. The reduction of the LED luminous efficiency leads to a decrease of the Current Transfer Ratio (CTR) and eventually optocoupler failure [20]. Commercial driver manufacturers have turned to the use of inductive [23] or capacitive isolation technologies [24,25] to overcome this issue.
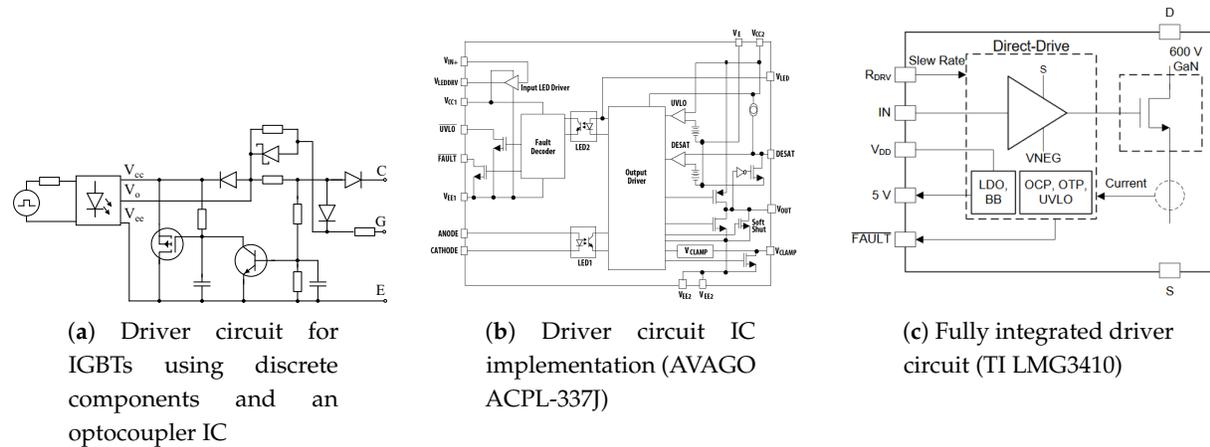

(**a**) Driver circuit for IGBTs using discrete components and an optocoupler IC

(**b**) Driver circuit IC implementation (AVAGO ACPL-337J)

(**c**) Fully integrated driver circuit (TI LMG3410)

Figure 1. Several examples of integrated and non-integrated driver circuits.

2.2. Transistors and Diodes

Transistors such as MOSFETs or IGBTs are controllable by applying a voltage to the gate. Diodes, in contrast, are non-controllable switches. Their state is a consequence of external circuit conditions, which makes them forward (on) or reverse (off) biased. In general, a diode can be replaced by an active switch. In DC/DC converters using unipolar devices (e.g., MOSFETs), this is typically done to decrease conduction losses, as the voltage drop across the device is purely resistive. However beneficial from an efficiency perspective, an active switch also introduces additional gate drivers. Furthermore, floating power supplies are required when the switch is not referenced to ground. This trade-off was already highlighted in [26], where it was shown that a diode is preferred over a switch in boost converters from a reliability perspective although the synchronous boost is preferred from an efficiency perspective.

From a reliability point-of-view, the switches and their gate drivers are one of the components that fail most frequently [27,28].

Bond wire lift-off as a consequence of thermal cycling is reported as a major problem for IGBTs [29]. PoF models which are based on a single failure mechanism such as solder joint or bond wire degradation in IGBTs are still mainly constructed empirically. The most common approach is based on a combination of finite elements modeling in parallel with accelerated stress testing. The boundary conditions of the stress test are mimicked in a finite elements model of the component in question which then calculates the amount of creep deformation in the solder joint or the amount of energy dissipated in the bond wires. These simulated damage parameters are then linked to the amount of cycles to failure obtained from their respective accelerated stress test. This approach is performed on various accelerated stress levels and can thereafter be fit into a lifetime model for the studied failure mechanism [30]. Widely known examples of such models are Darveaux for the amount of dissipated energy in Ball Grid Arrays (BGA) and Norris–Landzberg for the amount of plastic strain in solder joint interconnects [31,32]. These models can be referred to as grey box models due to their link with the PoF of one particular failure mechanism, such as a white box model, while still being derived empirically from a large data set of a single component. They tend to require minimal computation time and are typically used for mission profile-based lifetime estimations using a combination of rainflow counting and Miner's rule [33,34].

Direct copper clip bonding was presented as an alternative to traditional bond wire interconnects [35]. This technology allows to reduce the electrical parasitics and decreases the package thermal resistance. Also packages with double sided cooling are easier to produce. In [36], the thermal resistance of a SiC power module was halved and improved reliability figures were obtained by applying copper clip interconnects. For GaN transistors, packages exist that avoid the use of bond wires completely [37]. This is an interesting evolution as it avoids one of the typical dominant failure modes in transistor packages.

2.3. Capacitors

Next to switches, capacitors are one of the components that are prone to failure in power electronics applications. For high temperature applications, it is stated as the most troublesome component [38]. An excellent overview of the reliability aspects of DC link capacitors is given in [39]. Within this subsection, DC link capacitors that are mainly used as energy buffer, are considered. In Section 2.5, capacitors for resonant applications, that typically experience higher current stress, are treated.

Compared to switches, the maximum operating temperature of capacitors is fairly low. This might be problematic for high temperature applications, excluding specific capacitor types. Aluminum (Al) electrolytic capacitors for example have a typical maximum operating temperatures of 85 up to 105 °C and a maximum voltage rating up to 750 V. When the operating temperature is close to this limit, the lifetime will decrease drastically due to electrolyte evaporation. This is considered the main wear-out mechanism and is strongly accelerated by high temperatures. It was also found that the wear-out of Al electrolytic capacitors is not strongly affected by voltage, as long as this is within the allowed operation limit [40]. This means that designing with a large voltage tolerance is not very effective to increase the component lifetime. A possible solution to the evaporation problem can be found in polymer Al electrolytic capacitors where the liquid electrolyte is replaced by a solid polymer, thereby removing the problem of evaporation [41]. Furthermore, a lower ESR can be obtained which also increases their ripple current capability [42]. Currently, industrial grade polymer electrolytic capacitors are available with working temperatures up to 150 °C but the voltage level is limited to 125 V.

Industrial grade Multi Layer Ceramic Capacitors (MLCCs) and film capacitors can reach temperatures up to 200 °C and 150 °C respectively. Capacitors optimized for placement in high temperature environments such as subterranean drilling, avionics, and automotive received more attention over recent years. Operating temperatures for Tantalum (Ta) electrolytic capacitors have increased past the 200 °C mark [43] and Highly Accelerated Lifetime or Stress Testing (HALT/HAST) of traditional, C0G/NP0 and X7R MLCC type capacitors, have increased conditions up to 300 °C [44]. It must be noted that the lifetime expectancy of capacitors placed in these type of conditions is severely lower that what can be expected compared to consumer product implementations.

MLCCs present excellent reliability figures that make them useful for high reliability, such as space applications [45,46]. Although the problem of MLCC cracking due to vibrations, PCB bending and Coefficient of Thermal Expansion (CTE) mismatch has been recognized. Several techniques are proposed to circumvent this problem. MLCCs exist in packages with J-leads [47], flexible terminations [48] or open mode designs [49]. The first two relieve mechanical stresses in the ceramic material, which is the root cause of the cracks. The latter tries to avoid the short-circuit failure mode, which is the consequence of the cracks. All three options lead to an increased component cost. Open mode designs also have a reduced capacitance due to the lower useful surface. Besides cracking, a designer also needs to take into account problems related to capacitance variations. The nominal capacitance as given in the datasheet and the actual capacitance can differ strongly. Three main effects are typically taken into account: aging, DC or AC bias and temperature. Class 1 MLCCs such as C0G or NP0 do not suffer from aging or voltage bias [50]. Their temperature coefficient is around 0 ± 30 ppm/K, leading to a very stable capacitance from -55 up

to 125 °C [51]. However, class 2 MLCCs such as X5R or X7R are more prone to capacitance variations but they are often employed due to their high energy density. In [52], the above effects were investigated for X7R MLCCs and it was highlighted that the DC bias effect is more significant compared to the applied temperature. The reported capacitance reduction was reduced by 80% when 80% of the nominal voltage was applied. Furthermore, a reduced efficiency of 2.4% was reported when comparing the performance at 10 and 1000 h.

Metallized film capacitors can be designed with a variety of dielectric films and this will affect not only the electric performance but also the useful temperature operating range. Mostly PolyEthylene Terphtalate (PET) or PolyPropylene (PP) are used. They both have a typical operating temperature up to 100 °C. From an electrical perspective, PP has superior characteristics in terms of capacitance change with temperature and dissipation factor. PET in contrast has a higher dielectric constant (ϵ_r) which leads to a higher capacitance per volume. When higher operating temperatures are required, PolyEthylene Napthalene (PEN) or PolyPropylene Sulfide (PPS) are used with respective operating temperatures up to 125 °C and 140 °C. The distinct advantages of metallized film capacitors are the dominant open mode failure and the self-healing capability [39]. The open mode failure is typically a consequence of a reduced capacitance by consecutive self-healing processes and referred to as a soft failure [40]. The self-healing process is in fact a localized electric breakdown in the film that is automatically cleared by evaporation due to the large temperature increase [53]. Although temperature stresses degrade the performance and induce degradation by CTE mismatch, aging is mostly induced by the applied voltage stress, and more specifically by the applied peak voltage [54]. As a consequence and in contrast to electrolytic capacitors, it is very useful to provide enough margin between the applied voltage and the maximum capacitor voltage to increase the operational lifetime of film capacitors.

When a large DC link capacitance is required, multiple capacitors are placed in parallel. This reduces the equivalent ESR of the capacitor bank and spreads the losses over multiple components, thereby limiting the temperature rise per component. Depending on the application one must take care that the high frequency behaviour of the individual capacitors in the bank does not cause unwanted resonances due to their own oscillation frequencies which could be triggered by various reasons. A practical approach is to make sure all capacitors placed in a bank are of the same type, value and vendor. However, combining different technologies might be necessary from a cost or power density perspective. When this occurs, one needs to keep in mind that not all capacitors have the same dominant failure mode. Al electrolytic and MLCCs tend to fail in a short-circuit mode, whereas the dominant failure mode of film capacitors is an open-circuit due to decreasing capacitance [39]. The short-circuit failure mode is more troublesome as it leads to an immediate failure whereas open-circuit failures lead to a decreased performance.

In conclusion, capacitors are unavoidable but also troublesome components in high temperature applications. Manufacturers are aware of the reliability issues and have reached out with several new materials and solutions that increase the performance of their products, although at an increased cost. For high temperature applications, it is advised to keep the amount of capacitors to a minimum. Converters that rely heavily on capacitor circuits such as switched capacitor topologies [55] or capacitive voltage multiplier cells [56] are not preferred.

2.4. Inductors and Transformers

From field experience, inductors and transformers are seen as very reliable components. Only a few papers have investigated failure causes and the expected lifetime [57]. Most problems are related to cracking, to which mainly ferrites (in essence a ceramic material) are prone. Inductors and transformers are relatively heavy parts on a PCB. Vibration can be a major stressor for these parts. Component size needs to be taken into account for certain applications such as launch electronics in aerospace or drilling

applications in the oil and gas industry as the vulnerability to cracking increases with size. Extra brackets that fix the inductors to the PCB might be required to alter the stiffness of the system. Limited form factors can trigger new ways of implementation such as Rigid-Flex PCB designs [58].

From a temperature perspective, inductor cores exhibit stable electrical properties up to the Curie temperature (T_C) which is in the range of 400 up to 700 °C for powder core materials and 135 up to 300 °C for ferrites. Although T_C is much higher for powder cores, the limitation is found to be the used binder and the epoxy coating material that allow temperatures up to 150 up to 200 °C. This limit can however be extended when the inductors are potted in specific compounds [59]. Furthermore, when the core is exposed continuously to high temperatures, e.g., above 105 °C, thermal aging can occur in the form of increased core losses for powder cores. This is a consequence of a reduced resistance of the electrical insulation between the powder particles, leading to more eddy currents [60].

2.5. Soft Switching

The use of Soft Switching (SS) in power electronics is popular because it is an effective method to simultaneously reduce switching losses and ElectroMagnetic Interference (EMI). By the reduction in switching losses, a higher efficiency can be achieved or the switching frequency can be increased to improve the power density.

Resonant circuits such as the LLC converter are often used in industry. Due to an LC resonance, the current and voltage are phase-shifted and SS can be achieved. In [61], a survey was performed showing that mainly the switches and the resonant capacitor tend to fail. The resonant capacitor (C_r) has to carry the entire input current. Therefore, PET/PP film capacitors are typically used because of their low dissipation factor (tan δ) and capacitance stability over a wide frequency range. As discussed under Section 2.3, capacitor lifetime quickly decreases for increasing temperature. For converters with high input currents and high ambient temperatures, sufficient cooling is required to limit the internal capacitor temperature increase. When sufficient cooling cannot be guaranteed, resonant converters should be avoided. As an alternative, a phase-shifted full bridge can be used where the SS is achieved by means of the MOSFET output capacitance (C_{oss}). The advantage is that no extra capacitor is required.

Another class of SS converters are Zero Voltage or Zero Current Transition (ZVT/ZCT) converters. Their working principle is inherently different to LLC converters since an external circuit is triggered that causes a ZVT/ZCT of the main switch. Multiple examples can be found in the literature of which one is depicted in Figure 2 [62]. Note the large amount of components that is introduced to reduce the losses of the main switch, including an auxiliary switch. The increased cost of the extra components can be countered by the use of a smaller heatsink. However, when the cooling mechanism of the main switch is designed for SS operation and one of the components in the ZVT circuit fails, the converter will fail due to an overtemperature of the main switch. Therefore, it is not recommended to rely solely on ZVT/ZCT circuits for safe operation in high temperature applications.
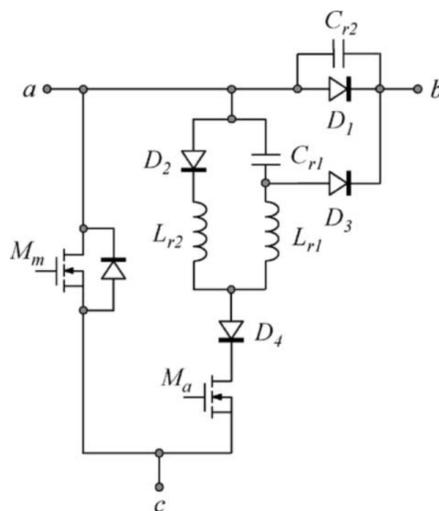
Figure 2. Example of a ZVT network added to a converter [62].

3. Methods to Further Improve Reliability and Availability

In the previous section, an overview of key aspects was provided for topology selection. In this section, several solutions are presented to further improve converter reliability and availability.

3.1. Redundancy

Redundancy is an interesting means of increasing system reliability. In general, the major drawback of redundancy is the increased cost due to the increased component count. Furthermore, the control becomes more complex.

A well-known example is shown in Figure 3. One diode can be implemented as a series/parallel combination of four diodes. In this configuration, both an open-circuit failure and a short-circuit failure are tolerated and require no additional control circuits. Please note that this solution doubles the forward voltage drop, thus leading to a double amount of losses. The current under normal operating conditions is halved but the diodes and their cooling need to be dimensioned for the full load current such that one branch can take over in case of a failure. The price increases fourfold compared to a one diode solution.

Another option, highlighted in Figure 4, is the use of a redundant power supply. The output voltage of sources $V_{aux,1}$ and $V_{aux,2}$ differ by a small amount. In regular operation, $V_{aux,1}$ supplies the load R via diode D_1. In case of a failure in $V_{aux,1}$, the voltage will drop and $V_{aux,2}$ will automatically take over. This redundant power supply can for example be used to power the gate drivers or the signal section of the converter. This is again an example of automatic redundancy.

A third possibility to include redundancy in the system, is by parallel connection of multiple converters. In larger systems such as EV charging stations and datacenters, this is already common practice and the converters are hot swappable, meaning that failed converters can be replaced during operation [63]. In smaller systems, the parallel legs can be implemented on a single PCB and interleaved to reduce the current ripple. In [64], the case of a two- and a three-stage interleaved boost converter was examined. Because the losses are spread over multiple components, the temperature increase per component is lower which results in a longer lifetime. The calculated MTTF (Mean Time To Failure) increased from 9.8 to 14.8 years for the two-, respectively three-stage design. Another advantage is that the converter can remain operational under reduced load when one of the components fails in open mode.
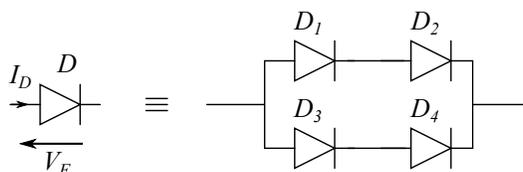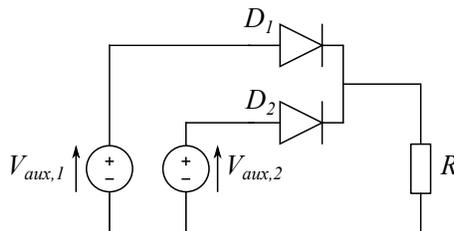
Figure 3. Redudant diode.

Figure 4. Back-up power supply using a diode OR function.

3.2. Standardized Parts

Central advise and mission organs in both space and the automotive industry have compiled a list of known-good components for various applications of electronic circuits. The European Preferred Part List (EPPL) [65] is an extensive list of parts that can be used as a guideline for projects at the European Space Agency (ESA). The list consist of MOSFETs and diodes as well as passives, micro-controllers and other hardware that is qualified by ESA to be used on missions. The AEC-Q100, AEC-Q101 and AEC-Q200 specify a stress test qualification for respectively integrated, discrete and passive components in the automotive industry. These qualifications can also be used when choosing components in designs requiring a long lifetime. A practising engineer can use these libraries to his or her benefits and is advised to keep an own reference list of known-good components for future use.

3.3. Control

Although the primary interest of this paper is on hardware related aspects of reliability, the importance of the software layer cannot be neglected. Active thermal control can be an effective method of reducing or controlling the amplitude of temperature cycles that components experience. It goes beyond the scope of this paper to provide a detailed analysis and the authors would like to refer to [66] for further information on this topic.

4. Methodology

Based on the discussions in the previous sections, a heuristic methodology will be presented in this section. Note the use of the term heuristic: In Section 1, it was already stated that the most reliable solution can only be found by evaluating every suitable topology using a PoF based reliability calculation. Given the large choice of available DC/DC converter topologies, this is a cumbersome task. To speed up this process, guidelines are presented in this section that can help circuit designers in selecting topologies.

To extend the capabilities of traditional power electronics converters, a clear trend is visible towards topologies that implement more switches and capacitors to achieve higher power densities compared to traditional designs that rely on magnetics [67]. Numerous examples can be found in high step-down converters [68–70], high step-up converters [56,71,72] and PV or wind power inverters [73–76].

From a reliability perspective, capacitors and switches are also the components that fail most often. In applications where a very long lifetime is envisioned in combination with a high thermal loading, those topologies are thus not the optimal choice.

The flowchart that is presented in this paper is shown in Figure 5. Starting from a given application, it is important to first specify the requirements in terms of cost, efficiency, size and reliability.

Based on the requirements, an initial converter design can be made by choosing a topology. This initial design step is typically not mentioned or not elaborated on in existing literature [77], although it is a crucial element in the DfR process.
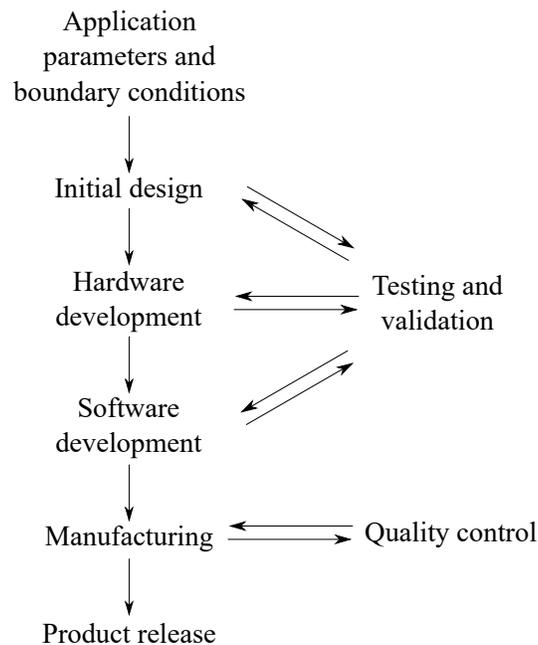
Figure 5. Heuristic methodology flowchart for the development of reliable converters.

To choose a reliable topology for long lifetime - high temperature applications, it is suggested to take the following guidelines into account:

- Use topologies with a minimal amount of components. Not only the component itself can fail but also the solder joints might crack after severe thermal loading.
- Use topologies with a minimal amount of active switches and avoid replacing passive switches with active ones. Preferably use active switches that do not require a floating power supply as this further increases the component count and circuit complexity.
- Avoid the use of topologies with resonant capacitors to allow SS. The high currents that flow through the capacitor will lead to a strong thermal loading. Make preferrably use of the parasitic capacitance of the components, such as the C_{oss}. Also ZVT/ZCT circuits need to be avoided as they strongly increase component count and complexity.
- Avoid to rely on ZVT/ZCT circuits in order to decrease the heat sink size.
- Inductor- or transformer-based topologies are preferred over capacitor-based designs due to their inherent robustness at high temperatures.

Based on the above set of guidelines, one or multiple topologies can be selected for further evaluation. The next step in Figure 5 relates to the hardware development. The state-of-the-art reliability aspects of power components were highlighted throughout Section 2. The main conclusions are repeated here for completion:

- Choose a gate driver IC that requires a minimum of external components and does not use optical isolation. Consider the combined use of a driver with transistor to further reduce the amount of solder joints and the possibility of design errors.
- Active rectification, where diodes are replaced by transistors, is an interesting means to boost effciency. When evaluating the reliability of both solutions, the extra gate driver, isolated power supply and increased circuit complexity need to be taken into account to make an informed decision.
- Bond wire lift-off due to thermal cycling is one of the major failure mechanisms of transistors. Components exist that employ alternative techniques such as direct copper clip bonding and are preferred in terms of reliability.
- Aluminum electrolytic capacitors need to be avoided in high temperature applications, as the electrolyte evaporates more rapidly, leading to component failure. Alternatives such as MLCCs or film capacitors can be chosen. For MLCCs, preferably components with J-leads, flexible terminations or open mode designs are used to avoid the short-circuit failure mode. For film capacitors, providing sufficient margin on the voltage can further increase their lifetime.
- Inductors and transformers are inherently robust parts from a temperature perspective. Powder cores are preferably avoided when the component operates continuously above 105 °C, as thermal aging can lead to increased core losses over time.
- Avoid to rely on ZVT/ZCT circuits in order to decrease the heat sink size. Design the cooling system with sufficient margin such that, in case of malfunctioning of the SS circuit, the junction temperature does not increase beyond the thermal limit as specified in the datasheet.
- Redundancy can strongly increase converter reliability but also raises the price, and possibly the circuit complexity, considerably.
- Make use of parts that have an automotive (AEC-Qxxx) or space (EPPL) certification.

The next step to further increase reliability, shown in Figure 5, is the development of an adequate software layer. Besides the protection against unexpected events such as overvoltage, overcurrent or overtemperature, which require an immediate shut-down, active thermal control is an intelligent way to reduce the amount or intensity of the temperature cycles that the components undergo. As voltage and current sensors are already available for the primary converter controls, this is a relatively cheap way to boost converter performance in terms of reliability.

Please note that during each step, iterations are required to test and validate the choices. This can be done in typical PoF based DfR methods that are already described in the literature and include a combination of numerical electrical and thermal simulations, hardware and software prototyping, and accelerated stress tests. When the results are satisfactory, the developer can go the manufacturing process. This step requires a specific quality control such that a high reproducability can be obtained before the product is released to the market.

The steps that are described in this heuristic methodology do not intend to replace a PoF based approach, but to give more insight to practising developers in terms of component and topology selection. From that perspective, it serves as an addition to what is already described in the literature.

5. Case Study: BIPV

5.1. BIPV as a Mission-Critical Application

In this section, the methodology to select a reliable converter topology will be applied to façade BIPV Module-Level Converters (MLCs). As a first step in the methodology, the application boundary conditions and electrical requirements are carefully described. BIPV MLCs are integrated in the framework of façade curtain wall elements. An overview of the requirements of BIPV MLCs can be found in [17]. In [18], it was

shown that commercially available MLCs are not optimal for BIPV applications due to a thermal, electrical or dimensional mismatch of the specifications.

Ambient temperatures above 75 °C are expected in combination with a specific form factor that limits the use of large heat sinks. The high temperature is a consequence of the converter being placed in close proximity to the PV panel, and in close proximity to thermal insulation materials. Forced air cooling is not considered as the lifetime of the fan's bearings is too limited.

An operating life of more than 25 years is required, without the possibility to replace or repair the MLC. It is assumed that the MLC is pre-installed in the framework of a curtain wall module and not accessible after installation. The exact amount of operating hours will depend on the amount of sunshine at the site and the orientation of the building. Assuming an average of 8 h a day over 25 years, leads to 73,000 working hours. Compared to the automotive industry, the lifetime of a vehicle is 15 years, and the motor management controller should last 15,000 operating hours [78], being five times less. Moreover, automotive systems are designed in a way that repair is relatively easy, which is difficult in BIPV systems.

The long lifetime is not only very demanding for the power circuit but for the entire converter, including the micro-controller, measurement system and auxiliary power supply. In this paper, the focus is on the choice of the converter topology. Given the desired long lifetime, a topology will be chosen that offers inherently high reliability characteristics.

5.2. Electrical Requirements

The input of the MLC is connected to a PV panel. The voltage rating will depend on the amount of PV cells and can be different in BIPV compared to Building Applied PV (BAPV). In BAPV, 60- or 72-cell Si modules are standard. For this case, a 40-cell module is assumed with voltages ranging from 10...30 V, depending on the irradiance, temperature and possible shading from nearby objects. The maximum input current is assumed to be 10 A. The converter output is connected to a Low-Voltage DC (LVDC) bus of 400 V. The advantage of using a DC instead of an AC bus is that no AC conversion is required, which leads to a reduction in the amount of components and sensors. Furthermore, the large DC bus capacitance that buffers the difference between input and output power, and is typically an electrolytic capacitor, is not required in this case.

5.3. Initial Design—Converter Topology Selection

The boundary conditions and requirements are known and the next step in the methodology is the inital design step, were the developed guidelines of Section 4 can be followed to select a converter topology.

In literature, several circuits have been experimentally investigated that fall into the specifications of the BIPV MLC, and a selection of multiple topologies is given in Table 1. An elaborate overview of non-isolated boost topologies can be found in [67].

Table 1. Overview of possible high step-up BIPV topologies.

Ref.	Topology	Ideal Gain	Input Voltage [V]	Output Voltage [V]	Output Power [W]	Galvanic Isolation	#S	#D	#C	#L
[79]	Boost	$\frac{1}{1-\delta}$	12-36	48	200	No	1	1	2	1
[56]	Boost with VMC	$\frac{3}{1-\delta}$	10-25	120	200	No	2	6	6	2
[55]	3-L EDR boost	$\frac{3}{(1-\delta)}$	20-40	225	250	No	3	3	4	3
[80]	Passive clamp, coupled inductor boost	$\frac{5}{(1-\delta)}$	25-50	400	400	No	1	3	4	2
[81]	Synchronous boost, SR FB	$\frac{2.N}{1-\delta}$	15-45	400	275	Yes	6	2	5	2
[82–84]	Interleaved boost, SR FB	$\frac{2.N}{1-\delta}$	10-40	400	300	Yes	7	7	4	4
[85]	IBIWCI	$\frac{1+N}{(1-\delta)}$	7.2-110	80-140	100	No	2	4	2	1
[86]	Current-Fed Push-Pull	$\frac{2.N}{(1-\delta)}$	20-50	400	250	Yes	2	2	4	1
[87,88]	IIBC	$\frac{2.N}{(1-\delta)}$	20-50	200	200	Yes	2	4	2	2

SRFB: Series Resonant Full Bridge, VMC: Voltage Multiplier Cell, IIBC: Isolated Interleaved Boost Converter; 3-L EDR: Three-Level Extended Duty Ratio, IBIWCI: Interleaved Boost with Integrated Winding Coupled Inductor.

The normal boost converter is an interesting circuit as it uses a minimal amount of components and it can be easily controlled by well-established methods. Interleaving this topology with additional redundancy is also fairly straightforward. The required voltage gain for this application varies from 13.33 to 40. From a practical perspective, the maximum gain of a normal boost is however limited to about 5 [89], which excludes the normal boost from our selection.

To increase the gain of the boost, several solutions have been proposed in the literature. For example capacitor-diode Voltage Multiplier Cells (VMCs), as reported by [56]. A gain of 12 can be reached by implementing two VMCs. For higher gains, the amount of components quickly increases, as does the complexity of the current controller [90]. Other extensions to the non-isolated boost are the 3 Level Extended Duty Ratio (3L-EDR) [55] and the passive clamp coupled inductor boost [80]. Those circuits were not selected as they make use of additional capacitors for soft switching, which are placed in the main power path and have to carry a large current which induces additional thermal stress on the components.

In [81–84] a two stage topology is presented that consists of an (interleaved) boost converter cascaded with a Series Resonant Full Bridge (SR FB) converter. The advantage is that the Maximum Power Point Tracking (MPPT) and the high step up are decoupled, allowing operating the SR FB with a constant switching frequency, which relaxes the constraints on the transformer design [81]. The major drawback of this circuit is the large amount of components, especially transistors, and the use of a series resonant capacitor.

In [85] an Interleaved Boost with Integrated Winding Coupled Inductor (IBIWCI) is presented and the effect of the parasitic resistance on the voltage gain is compared to other coupled inductor boost topologies. It was found that the voltage gain of the IBIWCI suffers the least from this effect. Please note that the voltage gain which is given in Table 1 is valid for $\delta > 0.5$. The topology is an interesting option as it only uses two ground-referenced switches, has an interleaved input, and no resonant capacitors are required.

The two last topologies that were investigated are the current-fed push pull (CFPP) and the Isolated Interleaved Boost Converter (IIBC). Both topologies are interesting from a reliability perspective due to the low component count. However, the IIBC is preferred over the CFPP because the voltage rating of the transistors is halved and the input current is interleaved, which reduces the required input capacitance.

The IIBC topology is shown in Figure 6 and has several interesting properties that make it a suitable candidate for BIPV applications. First, all switches can be referenced to ground, which means that no floating gate driver supplies are required. Furthermore, the required reverse blocking voltage of the MOSFETs is V_{out}/n, which means that transistors with lower $R_{DS,on}$ and faster switching speed can be used. Second, the transformer has a bidirectional excitation, in contrast to e.g., a flyback converter which has a unidirectional excitation. The transformer core can be sized smaller and no air gap is required for energy storage purposes. Third, the topology is inherently an interleaved topology. Consequently, the input current ripple is strongly reduced and fewer input capacitance is required. Fourth, the transformer can prevent that failures on the low voltage side propagate and impact the high voltage side.
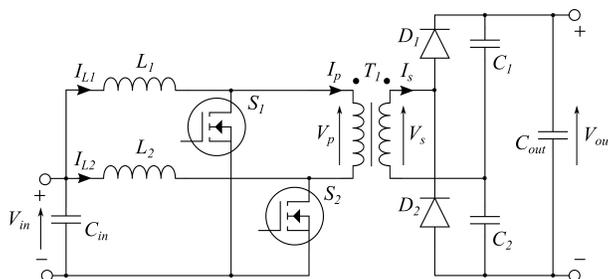

Figure 6. Circuit topology of the Isolated Interleaved Boost Converter.

5.4. Hardware Development

Now that a topology is selected, components can be selected taking into account the guidelines that were developed in Section 4. Figure 7 shows the developed IIBC prototype and highlights the major building blocks. An overview of the used components is given in Table 2. The dimensions of the PCB are 125×55 mm^2 and the converter operates at a switching frequency of 100 kHz.
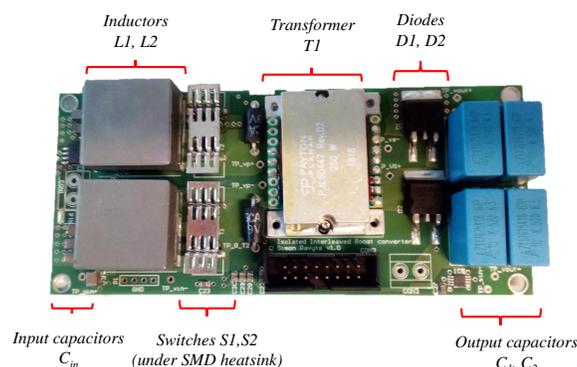

Figure 7. Experimental prototype of the Isolated Interleaved Boost Converter.

Table 2. Overview of components for the experimental prototype.

Component	Type	Value
C_{in}	KEMET C475M1R2C7186	100 V, 5×4.7 µF
L_1, L_2	BOURNS SRP2313AA-470M	14 A, 47 µH
S_1, S_2	TOSHIBA TPH3R70APL	100 V, $R_{on} = 3.1$ mΩ
D_1, D_2	ST STTH12R06	600 V, $V_f = 1.4$ V
C_1, C_2	EPCOS B32672P5105K000	520 V, 4×1 µF
T_1	Payton custom design	n = 5

To increase the power density, MLCCs with J-leads are preferred above film capacitors at the input. The inductors have an automotive grade AEC-Q200 certification. The MOSFETs employ copper clip technology instead of bond wires and are cooled using miniature SMD heat sinks. For the output, diodes are preferred over active switches since they do not require a gate driver. Film capacitors are used with a relatively large voltage margin of 200/520 V to further increase their lifetime and because their dominant failure mode is open circuit. This is an important feature because the failure of one MLC may not imply the failure of the entire BIPV feeder.

Care was taken in achieving a symmetrical lay-out of the input stage such that the parasitics in both branches would be approximately equal. By doing so, the current is divided equally between both branches and a single current sensor can be used for controlling the input current.

The converter efficiency for different input voltages and a constant output voltage of 400 V was measured using a ZES ZIMMER LMG500 power analyzer and is plotted in Figure 8. A peak efficiency of 93.3% is reached for an input of 30 V. In comparison, the IIBC that is presented in [87] also operates at 100 kHz, employs SS and steps up to 200 V, has a peak efficiency of 94.1%. Pease note that the efficiency is lower compared to other state-of-the-art converter solutions, however the focal point of this paper is on reliability and measures that increase the efficiency, such as soft switching and synchronous rectification, were avoided for this reason. This design can be the starting point for future efficiency improvements, for example by a custom design of the inductors.
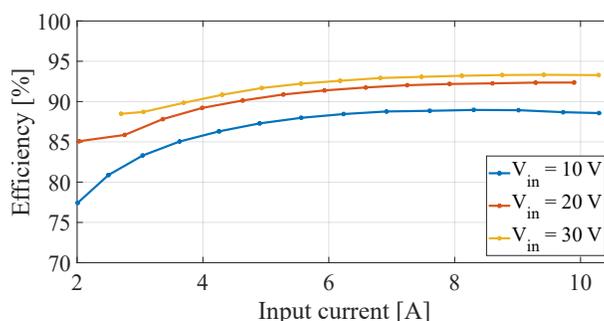
Figure 8. Measured efficiency curve of the developed prototype for different input voltages to an output voltage of 400 V.

One of the possible failure modes of this converter, namely MOSFET solder joint degradation, has been investigated in [16]. It was found that solder joint crack initiation might occur after 4.3 or 9.1 years, depending on the installment location. In [34], the placement of a BIPV converter in several locations around the frame, and the impact of the placement on film capacitor reliability, was investigated using a measured one-year mission profile. A B10 lifetime of 1063 years was found for the output film capacitor and the conclusion was that the film capacitor is propably not the first component to fail in the converter. In future work, other failure mechanisms such as bond wire lift-off and solder joint degradation in the diodes; and MLCC cracking due to CTE mismatch will be further investigated.

To further improve the reliability of the converter, the addtion of an active thermal control layer is a next logical step in the design process. This is however not included in this paper as the focus was on the hardware aspects of the system.

6. Conclusions

This paper presented a heuristic methodology for designing reliable DC/DC converters, specifically intended for BIPV applications. First, different components and their impact on converter reliability were discussed. Second, an overview of practical methods is provided to further enhance the availability. Then, a heuristic methodology was presented that can be used as an addition to the existing DfR literature and focuses specifically on the hardware aspects and converter topology selection. Lastly, the methodology was applied to the case of BIPV MLCs, which is a mission critical application with high peak temperatures. An overview of candidate topologies was presented and the IIBC was selected. An experimental prototype was built and the efficiency results discussed.

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