Ammonium sulfide vapor passivation of $In_{0.53}Ga_{0.47}As$ and InP surfaces

Alireza Alian, Guy Brammertz, Clement Merckling, Andrea Firrincieli, Wei-E Wang, H. C Lin, Matty Caymax, Marc Meuris, Kristin De Meyer, and Marc Heyns

View Online   Export Citation

ARTICLES YOU MAY BE INTERESTED IN

Passivation of InGaAs surfaces and InGaAs/InP heterojunction bipolar transistors by sulfur treatment
Applied Physics Letters **73**, 665 (1998); https://doi.org/10.1063/1.121941

A systematic study of $(NH_4)_2S$ passivation (22%, 10%, 5%, or 1%) on the interface properties of the $Al_2O_3/In_{0.53}Ga_{0.47}As/InP$ system for n-type and p-type $In_{0.53}Ga_{0.47}As$ epitaxial layers
Journal of Applied Physics **109**, 024101 (2011); https://doi.org/10.1063/1.3533959

Surface passivation of III-V compound semiconductors using atomic-layer-deposition-grown Al_2O_3
Applied Physics Letters **87**, 252104 (2005); https://doi.org/10.1063/1.2146060

AIP Publishing

Ammonium sulfide vapor passivation of In$_{0.53}$Ga$_{0.47}$As and InP surfaces

Alireza Alian,[1,2,a)] Guy Brammertz,[1] Clement Merckling,[1] Andrea Firrincieli,[1,2] Wei-E Wang,[1] H. C Lin,[1] Matty Caymax,[1] Marc Meuris,[1] Kristin De Meyer,[1,2] and Marc Heyns[1,2]

[1]IMEC, 3001 Leuven, Belgium
[2]KULeuven, 3001 Leuven, Belgium

The efficiency of the ammonium sulfide vapor (ASV) treatment, as opposed to the wet treatment in the liquid ammonium sulfide solution, on the performance improvement of the In$_{0.53}$Ga$_{0.47}$As surface-channel as well as InP-capped buried-channel metal-oxide-semiconductor field-effect-transistors (MOSFET) was demonstrated for the first time. MOSFETs were fabricated with either HCl or ASV surface treatments prior to the gate oxide deposition. ASV treatment was found to be very efficient in boosting the drive current of the transistors compared to that of the HCl treatment. It was also found that the ASV treatment leads to a lower border trap density and slightly higher oxide/semiconductor interface defect density compared to that of the HCl treatment. X-ray photoelectron spectroscopy (XPS) studies of In$_{0.53}$Ga$_{0.47}$As native oxide regrowth after both surface treatments identified indium sub-oxides as a possible cause of the performance degradation of the HCl treated devices. Based on this work, ASV treatment could be an efficient solution to the passivation of III-V surfaces. © 2011 American Institute of Physics. [doi:10.1063/1.3638492]

III-V materials, due to their high electron mobility, have been considered as one of the strong candidates to further scaling of the Complementary-MOS (CMOS) technology.[1–4] One of the bottlenecks against the introduction of these materials in CMOS production, however, is the lack of a high semiconductor/dielectric interfacial quality which leads to significantly degraded transistor characteristics. Various treatments have been suggested to mitigate the passivation issues of III-V surfaces. Among them, sulfur treatments have been studied extensively and seem to offer a promising solution path.[5–13] Effect of ASV on the surface passivation behavior of InP has been reported previously using XPS and Capacitance-Voltage (C-V) measurements of MOS capacitors.[14] However, no studies have been carried out on the effect of ASV on In$_{0.53}$Ga$_{0.47}$As and its direct impact on the transistor device characteristics. This work compares the surface passivation behavior of In$_{0.53}$Ga$_{0.47}$As and InP after treatments with either HCl or the vapor from (NH$_4$)$_2$S solution, as opposed to the treatment in the aqueous (NH$_4$)$_2$S solution,[7–13] by electrical characterization of the implant-free quantum-well MOSFETs treated with the aforementioned chemicals prior to the gate oxide deposition. Results of the XPS measurement on the In$_{0.53}$Ga$_{0.47}$As surface as well as the capacitance-voltage (C-V) and the current-voltage characteristics of the transistor devices are compared with and without ASV surface treatment.

The cross section and the structure of the MOSFET devices fabricated as the test structure is shown in Figure 1. Epitaxial heterostructures were grown on (001)-oriented InP semi-insulating substrates by metal organic vapor phase epitaxy (MOVPE). 100 nm thick SiO$_2$ was sputtered on the surface serving as the hard mask. After the mesa isolation etch, the gate recess etch was performed by selective wet etching of the highly n-doped In$_{0.53}$Ga$_{0.47}$As layer to the InP

in an H$_2$SO$_4$:H$_2$O$_2$:H$_2$O solution. The 3 nm InP cap was kept to serve as the top barrier layer on the buried channel devices. On the surface channel devices, the InP cap was removed through wet etching of InP selective to the In$_{0.53}$Ga$_{0.47}$As channel using an HCl:H$_2$O solution. The surface of the surface channel devices was either left untreated (in fact, the surface is HCl treated from the previous InP cap etching step) or was treated with ASV. Buried channel devices received a diluted HCl treatment followed by either no treatment (HCl-treated) or the ASV treatment. ASV treatment was accomplished by simply holding the HCl treated sample faced down above a beaker containing ammonium sulfide solution. The duration of the ASV treatment was 3 min and the samples were immediately transferred to the atomic layer deposition (ALD) tool for the gate oxide deposition. The gate oxide was made of 10 nm thick Al$_2$O$_3$ layer deposited at 300 °C. After the oxide deposition, 40 nm TiW was deposited and patterned as the gate metal followed by the source/drain contact opening and metallization. The devices were forming gas (10% H$_2$, 90% N$_2$) annealed at 370 °C for 15 min. Additional samples were prepared for the XPS evaluation to understand the efficiency of the ASV treatment in blocking the native oxide formation. For this purpose, In$_{0.53}$Ga$_{0.47}$As samples with and without ASV surface treatment were capped after 30 min of air exposure following the treatment with 2 nm Al$_2$O$_3$ deposited by solid source molecular beam deposition.[15]

Figure 2 shows the C-V characteristics of the surface and buried channel devices with either HCl or ASV treatment prior to the gate oxide deposition. The C-V was collected at 15 frequencies swept logarithmically from 1 kHz to 1 MHz. The C-V behavior clearly shows less flatband frequency dispersion for the ASV treated device compared to the HCl treated one. It can also be observed that the C-V valley capacitance is slightly lower for the HCl treated device compared to the ASV treated one. This could point out to the slightly higher interface state density (D_{it}) closer to the
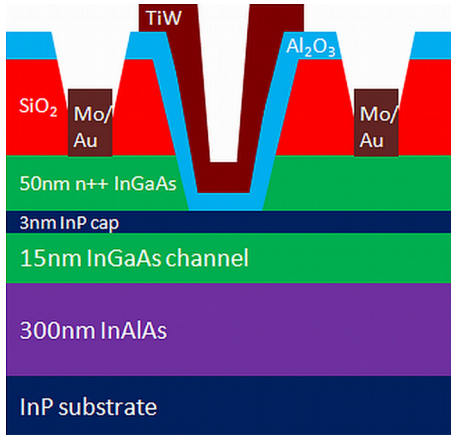
FIG. 1. (Color online) Transistor device structure. Shown in the picture is the structure of the buried channel device. For the surface channel device the 3 nm InP cap is removed during the recess.

FIG. 3. (Color online) (a) Drive current (I_{on}) and (b) the peak transconductance (g_m) as a function of the gate length for ASV and HCl treated surface channel and buried channel devices.

valence band side of the band gap of both InP and $In_{0.53}Ga_{0.47}As$ when treated with ASV. The D_{it} was extracted from the conductance measurements.[16] The measurement frequency (f) was associated with the energy of the traps (E_t) measured with respect to the conduction band edge through $1/f = \tau_{it} = \exp(E_t/kT)/(\sigma v_{th} N_c)$, where k is the Boltzmann constant, T is the temperature, σ is the trap capture cross section (assumed to be 1×10^{-15} cm^2), v_{th} is the electron thermal velocity, and N_c is the density of states in the conduction band.[17] The extracted D_{it} values are 4×10^{12} and 7×10^{12} cm^{-2}eV^{-1} at 0.2 eV below the conduction band (CB) edge of $In_{0.53}Ga_{0.47}As$ for the HCl and ASV treated devices, respectively. For InP, the corresponding D_{it} values are about 8×10^{12} and 9×10^{12} cm^{-2}eV^{-1} at 0.2 eV below the CB edge of InP. To probe, the D_{it} closer to the CB edge, conductance measurements were conducted at 77 K. It was found that the D_{it} values are smaller closer to the CB edge and become lower for the ASV treated devices than for the HCl treated ones. The D_{it} values at 70 meV bellow the CB edge are 2.5×10^{12} and 1.5×10^{12} for $In_{0.53}Ga_{0.47}As$ and 7×10^{12} and 5×10^{12} cm^{-2}eV^{-1} for the InP capped device, for the HCl and ASV treatments, respectively.

The drive current at an overdrive voltage (V_{od}) of 1.5 V and the transconductance (g_m) at a drain voltage (V_d) of 0.1 V are plotted in Figures 3(a) and 3(b) as a function of the gate length for both the surface and buried channel devices, respectively. These results clearly demonstrate that ASV is very efficient in boosting the ON state performance of both the surface channel and the buried channel devices. A comparison with previous studies[12,13] shows that ASV is as efficient as the aqueous $(NH_4)_2S$ in gaining a high drive current. As explained earlier, D_{it} is larger in the midgap for the ASV treated device than the HCl treated one. However, as the nature of these states is donor-like,[18] they will be electrically neutral during the ON-state operation of the device and will not influence the performance. The portion of the D_{it} located close to and above the surface Fermi level position during the device operation is affecting the ON-state performance as these traps are electrically active. The higher ON-state performance of the ASV treated device could be explained considering that the Fermi level is close to (and above) the CB edge during the ON-state operation and noting that the D_{it} is lower close to (and possibly above) the CB edge for the ASV treated device than the HCl treated one.

Figure 4 shows the drain current versus the gate voltage at a drain voltage of 100 mV for the surface and buried channel devices with different surface treatments. The comparison of the sub-threshold slope (SS) of the ASV treated device with the HCl treated one reveals a degradation which may point to the higher interface state density deeper in the band gap of the material for the ASV treated devices. These results confirm those of the D_{it} extraction discussed previously. However, based on the previous studies,[14] ASV treatment on the InP surface leads to strong surface doping effects and as a result, it
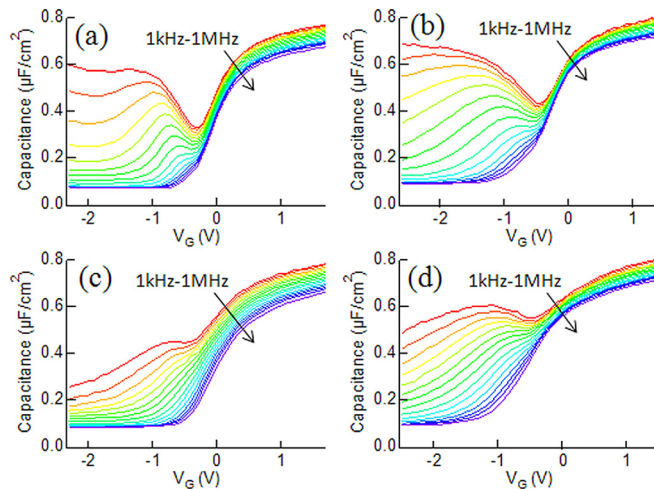

FIG. 2. (Color online) C-V characteristics (collected at 15 frequencies swept logarithmically from 1 kHz to 1 MHz) of the surface channel (a,b) and the buried channel (c,d) devices with either HCl (a,c) or ASV (b,d) treatments prior to the gate oxide deposition.
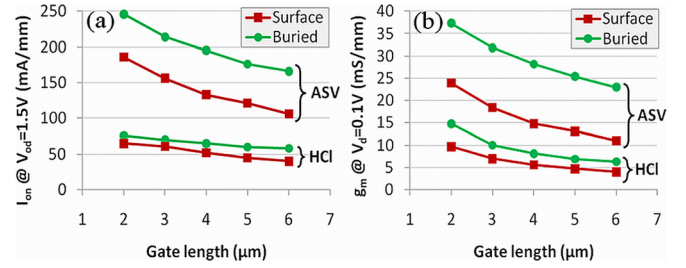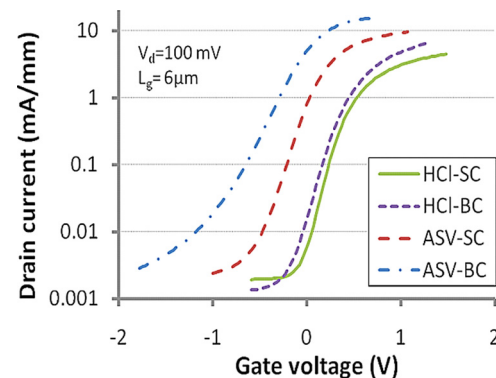

FIG. 4. (Color online) Drain current versus the gate voltage for the HCl and ASV treated surface channel (SC) and buried channel (BC) devices.
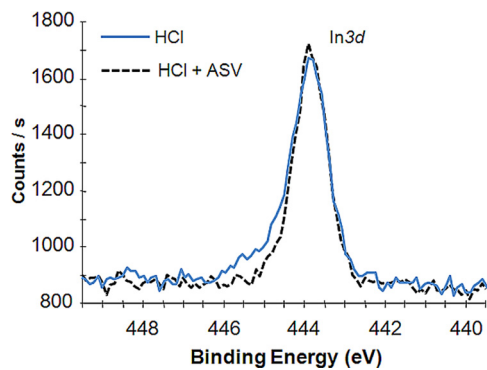
FIG. 5. (Color online) XPS spectrum of the In3d peak indicates the efficiency of ASV treatment in avoiding native oxide formation.

could degrade the *SS* by increasing the value of the depletion capacitance. Hence, most of the degradation in the *SS* of the ASV treated buried channel device is believed to be due to the surface doping effect. Comparing the buried channel and the surface channel devices, doping effect seems insignificant on the $In_{0.53}Ga_{0.47}As$ surface after ASV treatment, as the change in the *SS* value is less prominent for the ASV treated surface channel device compared to the HCl treatment. Consequently, one could conclude that the threshold voltage shift of the ASV treated surface channel device with respect to the HCl treated device is mostly due to the reduction in the negative oxide charge density. On the other hand, the threshold voltage shift of the buried channel device also includes the fixed charges formed at the interface of InP/Al_2O_3 resulting from the surface doping effect of ASV on the InP surface. The corresponding reduction in the oxide charge density after ASV treatment on the $In_{0.53}Ga_{0.47}As$ surface is about 2.2×10^{18} cm^{-3}, assuming a uniform charge distribution in the Al_2O_3 layer. The estimated fixed charge density as a result of the InP surface doping effect of ASV is about 1×10^{12} cm^{-2} at the Al_2O_3/InP interface.

XPS spectra of the In *3d* core levels for both HCl and ASV treated $In_{0.53}Ga_{0.47}As$ surfaces are shown in Figure 5. For both surface treatments, the concentration of arsenic and gallium sub-oxides (not shown) was below the detection limit of the XPS analyzer. In the case of the HCl treated $In_{0.53}Ga_{0.47}As$ surface, indium oxide was clearly observed. For ASV surface treatment, the concentration of InOx formed at the interface is considerably reduced. These analyses confirm the efficiency of the ASV treatment in limiting the formation of native oxides at the oxide/semiconductor interface. In this respect, ASV seems as efficient as the aqueous $(NH_4)_2S$ treatment reported previously.[5,8,11] These results indicate that indium or its oxides might be responsible for the drive current degradation. This can occur either due to the diffusion of In into the high-k layer creating border traps or the formation of interface states with an energy above the CB edge of $In_{0.53}Ga_{0.47}As$ (Ref. 18) which would degrade the carrier mobility.

The efficiency of the $(NH_4)_2S$ vapor treatment, as opposed to the aqueous $(NH_4)_2S$ treatment, in boosting the drive current of $In_{0.53}Ga_{0.47}As$ channel MOSFET was demonstrated for the first time. ASV treatment was found to increase the ON-state performance of the device by about a factor of 3. At the same time, ASV treatment results in degraded sub-threshold behavior of the InP capped device which was attributed to the surface doping effect of the ASV process on the InP surface. The ASV surface doping effect was found insignificant on the $In_{0.53}Ga_{0.47}As$ surface. The data indicate that ASV reduces the formation of negative charges in the oxide. The results of this work suggest that ASV treatment could be an efficient treatment for the passivation of the III-V surfaces.

[1]M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. K. Hudait, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, IEDM, 1 (2009).
[2]M. Passlack, P. Zurcher, K. Rajagopalan, R. Droopad, J. Abrokwah, M. Tutt, Y.-B. Park, E. Johnson, O. Hartin, A. Zlotnicka, P. Fejes, R. J. W. Hill, D. A. J. Moran, X. Li, H. Zhou, D. Macintyre, S. Thorns, A. Asenov, K. Kalna, and I. G. Thayne, IEDM Tech. Dig., 621 (2007).
[3]Y. Q. Wu, M. Xu, R. S. Wang, O. Koybasi, and P. D. Ye, IEDM Tech. Dig., 323 (2009).
[4]F. Xue, H. Zhao, Y.-T. Chen, Y. Wang, F. Zhou, and J. C. Lee, Appl. Phys. Lett. **98**, 082106 (2011).
[5]E. O'Connor, R. D. Long, K. Cherkaoui, K. K. Thomas, F. Chalvet, I. M. Povey, M. E. Pemble, P. K. Hurleya, B. Brennan, G. Hughes, and S. B. Newcomb, Appl. Phys. Lett. **92**, 022902 (2008).
[6]C. Merckling, Y. C. Chang, C. Y. Lu, J. Penaud, G. Brammertz, M. Scarrozza, G. Pourtois, J. Kwo, M. Hong, J. Dekoster, M. Meuris, M. Heyns and M. Caymax, Surf. Sci. **605**, 1778 (2011).
[7]D. Lin, N. Waldron, G. Brammertz, K. Martens, W.-E Wang, S. Sioncke, A. Delabie, H. Bender, T. Conard, W. H. Tseng, J. C. Lin, K. Temst, A, Vantomme, J. Mitard, M. Caymax, M. Meuris, M. Heyns, and T. Hoffmann, Electrochem. Soc., **28**(5) 173 (2010).
[8]R. Driad, Z. H. Lu, S. Charbonneau, W. R. McKinnon, S. Laframboise, P. J. Poole, and S. P. McAlister, Appl. Phys. Lett. **73**(5) 665 (1998).
[9]Z. Jin, K. Uchida, S. Nozaki, W. Prost, and F.-J. Tegude, Appl. Surf. Sci. **252**(21), 7664 (2006).
[10]M. R. Ravi, A. DasGupta, and N. DasGupta, IEEE Trans. Electron Devices **50**(2) 532 (2003).
[11]H. J. Tang, X. L. Wu, K. F. Zhang, Y. F. Li, J. H. Ning, Y. Wang, X. Li, and H. M. Gong, Appl. Phys. A **91**(4) 651 (2008).
[12]Y. Xuan, Y.Q. Wu, T. Shen, T. Yang, and P. D. Ye, IEDM Tech. Dig., 637 (2007).
[13]Y. Q. Wu, W. K. Wang, O. Koybasi, D. N. Zakharov, E. A. Stach, S. Nakahara, J. C. M. Hwang, and P. D. Ye, IEEE Electron Device Lett., **30**(7), 700 (2009).
[14]W. M. Lau, S. Jin, X.-W. Wu, and S. Ingrey, J. Vac. Sci. Technol. B **8**(4), 848 (1990).
[15]Y. C. Chang, C. Merckling, J. Penaud, C. Y. Lu, W.-E. Wang, J. Dekoster, M. Meuris, M. Caymax, M. Heyns, J. Kwo, and M. Hong, Appl. Phys. Lett. **97**, 112901 (2010).
[16]K. Martens, C. O. Chui, G. Brammertz, B. De Jaeger, D. Kuzum, M. Heyns, T. Krishnamohan, K. Saraswat, H. Maes, and G. Groeseneken, IEEE Trans Electron Devices **55**(2), 547 (2008).
[17]G. Brammertz, K. Martens, S. Sioncke, A. Delabie, M. Caymax, M. Meuris, and M. Heyns, Appl. Phys. Lett. **91**, 1 (2007).
[18]G. Brammertz, H.-C. Lin, M. Caymax, M. Meuris, M. Heyns, and M. Passlack, Appl. Phys. Lett. **95**, 202109 (2009).