Applied Physics Letters

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Cite as: Appl. Phys. Lett. **93**, 183504 (2008); https://doi.org/10.1063/1.3005172
Submitted: 01 September 2008 . Accepted: 15 September 2008 . Published Online: 03 November 2008

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Capacitance-voltage characterization of GaAs–Al_2O_3 interfaces

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(Received 1 September 2008; accepted 15 September 2008; published online 3 November 2008)

The authors apply the conductance method at 25 and 150 °C to GaAs–Al_2O_3 metal-oxide-semiconductor devices in order to derive the interface state distribution (D_{it}) as a function of energy in the bandgap. The D_{it} is governed by two large interface state peaks at midgap energies, in agreement with the unified defect model. S-passivation and forming gas annealing reduce the D_{it} in large parts of the bandgap, mainly close to the valence band, reducing noticeably the room temperature frequency dispersion. However the midgap interface state peaks are not affected by these treatments, such that Fermi level pinning at midgap energies remains. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3005172]

We have recently shown that due to the larger bandgap of GaAs as compared to Si, the midgap interface states in GaAs are too slow to respond to the usual *CV*-characterization frequencies at room temperature.[1] In addition to room temperature measurements, measurements at higher substrate temperatures are also needed in order to deduce the characteristics of the interface states over the whole bandgap and in particular at midgap energies. In the following, we will apply the conductance method[2] to alternating current (ac) *CV* measurements performed with substrate temperatures of 25 and 150 °C on both *n*- and *p*-type GaAs substrates, in order to deduce the D_{it} as a function of energy in the whole bandgap. Alternative methods to derive the interface state density over the whole bandgap are quasistatic *CV* measurements with very slow sweep rates and long integration times[3] or photoluminescence intensity measurements.[3]

The samples analyzed in this work consist of 5×10^{17} cm^{-3} Si- (*n*-type) or Zn- (*p*-type) doped GaAs substrates on which 10 nm Al_2O_3 was grown by atomic layer deposition (ALD) in an ASM Pulsar ALD reactor. The Al_2O_3 was deposited at 300 °C using alternating pulses of H_2O and trimethylaluminum. Prior to deposition, two different surface treatments were applied. A first set of samples (*n*- and *p*-type) received a 5 min HCl clean and a second set of samples (*n*- and *p*-type) received a 5 min $(NH_4)_2S$ wet chemical clean. The resulting four samples got an Ohmic contact on the back side consisting of AuZn/Au (*p*-type) or AuGe/Ni/Au (*n*-type) multilayers, followed by a 30 s 380 °C forming gas anneal (FGA). On the front side Pt metal dots were deposited through a shadow mask. In addition, the samples with the $(NH_4)_2S$ clean were further treated with a 30 min FGA at 400 °C. 200 μm diameter metal dot capacitors were then measured with a standard HP 4284 *LCR* meter. In order to get a continuous picture of the D_{it}, 25 frequencies were measured varying logarithmically from 100 Hz to 1 MHz.

The experimental results from the samples with HCl clean are shown in Fig. 1, whereas the data for the S-treated samples with FGA is shown in Fig. 2. The four figures on the upper line show the regular *CV* data for the 25 measured frequencies of the *n*- and *p*-type samples at 25 and 150 °C, respectively. The four figures on the lower line represent the conductance data, plotted as a conductance map, which shows a two dimensional contour plot of the normalized substrate conductance ($G_{p/}A\omega q$) as a function of bias voltage and measurement frequency. Here, G_p is the substrate conductance, derived from the measured conductance G_m by correcting for the oxide capacitance (C_{ox}),[2] ω is the measurement pulsation, and q is the majority carrier charge. In the conductance plots of Figs. 1 and 2, the measurement frequency f on the vertical axis was directly transformed into trap energy in the bandgap E_t, using the characteristic emission time constants of the interface states, which behave according to general Fermi–Dirac statistics,[4]

$$\tau = \frac{1}{\sigma v_t N} \exp(\Delta E/kT), \tag{1}$$

where ΔE is the energy difference between the majority carrier band edge energy and the trapping state energy E_t (depth of the trap), k is the Boltzmann constant, T is the semiconductor temperature, σ is the capture cross section of the trapping state, v_t is the thermal velocity of the majority charge carriers, and N is the density of states in the majority carrier band. From this characteristic emission time τ, one can directly derive the characteristic response frequency $f = 1/2\pi\tau$ of a trapping state, knowing the depth of the trapping state in the bandgap. This equation shows that the characteristic emission frequency depends exponentially on the depth of the trapping state in the bandgap. The further the trap is away from the band edge, the slower it will emit a trapped charge. More details can be found in Ref. 1. Concerning the parameter values from Eq. (1), the thermal velocity and density of states are well known and well defined values for a specific semiconductor,[5] whereas the trap capture cross section depends strongly on the nature of the trap.[6] The capture cross section can take values varying from 10^{-12} to 10^{-20} cm^2. Even larger values than 10^{-12} cm^2 cannot be excluded. Nevertheless, the largest majority of trapping states has capture cross sections of the order of 10^{-15} cm^2 (Ref. 6). In the following, a capture cross section of 10^{-15} cm^2 is assumed in order to illustrate the effects of the characteristic emission time constant. Assuming a value for the capture cross section leads of course to an uncertainty concerning the absolute position of the interface state position in the bandgap. The further the real trap capture cross

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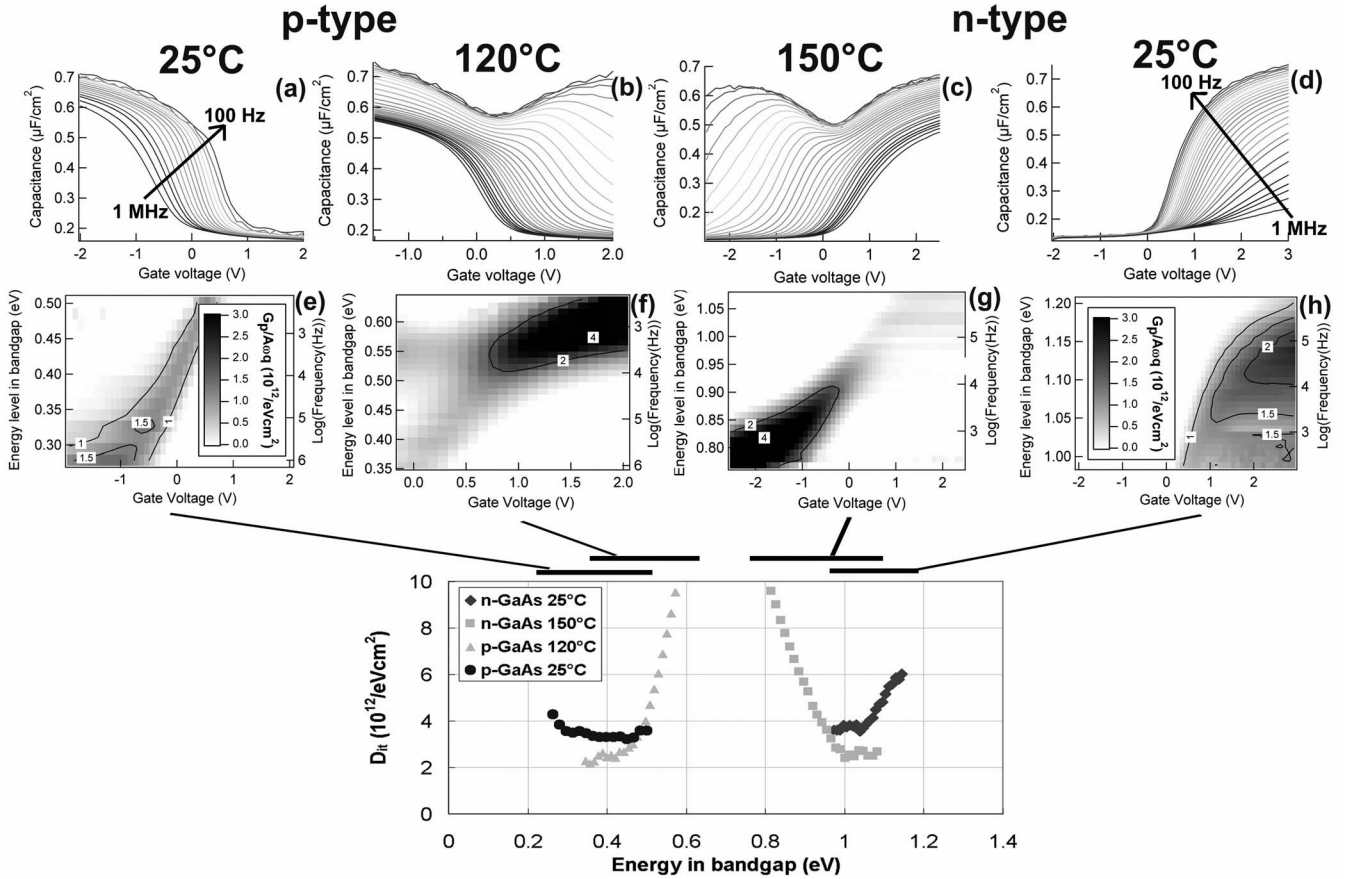

FIG. 1. Capacitance- and conductance-voltage measurements on 200 μm diameter GaAs/Al_2O_3 MOS capacitors with HCl clean: (a) 25 °C *CV* curves of *p*-type GaAs capacitor, (b) 120 °C *CV* curves of *p*-type GaAs capacitor, (c) 150 °C *CV* curves of *n*-type GaAs capacitor, (d) 25 °C *CV* curves of *n*-type GaAs capacitor, (e) 25 °C $G_p/A\omega q$ map of *p*-type GaAs capacitor, (f) 120 °C $G_p/A\omega q$ map of *p*-type GaAs capacitor, (g) 150 °C $G_p/A\omega q$ map of *n*-type GaAs capacitor, and (h) 25 °C $G_p/A\omega q$ map of *n*-type GaAs capacitor. The lower graph shows the GaAs–Al_2O_3 (HCl clean) D_{it} derived from the four conductance maps, the arrows indicating which measurement measures the interface state density in what portion of the bandgap.

section is off with respect to our assumed value of 10^{-15} cm^{-2}, the larger the error. Nevertheless, the exponential term in Eq. (1) is dominant and simple arithmetic on Eq. (1) shows that even a variation of the capture cross section by three orders of magnitude will only give rise to an energy difference of 0.18 eV. This somewhat exotic method of positioning the interface states in the bandgap is necessary because usually the conductance method relies on the determination of the flatband voltage in order to position the interface states in the bandgap, whereas this value can not be determined for our heavily pinned devices.[7]

In order to clarify the data in the conductance maps, Fig. 3 shows a subset of the data of Fig. 1(g) in a more generally accepted way of representing conductance data. This will allow the reader to interpret the data in the conductance maps. Nevertheless, the conductance maps show the conductance data in a more efficient and intuitive way, as it allows visualizing the movement of the surface Fermi level as the gate bias is varied. Clearly, the frequency for which the maximum in the conductance data for every gate bias occurs corresponds to the characteristic frequency of the trapping states at the energy position in the vicinity of the surface Fermi level position at that precise gate bias. Therefore, following the maxima in the conductance map visualizes how the surface Fermi level moves over the energy gap as the gate bias is varied. When this trace of maximum conductance turns horizontal, as can be seen in particular on Figs. 1(f), 1(g), 2(f), and 2(g), the Fermi level is effectively hindered from moving, which is generally expressed by the term Fermi level pinning. This can be easily visualized in such a conductance map. Applying the conductance method,[2] i.e., extracting the interface state data from the height of the conductance peaks, the D_{it} shown in the lower parts of Figs. 1 and 2 can be derived. Note that in the region where G_p/ω approaches C_{ox} ($D_{it} > 10^{13}$/eV cm^2), the extracted values are lower limits to the real D_{it}.[7] We can see that for both the HCl-cleaned and the S-cleaned samples, the D_{it} is governed by two large peaks around midgap energies. This is in agreement with the unified defect model[8] (UDM) and the pinned Fermi level around midgap energies for the vast majority of GaAs interfaces,[9] with the exception of the Ga_2O_3 passivated interface.[10] In addition, we see that somewhat closer to the conduction band, there is another much smaller peak. Photoluminescence spectroscopy data of Si-doped samples (not shown here) as well as deep level transient spectroscopy measurements[11] indicate that this smaller peak seems to be related to a Si defect in the bulk of the GaAs layer. This is also confirmed by the shape of the conductance peaks in Figs. 1(h) and 2(h), which have a more plateaulike shape toward accumulation, without a clear maximum, which is a typical signature of bulk defects.[2] The effect of the S-passivation and FGA can also be clearly seen. It reduces the D_{it} close to the valence band to levels close to mid-10^{11}/cm^2 eV. As a consequence of this reduction, the frequency dispersion in the room temperature *CV* curves of

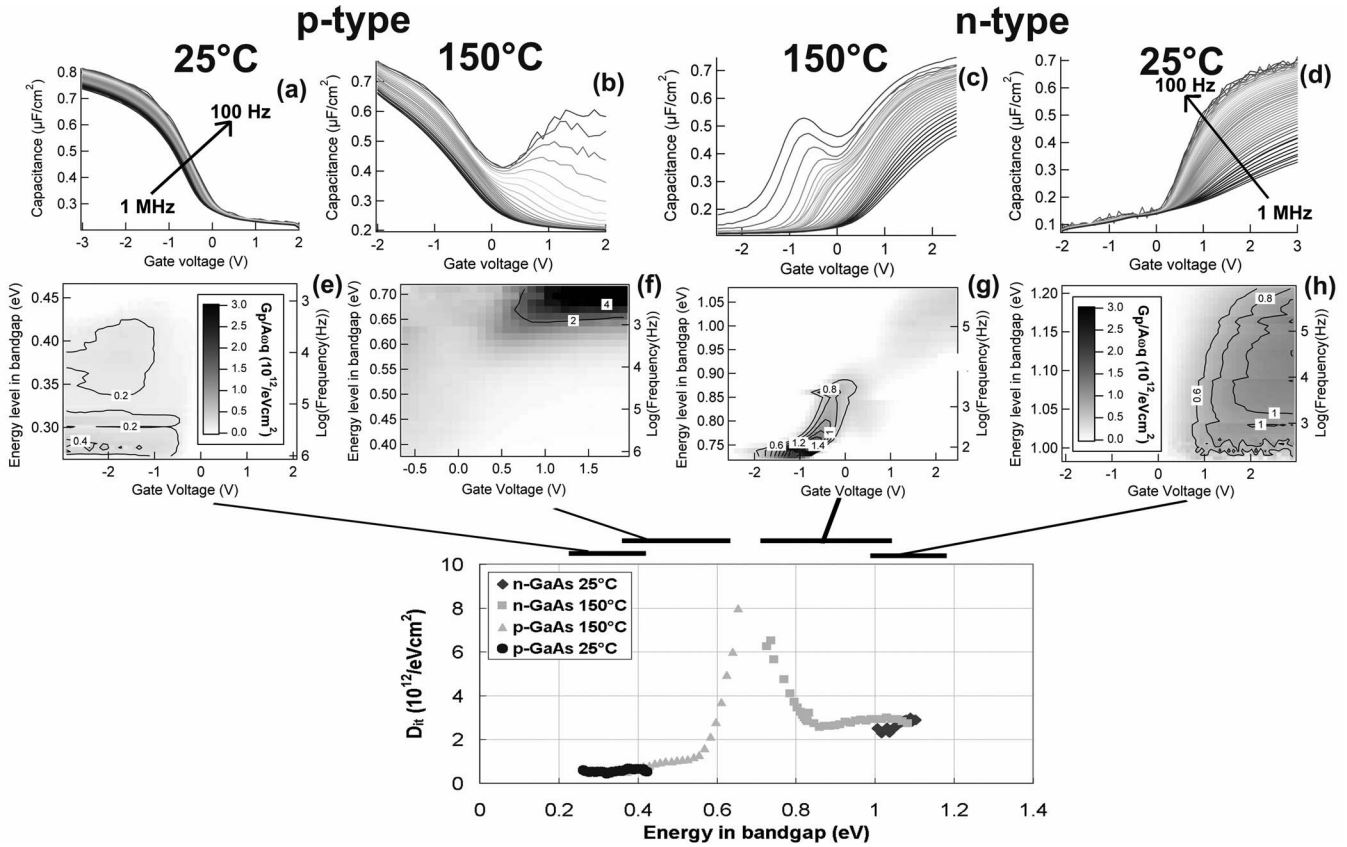

FIG. 2. Capacitance- and conductance-voltage measurements on 200 μm diameter GaAs/Al_2O_3 MOS capacitors with S-passivation and FGA: (a) 25 °C *CV* curves of *p*-type GaAs capacitor, (b) 150 °C *CV* curves of *p*-type GaAs capacitor, (c) 150 °C *CV* curves of *n*-type GaAs capacitor, (d) 25 °C *CV* curves of *n*-type GaAs capacitor, (e) 25 °C $G_p/A\omega q$ map of *p*-type GaAs capacitor, (f) 120 °C $G_p/A\omega q$ map of *p*-type GaAs capacitor, (g) 150 °C $G_p/A\omega q$ map of *n*-type GaAs capacitor, and (h) 25 °C $G_p/A\omega q$ map of *n*-type GaAs capacitor. The lower graph shows the GaAs–Al_2O_3 (S-passivated) D_{it} derived from the four conductance maps, the arrows indicating which measurement measures the interface state density in what portion of the bandgap.

the *p*-type samples is strongly reduced [Fig. 2(a)]. The region close to the conduction band does not seem to be affected as much by the S-passivation and FGA [Figs. 1(d) and 2(d)]. Most importantly, the two large midgap peaks, which completely dominate the D_{it}, although somewhat reduced or shifted in energy position, do not disappear. The Fermi level is still pinned around midgap energies. ALD Al_2O_3 with S-passivation and FGA is therefore not able to passivate the GaAs interface. Fermi level pinning around midgap energies for both *n*- and *p*-type GaAs remains, similar to molecular beam epitaxy deposited Al_2O_3 on GaAs.[10]

We have shown how the conductance method can be applied at 25 and 150 °C in order to derive the D_{it} over the whole bandgap of GaAs. Experimental measurements on HCl- and S-cleaned GaAs–Al_2O_3 metal-oxide-semiconductor (MOS) capacitors show that two large peaks around midgap energies govern the properties of the GaAs surface, which is in agreement with the UDM by Spicer *et al.* Although S-passivation and FGA have some beneficial effects on the interface state density, reducing notably the room temperature frequency dispersion of *p*-type devices, Fermi level pinning around midgap energies is still present.

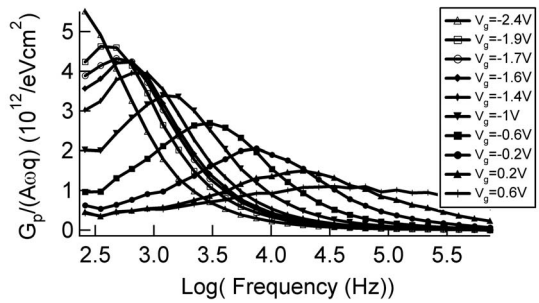

FIG. 3. More common representation of a subset of the conductance data from Fig. 1(g): $G_p/A\omega q$ as a function of frequency for different gate bias voltages.

The authors acknowledge support by the European Commission's project FP7-ICT-DUALLOGIC No. 214579 *Dual-channel CMOS for (sub)*-22 nm *high performance logic*.

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