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Shaping the future of nanoelectronics beyond the Si roadmap with new materials and devices

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Abstract

The use of high mobility channel materials such as Ge and III/V compounds for CMOS applications is being explored. The introduction of these new materials also opens the path towards the introduction of novel device structures which can be used to lower the supply voltage and reduce the power consumption. The results illustrate the possibilities that are created by the combination of new materials and devices to allow scaling of nanoelectronics beyond the Si roadmap.

Keywords: nanoelectronics, high mobility materials, Ge, III/V, new devices, tunnelFET's, nanowires

1. Introduction

The continued downscaling of the MOSFET dimensions according to Moore's law and scaling guidelines, is an unprecedented technological feat ([1-3]) with enormous economical implications. The scaling of the MOSFET has allowed increased functionality per unit chip-area, reduced cost per functionality, increased performance, and reduced device switching power. An important challenge that arises from the continuous scaling is that the performance is no longer keeping up with the scaling trend and a performance gap arises [4]. Over the last years many new materials and technologies had to be introduced in order to continue the scaling and increase the device performance. In the recent past further progress along the exponential miniaturization roadmap seemed to be made impossible by the downscaling of the silicon oxide thickness to unfeasibly thin layers. The properties of SiO_2 are seen as key to the success of the CMOS industry due to the high electrical quality of the Si/SiO_2 interface, its favorable material properties and reliability. The continued reduction of the physical oxide thickness demanded by the scaling requirements ultimately renders the material unfit for further scaling as it would increase the gate leakage current prohibitively due to fundamental quantum mechanical tunneling. Materials with a higher dielectric constant (κ-value) maintain channel control for larger thicknesses and reduce the gate leakage current. The introduction of high-κ metal gate technology, which resolved the gate leakage issue in 45 nm production MOSFETs [5, 6] proved to be an enormous challenge and is one of the largest recent innovations in CMOS technology. Further performance increases can be achieved by using channel materials with higher carrier mobility. Introducing strained Si was a first step in this direction, but the ultimate gains that can be achieved with advanced straining techniques is judged to be not sufficient on itself for future technology generations. A possible scenario for next generation devices for the 32 and 22nm nodes is to introduce alternative device architectures such as strained-SOI and/or multiple-gated devices (e.g. FinFETs, planar double gated or tri-gated) which results in better electrostatic control of the channel and improved transport due to tolerance to low channel doping. To further increase performance for the sub-22nm nodes, channel engineering may be necessary, introducing high mobility materials other than Si (e.g. Ge, or III-V compound semiconductors). Since ultimately, the major showstopper on the scaling roadmap is not device speed, but rather power density, the introduction of these advanced materials will go together with the introduction of new device concepts such as TunnelFET's that could operate at reduced supply voltage.

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2. High mobility substrates

The introduction of high-*k* gate dielectrics and metal gates into advanced CMOS technology has re-opened the door to germanium and III-V compounds as potential replacements for silicon channels, offering the possibility to further enhance the drive current of the devices and increase the performances of future CMOS generations. From an historical point of view, the first (bipolar) transistor was built on bulk Ge in 1947 by Bardeen, Brattain and Shockley from Bell Labs. This scientific and technological breakthrough was awarded by a Nobel Prize in Physics in 1956. About 12 years later, the first integrated circuit was invented by Kilby, also using a Ge substrate, and for which he received the 2000 Nobel Prize in Physics. The first MOSFET was fabricated in 1960 by Kahgn and Atalla, made of silicon, after Atalla showed that a Si/SiO_2 interface of good quality and stability was attainable with his oxidation recipe. The oxide of germanium, on the contrary, dissolves in water and the germanium oxide was found to be of insufficient quality. Together with the plentiful supply of silicon this explains why today CMOS ICs are made of silicon. Concerning the III-V channels, the advantage of GaAs MOSFET over its Si counterpart was early recognized because the electron mobility in GaAs is more than five times higher than that in Si. The first GaAs MOSFET work using SiO_2 as gate dielectric was already reported in 1965 [7], but it was quickly realized that SiO_2 was not the right gate dielectric for GaAs, which sparked an enormous research effort in the following decades with a search for a low-defect, thermodynamically stable gate dielectric for GaAs.

The most compelling reason for the use of high mobility channel materials is the promising drive current perspective. The mobility determines the relationship between the driving electric field and the carrier velocity at low fields. Long-channel devices operate in the low field regime and hence a direct increase in the drive current is observed when the carrier mobility in the channel is increased. In very short-channel devices the high field saturation velocity influences the drive current and beyond the 22nm node devices when devices start to exhibit (quasi-)ballistic transport, the importance of the carrier mobility is still a topic of debate. It has been suggested [8] that in this case the drive current is determined by the carrier injection probability which on its turn is related to the low field drift mobility. According to this model high mobility materials would provide increased drive currents even for highly scaled devices. Although the full theoretical understanding on the importance of mobility in ultra short channel devices is still lacking, an improved performance is predicted for these highly scaled devices when high mobility materials are used that also have a high carrier density [9]. Germanium has a relatively high mobility for both electrons and holes and could be suitable for both nMOS and pMOS devices. This promise seems to be hold for Ge pMOS devices but, despite some recent encouraging results [10, 11], the current performance of short channel Ge nMOS devices with low EOT (Equivalent Oxide Thickness) is still below expectations. There are many III-V materials that exhibit very high electron mobility and thus are suitable candidates for nMOS devices, but the selection of a proper III-V compound semiconductor with high hole mobility that can be used for pMOS channels is still an important research topic [12]. Strain engineering will most likely play in important role in achieving the final target device performance for both Ge and III-V compounds, similar to the current Si technology, and especially for the III/V pMOS materials this may be a crucial parameter [13].

To be able to realize the Ge-III/V technology, it is essential to develop a method to introduce these materials on a large Si substrate. Since there is only a limited availability of Ge it will be necessary to use and develop GOI (Germanium-On-Insulator) substrates or GOS (Germanium-on-Silicon) substrates of sufficient quality or otherwise locally introduce the Ge. Various methods are being explored for this ranging from (selective) epi growth [14] to the (local) Ge condensation technique whereby a SiGe layer is deposited on top of a SiO wafer and the Ge concentration is increased by specially tuned oxidation steps followed by subsequent etching [15]. Also the III-V materials will have to be introduced on a Si platform wafer. The relatively important lattice mismatch requires careful tuning of the buffer layers and can result in rather complex stacks [16]. Also, the use of alternative techniques such as microchannel epitaxy are considered as a possible option [17]. In all cases defect densities in the material are a prime concern since it will affect both the carrier mobility and the leakage currents in the devices. Direct growth of both Ge and III/V in Si STI trenches is proposed to be the most attractive option at present for co-integration of these materials on bulk Si substrates. The basic idea behind this approach is that, either the misfit dislocations terminate at the walls of deep and narrow STI trenches before they turn into threading dislocations, or that eventual threading arms themselves can be stopped at these edges below the active device region thanks to the large aspect ratio. Therefore, they are trapped at the bottom of the trenches leaving the top layer with a low defect density so that active device layers with low defectivity can be grown. The growth of high crystalline quality InP layers selectively grown in STI trenches on Si (001) substrates with 6º offcut toward (111) were already demonstrated [18]. These layers provide the starting templates for fabrication $In_{0.53}Ga_{0.47}As$ high mobility channel nMOS devices on Si substrates.

In all cases the key challenge is the electrical passivation of the interface between the high-κ dielectric and the alternative channel materials. Finding a high quality gate insulator and forming a well-passivated interface with sufficiently low density of interface states is a major challenge for both Ge and III-V compounds. A high density of active interface defects will hamper the electrical properties of surface channel devices, like inversion-mode MOSFETs. Nearly all well functioning high-κ dielectrics with low EOT (Equivalent Oxide Thickness) on Si still use a thin Si/SiO_2 interfacial layer on top of which a high-κ dielectric is deposited and thereby still rely on the excellent properties of this unique material combo. Various studies have been aiming at mimicking this Si/SiO_2 interface on Ge and III/V materials by introducing an ultrathin Si capping layer of only a few monolayers thick as a surface passivation layer. In the specific case of Ge this approach has been demonstrated to be very successful for pMOS devices [19, 20]. Also on III-V surfaces the use of a very thin amorphous or crystalline Si layer as an interfacial control layer has provided some encouraging results [21-26]. Other approaches to obtain passivated surfaces on Ge are based on a thermally grown GeO_2 or GeON interfacial layer [27-29] or use various types of passivating surface treatments [30, 31], while some high-κ dielectrics have also been shown to provide improved Ge surface passivation [32, 33]. Some early studies on III-V materials discovered that various sulfides could passivate the GaAs surface and improve the electronic properties [34, 35] and the combination of this passivation method with ALD (Atomic Layer Deposition) of high-κ dielectrics has been shown to improve the interface passivation of GaAs and InGaAs surfaces [36, 37]. On GaAs excellent surface passivation was obtained by in-situ deposition of $Ga_2O_3(Gd_2O_3)$ dielectric film by electron-beam evaporation from single-crystal $Ga_5Gd_3O_{12}$ [38-40], stimulating a series of dielectric device work on this material system.

3. Passivation of Ge surfaces

Initial studies on Ge suggested that a GeO_2-like passivation of this interface would be impossible, but more recent results have provided new insights into this issue. Results obtained on all in-situ grown high-κ gate stacks comprising a thermal GeO_2 layer and ALD ZrO_2 or Al_2O_3 layers show very decent CV curves on both p and n-type substrates [41]. A detailed XPS study of these layers suggests that under processing conditions where the formation of specific metal-Ge bonds can be avoided, GeO_2 provides an excellent surface passivation. These observations are also supported by first principles calculations on the GeO_2/Ge systems (fig.1) [42].

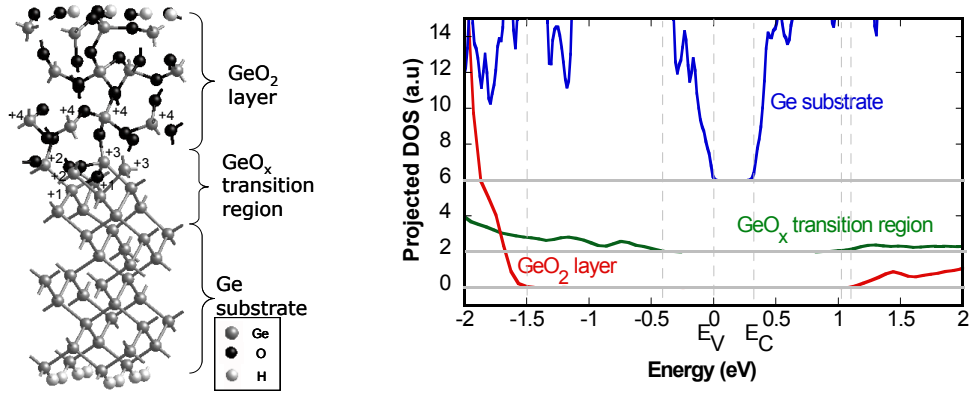


Figure 1: Simulated cell for oxidation of Ge to GeO_2, with a GeO_x transition region comprised and projected Density of States (DOS) for the Ge substrate, GeO_x transition region and GeO_2 layer, showing that neither GeO_2 nor GeO_x states fall within the Ge bandgap [42].

Good results have been shown with this passivation method for both pMOS and nMOS device [10, 11, 27, 29] using mostly relatively thick GeO_2 layers. Maintaining the performance at aggressively scaled EOT ranges around 1nm or below seems to be a major issue. Also, the relatively poor thermal stability of the GeO_2 and its high reactivity with moisture in the ambient poses a serious problem for the implementation of GeO_2 layers in a complete process flow [43, 44]. Since the GeO_2 layer is very hygroscopic full in-situ processing of GeO_2 formation and high-κ deposition must be performed. One possible solution may be to mix the GeO_2 layer with another material in order to make it more robust. Experiments carried out in a Riber 200 mm molecular beam epitaxy cluster production system [45] suggest that the formation of a aluminium germanate ($GeAlO_X$) at the high-κ/GeO_2 interface also results in well-behaved C-V curves

with very low frequency dispersion in accumulation and depletion without any significant bump [45]. This indicates that the interface state density (D_{it}) near mid-gap is small ($D_{it} \sim 2.10^{11}$ $cm^{-2}.eV^{-1}$) and the surface Fermi level is likely unpinned [45]. This mixed material can allow a further scaling of the equivalent oxide thickness of these layers by avoiding the need for a relatively thick interfacial GeO_2 layer.

One of the most successful passivation techniques for Ge pMOS gate stacks is a thin, epitaxial layer of Si on top of which a regular high-κ metal oxide such as HfO_2 can be deposited. The growth of the ultra-thin Si layer on Ge is not as trivial as it appears [46]. Si growth on Ge from Si_2H_6 in a cyclic way (Si_2H_6 adsorption at RT, followed by H_2 desorption at 550°C), results initially in a smooth Si layer that however gets rough beyond 1.5 ML, showing also Ge segregation [47]. This smooth layer was explained based on the lower surface energy of H-covered Si (from the RT Si_2H_6 chemi-sorption). Also, the epitaxial growth of SiGe alloys has often been reported to show segregation of Ge to the surface, which could be suppressed by H or other surfactants [48]. Extensive molecular dynamics simulations were done of the epitaxial growth of a Si layer on a Ge(100) surface [49]. It was found that a significant amount of Ge segregates towards the surface during Si deposition, but not as much as in the case of H-free Si deposition on Ge. Based on this understanding, a new Si deposition process was developed at lower temperature (350ºC) using a trisilane precursor [50], resulting in a reduced Ge surface segregation (figure 2). The presence of this Ge peak at the surface is expected to have a detrimental effect on the interface quality.

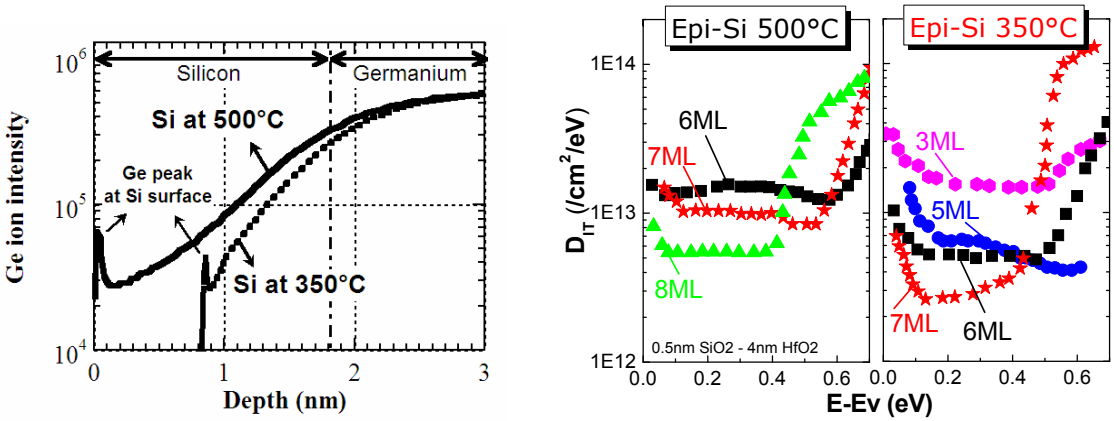
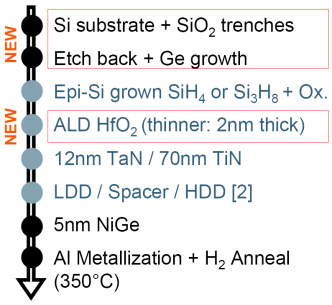


Figure 2 (left): SIMS depth profiles of Ge and Si in Si capping layer grown with SiH_4 at 500°C or Si_3H_8 at 350°C. The 350°C sample shows a reduced Ge peak at the top surface compared to the 500°C sample, as well as a steeper Ge segregation profile [51].
Figure 3 (right): Interface state density over the Ge band gap extracted from GV data performed at 80, 150, 230 and 300K for different Si thickness and grown at low (350°C) and high (500°C) temperature [52].

Using an adapted analysis technique [53], the interface states densities were extracted on Si-passivated Ge pFETs with different Si thicknesses grown at low and high temperatures (figure 3) [52]. As already reported previously [54], the extracted D_{it} profile is strongly asymmetric if silicon is used as a passivation layer for Ge devices. Moreover, the thicker the Si cap, the less symmetric profile becomes whatever the Epi-Si recipe used (350°C or 500°C). Although the physical origin of the D_{it} peak close to the Ge conduction band remains to be determined, the asymmetric profile obtained in figure could be seen as the consequence of the energy band diagram asymmetry commonly observed in Si/Ge structures [55] (E_{cSi} is lower in energy than E_{cGe}, allowing a possible quantum well formation for electrons; while, E_{vGe} is higher in energy than E_{vSi}, resulting in a hole confinement at the s-Si/Ge interface). In the lower part of the Ge band gap, a significant reduction of the D_{it} is observed for the same Si thickness using the low temperature Si passivation. This is most probably a direct consequence of the reduced Ge surface segregation that occurs during the Si deposition at a reduced temperature. It must be remarked that the thin Si passivation layer is highly strained and consequently the conduction band of the strained Si is lying ~0.55eV below the conduction band of unstrained Ge. This has a severe impact on the band diagrams of MOS devices [50]. For Ge pMOS devices in inversion the misalignment of the valence bands results in a potential well at the Ge/Si interface and a Si layer that is depleted in carriers. The inversion capacitance thus also includes the contribution of the depleted Si layer. Therefore, the Si thickness should be kept to a minimum on these devices. For Ge nMOS devices the Si passivation method is not suited since the electrons will be located in the thin Si layer rather than in the Ge substrate.

4. Ge DEVICES

Despite the promising results already reported on pFET devices using various transistor architectures [56-62], several challenges remain to be solved before they can be incorporated into high-performance CMOS technologies. The main technological challenges consist into the Ge epitaxial layer growth, the scaling of the gate dielectric and the control of the junction leakage. Recently, selective Ge growth inside the active regions of STI-patterned wafers has been demonstrated [63]. Starting from STI-patterned silicon wafers, Si is selectively etched in an ASM Epsilon 2000 reactor, followed by an epitaxial growth of undoped Ge using a GeH_4 precursor in a two-step process (450°C, H_2 carrier and 350°C, N_2 carrier). After the growth, the etching of defects revealed a TDD of $2x10^{10}$ cm^{-2}, which after a proper annealing could be reduced to $4x10^8$ cm^{-2}. The layers were found to be smooth and showed little or no facets [14]. P+/n junctions have been implanted in these layers to evaluate the diode leakage [63]. The leakage has been decoupled into the area and isolation components J_A and J_I , respectively [64]. Thin Ge layers show about 70% higher area leakage than the reference substrates. Although the most probable reason for this is the higher TDD, the fact that J_A scales nonlinearly with TDD suggests that other generation mechanisms contribute significantly to J_A as well, such as generation through defects formed by the implantations. Although J_A is increased for the thin epitaxial layers, they lead to about 5 times lower J_I, thanks to the STI that provides better isolation than the deposited oxide used for the thick substrates. Using this STI module, a 70nm Ge-pFET technology was developed allowing the scaling of EOT down to 0.85nm [65]. The key fabrication steps are summarized in figure 4. Starting from standard Si wafers with Shallow Trench Isolation (STI), the Si active area is recessed to a 300nm depth followed by a selective epitaxial growth of Ge. This STI scheme has several advantages. It provides a high-quality isolation, allows co-integration of Si and Ge-based devices and results in low topography wafers needed for the implementation of advanced processing modules. A TEM analysis of our 70nm gate length pFET with 2nm HfO_2 is shown in figure 5. Capacitance-Voltage measurements showed an EOT of 0.85nm (figure 6) with a gate leakage that follows the HfO_2 scaling line from the Si technology and remains below 0.2 A/cm^2. The ON current of the devices increases as expected with decreasing EOT and a +40% gain is observed when the EOT is scaled from 1.25nm to 0.85nm (figure 7).



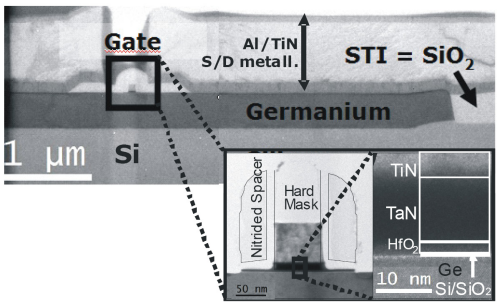
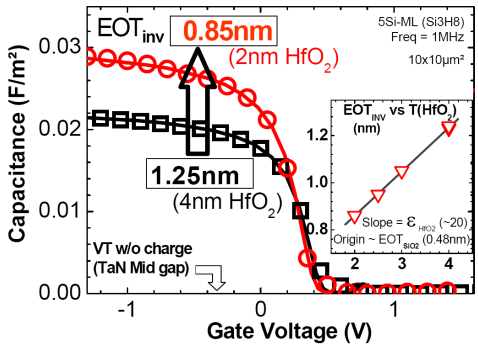


Figure 4 (left): Main steps of the process flow. Details about implants can be found in [51].
Figure 5 (right): X-SEM of the Ge-in-STI structure. The inset shows a TEM of the gate stack with 2nm of HfO_2.



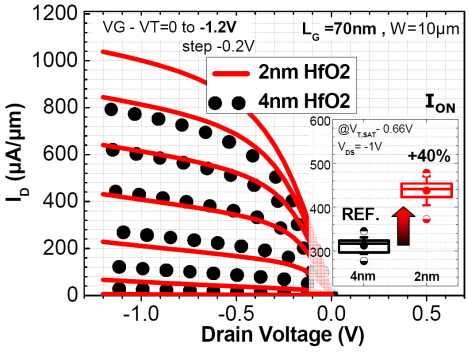


Figure 6: CV characteristics in inversion comparing different gate stacks (4 and 2nm HfO_2 pFETs). The inset shows the EOT_{inv} versus the thickness of the HfO_2 layer [65].
Figure 7: IV characteristics of 70nm Ge pFETs with 4 and 2nm HfO_2. The inset shows the I_{on} at $V_g=V_{T,SAT}(\sim 0V) - 2/3.V_{DD}$ where $V_{DD}= -1V$ [65].

5. PASSIVATION OF THE GaAs SURFACE

Unfortunately, III-V/oxide interfaces are not quite as robust as the Si/SiO_2 one and most of them present rather high densities of interface states. One of the key problems in developing inversion-mode MISFETs is the near midgap Fermi level pinning associated with the high density of states present at the high-κ/III-V interface [66-69]. The origin of these interface states has been heavily debated on in the past [70] but there are clear indications that a strong relationship exists with native antisite point defects (As_{Ga} or Ga_{As}) [69], as also evidenced by scanning tunneling microscopy data [71, 72]. It implies that the kind of high-κ material used as gate oxide has probably a secondary impact on the nature and energy distribution of the interface states and, hence, on the Fermi level pinning point. Yet, the density (D_{it}) can be strongly affected by the surface preparation (cleaning, passivation).

To illustrate these points the interface state distribution of HCl-cleaned and S-passivated GaAs-Al_2O_3 and MBE deposited GaAs-Gd_2O_3 interfaces were determined from admittance spectroscopy at room and high temperatures [73]. The 10 nm Al_2O_3 layer was deposited by ALD using $Al(CH_3)_3/H_2O$ as precursors. Prior to ALD deposition, a wet HCl clean of the 5 10^{17} n- and p-type doped GaAs wafers was performed. The 10 nm Gd_2O_3 film was deposited by molecular beam epitaxy (MBE) from the evaporation of Gd from an effusion cell and simultaneous oxidation from an oxygen plasma. Prior to oxide deposition, a clean (2x4) As-rich surface reconstruction was obtained from the desorption of a 1μm thick As-cap. Due to the presence of the oxygen plasma, a re-growth of interfacial Gallium oxides and Arsenic oxides is expected during the first stages of the deposition of the oxide. The interface state distributions are in both cases similar and show four pronounced peaks at different levels in the GaAs bandgap (figure 9). Two large peaks around the mid-gap energies dominate the interface state distribution. From DLTS measurements on the Al_2O_3-GaAs samples [74], the capture cross sections of the two mid-gap peaks were determined to be 10^{-17} cm^2 for the donor-like peak localized 0.6 eV above the valence band and 10^{-18} cm^2 for the acceptor-like peak localized 0.8 eV above the valence band. In addition to the two large mid-gap peaks, two smaller peaks close to the band-edges are also observed. These peaks are predominantly responsible for the room temperature frequency dispersion, as they lie in the measurement range of room temperature CV-measurements [75]. The S-passivated samples received an $(NH_4)_2S$ wet chemical clean before the deposition of the high-κ (ALD) and an additional 30 min forming gas anneal at 300°C afterwards. From the results, it is observed that the two large mid-gap peaks are not strongly affected by the sulfur passivation and the forming gas anneal. However, the two smaller peaks closer to the band edges are strongly reduced by the S-passivation and the forming gas anneal. Considering that the forming gas anneal mainly passivates dangling bond states at the III-V/oxide interface and that the S-passivation cleans the native oxides at the III-V interface and prevents the re-oxidation before the oxide growth [76], it is reasonable to assume that the peaks close to the band edges are caused by Ga-O, As-O, Ga dangling bond and As dangling bond states.

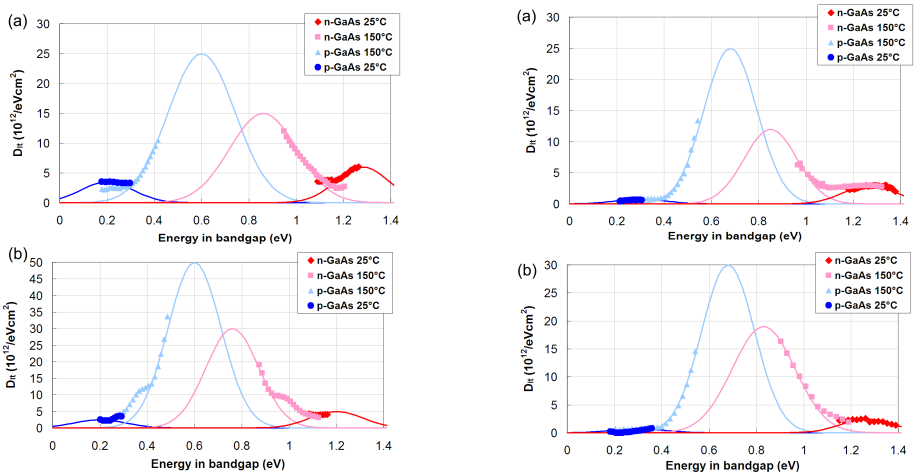
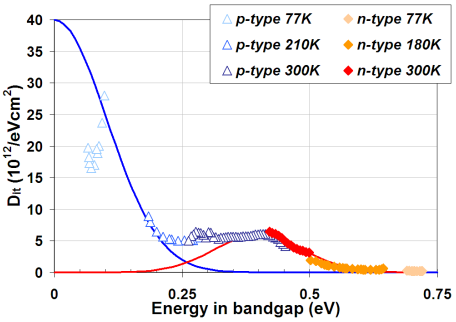


Figure 9: Left: Interface state distribution at the HCl-cleaned GaAs-Al_2O_3 (a) and MBE deposited GaAs-Gd_2O_3 interfaces (b). Right: Interface state distribution at S-passivated and forming gas annealed GaAs-Al_2O_3 (a) and GaAs-HfO_2 interfaces (b). The interface state distribution is determined from admittance spectroscopy at room and high temperatures. The solid lines are Gaussian peak fits to the experimental data points (symbols). Zero energy corresponds to the valence band edge energy [73].

Although the S passivation and the forming gas anneal can reduce the interface state density close to the band edges, there remains a very large interface state density around mid-gap energies. Since the nature of the oxide does not seem to have any influence on the mid-gap interface state density, it can be suggested that these defect peaks are caused by intrinsic GaAs defects. The most likely cause for this large mid-gap energy peaks is the generation of a large density of Ga- and As-vacancies at the interface, caused by the physical stress of the amorphization of the interface. The dynamics of this process have been shown by first-principles molecular dynamics simulations of the oxidation of GaAs [77, 78]. A qualitative model for the growth of the native oxide (few monolayers thick) and the formation of the interface with the GaAs substrate was derived [78]. The analysis of the local density of states (DOS) shows that the defect gap states arise from the aggregate of As dangling bonds due to the Ga vacancy, while the electronic states at the conduction band edge correspond to an As–As wrong bond present at the interface [78].

A typical interface state distribution of the $In_{0.53}Ga_{0.47}As$-Al_2O_3 interface is shown in figure 10. The 10^{17} cm^{-3} doped $In_{0.53}Ga_{0.47}As$ was grown lattice matched on InP(001) substrates. ALD, using $Al(CH_3)_3/H_2O$ as precursors, was used to deposit a 10nm Al_2O_3 layer, followed by a subsequent 30 min forming gas anneal at 300°C. Prior to oxide deposition, the $In_{0.53}Ga_{0.47}As$ sample received an $(NH_4)_2S$ wet chemical clean. The interface state density is dominated by two peaks, one large peak close to (and probably partly in) the valence band and one smaller peak around mid-gap energies. Both interface state peaks seem to be donor-like and are uncharged, when the Fermi level is close to the conduction band, which allows for relatively large I_{on} and carrier mobility (figure 11) usually measured in $In_{0.53}Ga_{0.47}As$ -based nMOSFET devices [79, 80], despite the large overall interface state density.



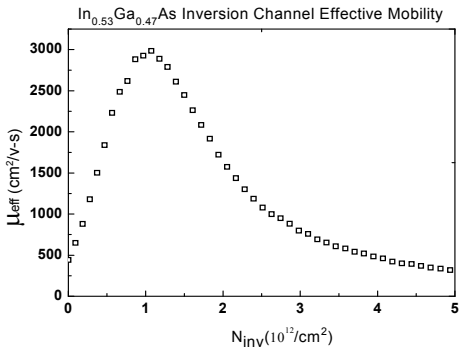


Figure 10 (left): Interface state distribution at S-passivated and forming gas annealed $In_{0.53}Ga_{0.47}As$-Al_2O_3 interfaces as determined from admittance spectroscopy at room and low temperature [73].
Figure 11 (right): Extracted channel field-effective mobility versus inversion charge density for self-aligned inversion channel n-MOSFETs fabricated on p-type $In_{0.53}Ga_{0.47}As$ on InP wafer with a $(NH_4)_2S$ surface treatment and 10 nm Al_2O_3 ALD gate dielectric [80].

Deep Level Transient Spectroscopy (DLTS) has been applied to MOS capacitors fabricated on n- and p-type GaAs and on n-type $In_xGa_{1-x}As$ epitaxial layers deposited by MBE on GaAs substrates [74]. The gate dielectric consists of 10 nm ALD Al_2O_3. It was shown that the dominant deep levels in the case of GaAs substrates are two broad interface-state-related bands centered around midgap, consistent with previous findings for a variety of gate dielectrics on GaAs. At the same time, it was observed that the interface state peak shifts closer to the conduction band for the $In_xGa_{1-x}As$ layers, whereby the activation energy becomes smaller for higher x. However, it was demonstrated that in this case not only interface states contribute to the DLTS emission signal but also deep levels associated with threading dislocations in the relaxed layers. This contribution grows progressively with the In content, i.e., with the amount of relaxation. From this, it is concluded that $In_xGa_{1-x}As$/GaAs substrates are not favorable for inversion-type of MOS devices due to the increasing impact of the TDs on the device performance.

6. Device structures for high-mobility materials

Since inversion mode devices do not seem to be the appropriate device for III/V based logic applications, other device types have been explored. It is well known that research on MOSFETs made of GaAs and other III-V compounds has started many years ago. However, III-V MOSFETS offering improved isolation at the gate have been studied in the past as improved versions of MESFETs and HEMTs in the context of analog, high-frequency/low-noise and low-density LSI

niche market applications. Due to their architecture which is based on buried-channel heterostructures and ohmic source/drain contacts, they operate in majority carrier enhancement or depletion mode and with insufficient electrostatic control over the channel, which are both the least compatible with CMOS. Traditional High Electron Mobility Transistors (HEMT's) are optimized for high-frequency applications or fiber-optic front end systems and have a relatively large source/drain (S/D) separation, resulting in a poor device pitch. Various studies [81, 82] have shown that reducing the distance between the gate electrode and the quantum well channel (QW) is key to allow scaling below 100nm gate length. A possible concern is that a δ-doping layer is present between the gate and the QW, which might prevent this distance to be reduced further. Therefore, the influence of removing this δ-doping layer under the gate was investigated [83], based on TCAD simulations. The proposed device enables VLSI-compatible processing by self-aligned S/D definition. The device performance was investigated by simulations performed on Si/Ge devices. Figure 12(a) offers a schematic view of the reference structure. On a Si substrate, a Ge QW with a thickness of 3 nm is deposited, capped with a Si spacer layer (h_{sp} = 5nm) containing a δ-doping layer (p-type 5.10^{12} cm^{-2}, 2.5 nm above the channel). On top of this a gate electrode is placed (L_G = 30nm) with a gate oxide of 0.5 nm SiO_2. 5 nm SiO_2 spacers isolate the gate laterally. This structure resembles a classical III-V HEMT and while this study focuses on the Ge-based QW pFET, one can expect similar behavior for III-V devices. Figure 12(b) shows the alternative QW device, where the δ -doping under the gate and spacers has been omitted. In turn, this allows bringing the gate closer to the channel, which was done in figure 12(c) (h_{sp} = 2 nm).

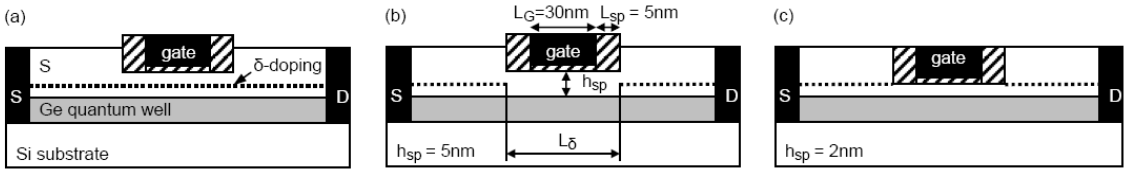
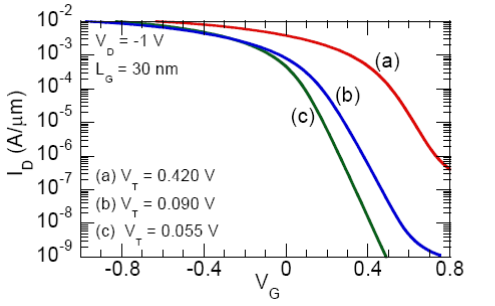


Figure 12: Classical quantum well transistor structure (a), QW transistor with interrupted δ-doping (b) enabling EOT scaling (c) [83].

I_D-V_G curves (at V_D = V_{DD} = -1V) for the structures depicted in figure 12 were simulated using sdevice (TCAD Sentaurus, [84]) (figure 13). The mobility model implementing impurity scattering in Ge was calibrated using data from literature [85]. The reference structure (a) has a V_T of 420 mV. Removing the δ-doping layer under the gate and spacers results in a V_T decrease of 330 mV. This can be understood by considering that an interruption of the δ-doping reduces the charge in the QW-channel. Also, removing the δ-doping layer does not change the sub-threshold behavior for structure (b). The advantage of interrupting the δ-doping is that it allows bringing the gate closer to the QW channel. As shown in figure 13, this leads to better gate control and superior scalability. The sub-threshold slope (SS) is reduced from 104 tot 77 mV/dec, while Drain Induced Barrier Lowering (DIBL) is also improved from 155 to 84 mV/V.



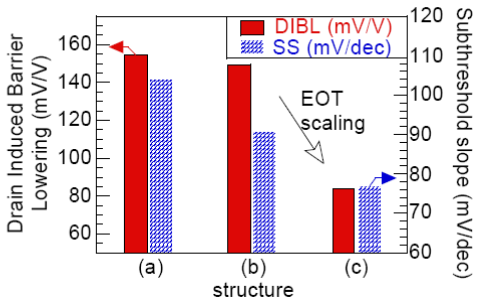


Figure 13 (left): I_D-V_G curves for the devices in fig. 1. An Improvement in sub-threshold behavior can be observed in (c) [83].
Figure 14 (right): Sub-threshold slope and Drain Induced Barrier Lowering for the structures in fig. 1, illustrating improved short channel control for structure (c) [83].

The relatively large S/D separation in traditional QW devices results in poor device pitch. Self-aligned S/D definition can be achieved by growing doped selective epitaxial S/D areas. A silicide can then be formed in a next step, allowing dense circuits. The doped S/D epitaxial layers serve both as a charge carrier supply for the QW (replacing as the interrupted δ-doping) and as a contacting layer. In the devices presented here, the doped S/D layer is separated from the QW channel by 1nm of undoped Si. While the proposed self-aligned contacting scheme allows for denser circuits, the series

resistance added by the tunneling barrier between the QW-channel and the epitaxial S/D areas should remain minimal. The total series resistance Rs of the device was estimated using TCAD. Two contributions can be distinguished: R_{spacer} is the resistance of the QW-channel under the spacer, while R_{tunnel} covers the tunneling barrier. As can be expected R_{tunnel} varies both with the length of the S/D contact and with the doping concentration in the epitaxial S/D. A lower doping level results in a thicker tunneling barrier and hence a higher value for R_{tunnel}. Also, larger contacts result in a lower value for R_{tunnel}. It was found that for S/D doping levels above 2.10^{20} cm^{-3} the total series resistance of the device remains limited to values below 80 Ω.µm unless the spacer length increases beyond 10nm. This increase can be explained by the fact that a portion of the QW is depleted of carriers (i.e. no holes are supplied from the S/D areas or from the gate in the portion under the spacers), resulting in a highly resistive segment of the QW under the spacer. The main advantages of the IF-QW devices are high mobility, better immunity to interface states, potential for more efficient channel formation, reduction of coulomb scattering at the S/D regions, better immunity to variability resulting from dopant fluctuations at reduced dimensions. In addition, the QW is in-line with the trend to develop thin-film channel technology for future nodes, while its thickness scales with Lg in a similar way to SOI body thickness implying that the QW channel approach may retain electrostatic integrity with reduced short channel effects.

7. TUNNEL-FET's

For future technology generations, it is very important to be able to scale the supply voltage beyond the current ~1V plateau. The latter scaling is a necessary condition for a reduction of the power consumption per transistor. In order to this with a sufficiently large I_{on}/I_{off} current window, devices with a subthreshold swing below the 60mV/decade limit of the MOSFET devices are needed. Tunnel-FETs (TFETs) have the potential to achieve these goals [86]. The TFET is in essence a reverse biased p-i-n diode with a gate (figure 15a). The gate action can induce a strong band bending at the source-channel interface such that tunnel path lengths decrease (figure 15b). The tunnel current then increases according to an exponential dependence on the tunnel path length. Silicon-based TFETs are the most attractive because they allow for a full re-use of the existing expertise in fabricating high-quality silicon-compatible gate dielectrics. However, the small band-to-band-tunneling efficiency in large-bandgap silicon results in low ON-currents of the all-silicon TFETs. To improve the ON-currents while maintaining a silicon channel, the incorporation of heterostructures has been proposed [87-89]. In general, it was shown that the largest ON-current is achieved in an *n*-channel heterostructure TFET with a small-bandgap material in the source region and a large positive electron affinity offset between the source and the channel material [87]. The ON-current of such a heterostructure TFET is boosted beyond the ON-current of the homostructure TFET, out of either of the two materials of the heterostructure. In particular, it was demonstrated that the Ge-source Si-TFET maintains the low OFF-currents of an all-silicon TFET, while boosting the ON-current to the same level as state-of-the-art MOSFETs, which corresponds to a boost of more than an order of magnitude. As complementary p-TFET, the indium(gallium)arsenide-source silicon-channel TFET was proposed (figure 16).

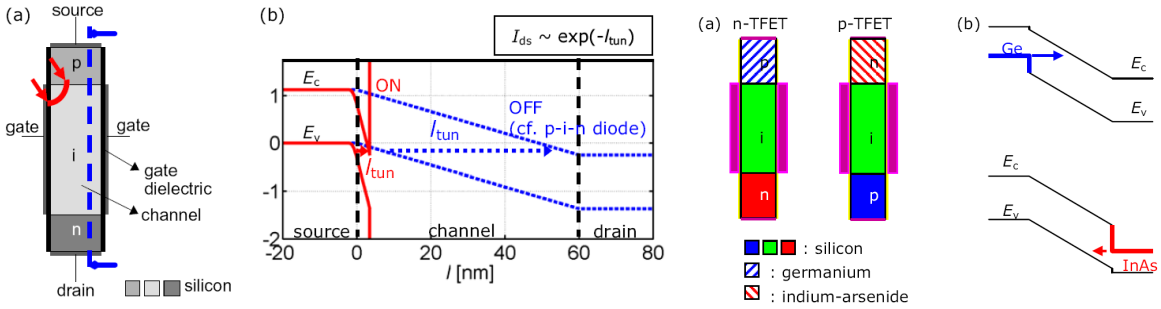


Figure 15 (left): (a) Schematic representation of the cross-section of a nanowire-based TFET. (b) Positions of the band edges along the cut-lines marked in (a), indicating the difference in tunnel-path length l_{tun} between the ON-state and OFF-state of the TFET [86].

Figure 16 (right): (a) Schematic representation of complementary heterostructure Si-based TFETs. (b) Schematic representation of the positions of the band edges corresponding to a cutline from source to drain of the configurations in (a). The p-doped section is at the left and the n-doped at the right for both drawings [86].

The operating principles of TunnelFET's were investigated using complementary Multiple-Gate Tunneling Field Effect Transistors (MuGTFETs) [90], implemented in a MuGFET technology compatible with standard CMOS-processing. The TFET devices (gated P-i-N diodes) were fabricated on a (100) SOI substrate with 65nm thick Si film on top of a

145nm BOX. Fin widths down to 25nm were patterned using 193nm optical lithography and aggressive resist and hardmask (HM) trimming. The channel of the device was left undoped. The gate stack consists of a 100nm poly silicon layer on top of a 5nm MOCVD TiN layer, a high-κ 2nm ALD HfO_2 on a 1nm interfacial oxide. After gate patterning, complementary source/drain doping was obtained by an As/BF_2 extension implantation at 45° tilt parallel to the gate using a modified mask design. Then, 50nm wide RTCVD nitride spacers were formed on a 5nm PECVD oxide liner. After HDD implantations, a 1050°C spike anneal was given followed by NiSi silicidation. No selective epitaxy was performed in the SD regions.

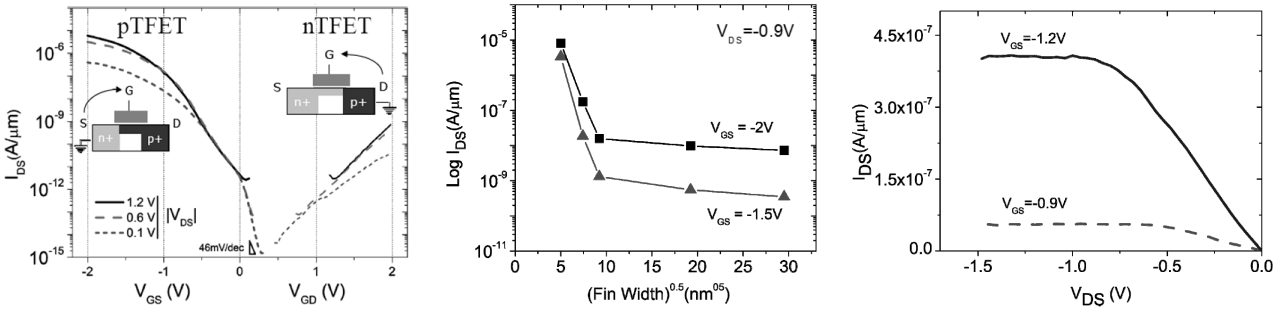


Figure 17 (left): pTFET and nTFET input characteristics for a 25nm wide fin (Lg=160nm) [90]. The side where the tunneling occurs is kept grounded [90].
Figure 18 (middle): W_{fin} dependence for different V_{GS} (L_g=160nm). Sharp increase of the tunneling current observed for narrow fins [90].
Figure 19 (right): I_{DS} vs V_{DS} for the 25nm wide fin (L_g=160nm) [90].

N- and p-type tunneling currents are observed on the same device structure and the input characteristics are shown in figure 17. Better performance is found for pTFET operation than for nTFET, likely due to the sharper junction profile at the N^+ side because of the lower diffusivity of arsenic used as n-type dopant, compared to boron at the P^+ side. An I_{on}/I_{off} ratio of 10^6 at a V_{DD} of 1.2V is obtained for the pTFET operation. A minimum point slope of 46mV/dec is extracted at low bias (V_{GS}=0.2V, V_{DS}=-0.1V) for the 25nm wide fin device, in line with previous reports of minimum point slope in planar TFETs for very low bias [91, 92]. MuGFETs are very attractive for CMOS technology because of their very good electrostatic control of the gate over the channel. In TFETs, the improved gate control over the channel potential is also expected to improve the tunneling current. For this reason the impact of the fin width on the TFET characterictics was investigated. A plot of the ON current versus square root of the fin width clearly shows a sharp increase for fins below 80nm, where the two gates at the sidewalls of the fin become coupled to each other (fig. 18). The output characteristics (fig. 19) show a perfect saturation of the device resulting in very low small-signal output conductance, making these devices very attractive for analog circuits. At low gate voltages an increase of the current was observed for large reverse bias, corresponding to an onset of tunneling at the opposite junction. No dependence on the gate length was found down to 160nm. For very long channels, a slight decrease is observed due to the large resistance of the undoped channel. A very weak dependence of the tunneling current on the temperature was measured, which is characteristic of tunneling. The OFF current showed an increase with the temperature proportional to the intrinsic carrier concentration, n_i, in line with the SRH generation current [93].

To ensure a high quality of the heterostructure interface in these heterostructure TFETs, nanowire-based configurations are a very promising implementation. The Ge-Si interface is expected to have a lower defect density (lattice mismatch of 4%) than the $In_{0.6}Ga_{0.4}As$-Si interface (lattice mismatch of 8.5%). However, the larger strain in the latter heterostructure may allow for a lower In-content in the InGaAs-source and therefore, a smaller lattice mismatch, while still maintaining high tunnel currents, because bandgaps are typically decreasing with strain. Except for a change of material, the doping density is also abruptly changing at the heterostructure interface and, as indicated by device simulations, the best TFET performance is achieved for both a high source doping density and an as steep as possible doping gradient. A top-down integration scheme for silicon vertical nanowire (NW) short-gate tunnel field-effect transistors (TFETs) with a 35nm nanowire dimension and using state-of-the-art metal gate and high-k gate dielectric was demonstrated [94]. The devices are fabricated using a process flow schematically illustrated in figure 20. The channel region and the top junction are obtained by undoped blanket epitaxial layer. The nanowires are formed by a top-down approach using an oxide hardmask (HM) and e-beam lithography. Nanowire dimensions down to 30nm were obtained. The bottom oxide isolation serves two purposes: 1) to isolate the gate from the substrate to reduce gate leakage, 2) to avoid an overlap of

the gate to the drain to reduce the tunneling at the drain side. The gate stack consists of 2nm ALCVD HfO_2, 10nm MOCVD TiN and 25nm LPCVD amorphous Si. The final gate length of the device is defined by the combination of the height of the nanowire, the gate hardmask thickness, the gate recess after etching and the thickness of the bottom oxide. In this work, the final gate length of the device is ~200nm. Gate length variation, however, is known not to affect significantly the tunneling current. The top contact is isolated from the gate by a nitride spacer. It is implemented by the deposition of a doped, amorphous Si capping layer and connects multiple NWs together. This layer also avoids over-silicidation of the very small NWs, similar to what is observed in FinFET processing. Electrical characterization is carried out by direct probing on silicide using a nanoprober setup. A TEM cross-section of the final vertical nanowire TFET is illustrated in figure 21.

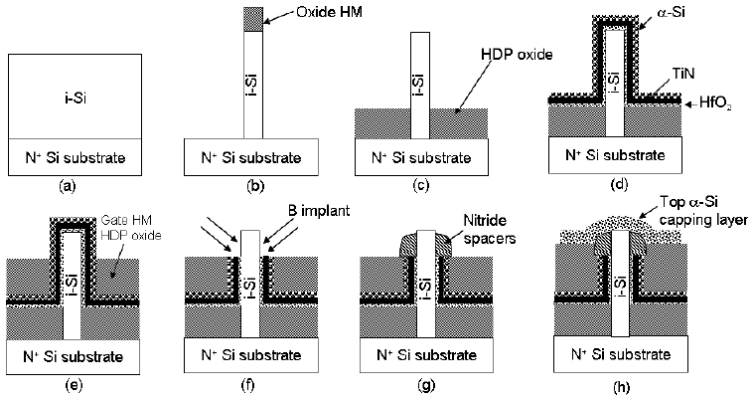


Figure 20: Schematic illustration of the process flow of the vertical nanowire silicon TFET (a) blanket epitaxy on highly doped substrate, (b) NW patterning using e-beam lithogrpahy (c) bottom isolation (d) Metal gate/high k stack deposition (e) Gate HM formation (f) Gate etch and top junction implantation (g) top nitride spacer formation (h) capping layer formation for nanowire array [94].

The input and output electrical characteristics of the 35nm diameter vertical NW nTFET are shown in figures 22 and 23. In figure 22, the curves are overlaid for different drain voltages as the gate to source voltage remains unchanged. In this device, the subthreshold slope is ~300mV/dec with a I_{on}/I_{off} ~1E5 at V_{GS}=3V. In figure 23, the tunneling current is flat with drain voltage, as expected. The device performance is not yet beyond the one of MOSFETs, likely due to the use of silicon and its large bandgap and the poor abruptness of the top junction obtained by implantation and large boron diffusion at rather low temperatures, but it acts as a proof-of-concept. A doped junction obtained from epitaxial growth along with low thermal budget processing would improve the junction profile and boost the performance. This implementation is currently under investigation.

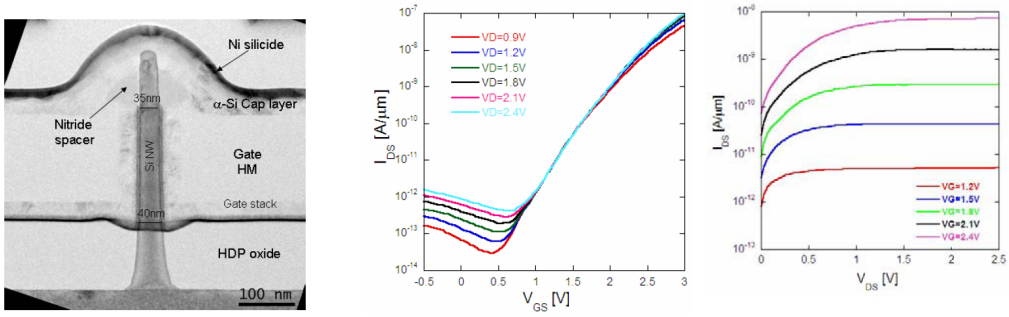


Figure 21 (left): TEM cross-section of the final vertical 35nm NW TFET device [94]
Figure 22 (middle): I_{DS} vs. V_{GS} in a 35nm diameter vertical NW n-TFET for different $V_{D=N+}$. ($V_{S=P+}$ = 0V) [94]
Figure 23 (right): I_{DS} vs. V_{DS} in a 35nm diameter vertical NW n-TFET for different V_G. ($V_{S=P+}$ = 0V) [94]

Instead of using etched nanowires, such vertical devices can also be made using grown nanowires (NW). In heteroepitaxial surface-bound NW growth, whereby the NW is lattice mismatched with respect to the underlying substrate, one unique feature of adopting a NW geometry is the small NW/substrate interface, especially when NWs are grown perpendicular to the substrate. Although in some cases the lattice mismatch between the III/V semiconductor and the substrate can be significant (e.g., ~11% for the InAs/Si system), the growth of high aspect ratio nanostructures such

as NWs allows for less stress at the interface, also considering differences in thermal expansion coefficients. By adopting bottom-up CMOS-compatible technology routes, it is possible to exploit the peculiar electronic and optical properties of III/V semiconductors. The technology to grow III/V semiconductors belonging to the (Al,Ga,In-) (N,P,As,Sb) system in bulk form has been applied with success to NW growth [95, 96]. The use of these one-dimensional (1-D) nanosized objects (whether group-IV or -III/V) paves the way for aggressive downscaling. Several NW growth experiments employ a catalyst, usually Au [97, 98]. In this case, a mechanism called vapor-liquid-solid (VLS) growth takes place (fig. 24a) [99]. In detail, first the Au particle reacted with Si to form droplets of liquid AuSi (eutectic). Then, additional Si from the gas dissolved into the droplets, supersaturating them with Si. The droplets remained on the tips of the whiskers and allowed them to continue growing. VLS growth is widely used today to achieve precise control of NW morphology while providing high quality single-crystal materials. The VLS approach also enables in situ doping through the metal catalyst and the formation of complex axial and radial heterostructures. However, the use of a metal catalyst, and especially Au, introduces the potential for unintentional incorporation of impurities. Catalysts such as In [100], Al [101] and Ni [102] have been used to replace Au for NW growth, with results not as satisfactory as for Au in terms of growth control and tailoring of NW properties. Materials such as GaN are known to form NWs without a catalyst quite easily [103]. In the III/V NWs, e.g., InAs and GaAs, selective area vapour phase epitaxy (SA-VPE) seems to be a very promising technique [104], especially on lattice-mismatched substrates. To grow surface-bound NWs by SA-VPE, a ~50 nm thick dielectric mask is typically patterned on a substrate, and dry/wet etching defines openings of generally 50–200 nm diameters (fig. 24b). Metal-organic or gaseous precursors are flown onto the heated substrate, and growth occurs only in the exposed substrate regions. Tuning of the growth conditions induces NW growth in a specific direction by epitaxy. Recent experiments of selective-area metal-organic vapor-phase epitaxy (SA-MOVPE) of InAs NWs on Si resulted in nanostructures of quality comparable to those grown by VLS [96, 104]. Substrate preparation was found to be very critical, as it is generally the case for planar, nonselective epitaxy. Despite the fact that the lattice mismatch problem in heteroepitaxy is a stronger concern than in VLS growth, very good results were achieved with this technique, as illustrated by the results shown in figures 25 and 26 [96]. This illustrates a possible route towards a progressive integration of III/V NW growth technology in current Si-based CMOS processing based on this method.

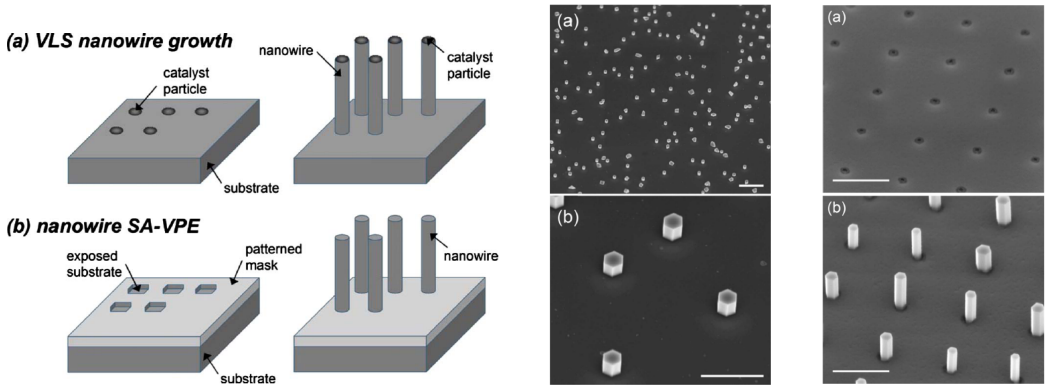


Figure 24 (left): Schematics of (a) catalytic VLS NW growth and (b) noncatalytic NW SA-VPE.
Figure 25 (middle): InAs NWs grown by MOVPE on blanket Si (111) substrates treated with toluene. The (111)-oriented NWs measure ~300 nm in diameter [96].
Figure 26 (right): InAs NWs grown by SA-MOVPE on a TEOS/Si3N4-masked Si (111) substrate patterned with 100 nm diameter holes. (a) The patterned Si substrate is subjected to NW growth (b) [96].

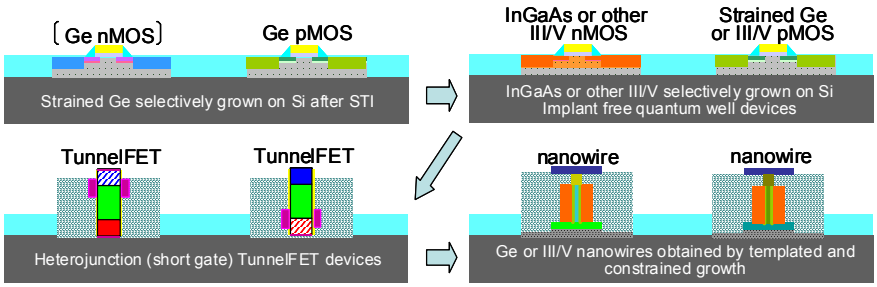


Figure 27: A schematic illustration of how new materials and devices can shape the future of CMOS technology.

10. CONCLUSIONS

A possible roadmap for the future of advanced CMOS is shown in figure 27. High-performance CMOS can be obtained by introducing high mobility channel materials such as Ge and III/V compounds. The introduction of these advanced materials will go together with the introduction of new device concepts such as highly scaled quantum well devices. Novel structures such as heterojunction Tunnel-FET's can fully exploit the properties of these new materials and provide superior performance at lower power consumption by virtue of their improved subthreshold behavior, allowing to reduce the supply voltages. Vertical surround gate devices can be produced from nanowires allowing the introduction of a wide range of materials on Si.

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