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On the interface state density at $In_{0.53}Ga_{0.47}As$/oxide interfaces

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The authors model the capacitance-voltage (*CV*) behavior of $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor (MOS) structures and compare the results to experimental *CV*-curves. Due to the very low conduction band density of states, ideal III-V MOS structures should present an asymmetric *CV* behavior, with lower accumulation capacitance on the conduction band side. The absence of this asymmetric *CV* shape in experimental *CV* curves points toward the presence of additional states inside the conduction band at the oxide-semiconductor interface. Comparisons between the model and experimental data allow the determination and approximate quantification of a large acceptorlike interface state density above the conduction band edge energy.
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Recent advances in the fabrication of $In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor field-effect transistor devices[1–5] have led to an increased interest in III-V devices for application as high performance transistors for complementary metal-oxide-semiconductor (CMOS) generations beyond the 16 nm node.[6] One of the numerous challenges being investigated is the reduction in the interface state density (D_{it}) at the III-V oxide interface. Using the conductance method,[7,8] the interface state distribution in the $In_{0.53}Ga_{0.47}As$ bandgap has been measured recently, showing an asymmetric D_{it} distribution with a large donorlike interface state peak below midgap and a lower donorlike interface state density above midgap.[3,5,9–11] The interface state density inside the conduction and valence band on the other hand cannot be measured with the conductance method and accessing the D_{it} inside the conduction band is not trivial. In the present paper we will model the electrostatic behavior of $In_{0.53}Ga_{0.47}As$ MOS structures, in order to compare experimental *CV* curves with simulated ones, thereby concluding on the interface state distribution in the lower part of the conduction band.

The modeling approach is the same as for classical Si MOS structures,[12] where one starts from the Poisson equation

$$\frac{d^2V(x)}{dx^2} = E(x)\frac{dE(x)}{dV(x)} = -\frac{e[N_d - N_a + p(x) - n(x)]}{\varepsilon_s}. \quad (1)$$

Here, N_d and N_a are the donor and acceptor concentrations in the semiconductor, which are supposed to be constant, $n(x)$ and $p(x)$ are the electron and hole densities and ε_s is the dielectric constant. Integrating Eq. (1) from the bulk of the semiconductor into the depletion region, yields the electric field $E(x)$ inside the semiconductor as a function of the potential $V'(x)$ inside the semiconductor

$$E[V'(x)] = 2\ \mathrm{Sign}(\Phi_s) \times \sqrt{\int_{\psi_B}^{V'(x)} -\frac{e\{N_d - N_a + p[V(x)] - n[V(x)]\}}{\varepsilon_s} dV(x)}, \quad (2)$$

where Φ_s is the surface potential of the semiconductor, which is chosen to be zero at the flatband position. Here it should be noted that, as the density of states in the III-V conduction band is low, the Fermi level can be allowed to travel quite far into the conduction band. It is therefore of upmost importance to use the exact electron density for degenerate semiconductors and not the exponential Boltzmann approximation only valid inside the semiconductor bandgap

$$n[V(x)] = \frac{2\sqrt{\pi}}{(kT)^{3/2}} N_C \int_{E_C}^{\infty} \frac{(E - E_C)^{1/2}}{1 + e^{[E - V(x)]/kT}} dE, \quad (3)$$

where E_C is the conduction band edge energy, N_C is the effective density of states in the semiconductor conduction band and T is the temperature.

Applying Gauss theorem on a cylindrical surface of section s=1 and axis x, of which one of the bases is at the semiconductor interface and the other inside the bulk of the semiconductor, yields $E_s = -Q_s/\varepsilon_s$, where Q_s is the net charge inside the semiconductor and E_s is the electric field at the semiconductor surface. This permits us to calculate the charge inside the semiconductor Q_s as a function of the surface potential Φ_s

$$Q_s(\Phi_s) = -2\ \mathrm{Sign}(\Phi_s) \times \sqrt{\int_{\psi_B}^{\Phi_s} -e\varepsilon_s\{N_d - N_a + p[V(x)] - n[V(x)]\} dV(x)}. \quad (4)$$

The semiconductor capacitance C_s can then be written as

$$C_s(\Phi_s) = -\frac{dQ_s(\Phi_s)}{d\Phi_s}. \quad (5)$$

The total capacitance of the MOS system is given by

$$\frac{1}{C_{tot}(\Phi_s)} = \frac{1}{C_{ox}} + \frac{1}{C_s(\Phi_s) + C_{it}(\Phi_s)}, \quad (6)$$

where C_{ox} is the oxide capacitance and C_{it} is the capacitance added by the charged interface states

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$$C_{it}(\Phi_s) = \frac{d\left(\int_{\Phi_s}^{+\infty} D_{it,D} dE - \int_{-\infty}^{\Phi_s} D_{it,A} dE\right)}{d\Phi_s}. \quad (7)$$

Here $D_{it,D}$ is the donorlike interface state density and $D_{it,A}$ is the acceptorlike interface state density.

Finally, the relationship between gate voltage V_G and surface potential Φ_s is given by

$$V_G = \Phi_s + \phi_m - \phi_s - \frac{Q_s(\Phi_s)}{C_{ox}} - \frac{Q_{it}(\Phi_s)}{C_{ox}}, \quad (8)$$

where φ_m and φ_s are the metal and semiconductor work functions, respectively, and $Q_{it}(\Phi_s)$ is the interface state charge at the semiconductor surface

$$Q_{it}(\Phi_s) = \int_{\Phi_s}^{+\infty} D_{it,D} dE - \int_{-\infty}^{\Phi_s} D_{it,A} dE. \quad (9)$$

Equations (6) and (8) allow us to calculate the thermal equilibrium *CV* behavior of a MOS structure, which can be compared to experimental data. All values for the different material parameters were taken from Ref. 13.

The devices used in this work consist of 2×10^{17} cm^{-3} n- and p-type doped $In_{0.53}Ga_{0.47}As$ layers grown lattice matched on, respectively, n- and p-type doped InP substrates. The top surface was cleaned with $(NH_4)_2S$ before atomic layer deposition (ALD) of a 10 nm thick Al_2O_3 dielectric film, using as precursors trimethylaluminium and H_2O. On top of the dielectric, 50 nm thick Pt metal dots were deposited through a shadow mask. The full stack was then annealed in forming gas at 400 °C during 5 min. Quasistatic *CV* curves were acquired using an Agilent 4156C parameter analyzer, using 0.1 s as the integration time, which should be sufficiently long for achieving full thermal equilibrium in the $In_{0.53}Ga_{0.47}As$ MOS system. Increasing the integration time further did not lead to any changes in the *CV* curves anymore.

Figure 1 shows the experimental (symbols) and simulated (solid line) *CV*-curves of the n- and p-type $In_{0.53}Ga_{0.47}As$ MOS capacitors. A good fit to both the n- and p-type *CV* curves could be obtained using the interface state density as shown in Fig. 2 and an oxide capacitance of 0.8 $\mu F/cm^2$. This value corresponds well to the expected value for a 10 nm thick Al_2O_3 layer with a relative dielectric constant of 9. The Al_2O_3 layers on $In_{0.53}Ga_{0.47}As$ were characterized extensively using transmission electron microscopy and internal photoemission, in order to assure the correct film thickness and the absence of a substantial interfacial layer.[14] The *CV* curve of an ideal device without any interface states is shown as well (dashed line). Finally, the semiconductor charge Q_s and the gate voltage V_G as a function of surface potential Φ_s corresponding to the two simulations of Fig. 1 are shown in Fig. 3. From the simulation of the ideal structure it becomes clear that the *CV* curve, in absence of any interface state density, should have an asymmetrical behavior, with the capacitance on the conduction band side being lower than on the valence band side.[15] This behavior is due to the low density of states in the conduction band, which actually leads to a semiconductor capacitance C_s that becomes never large compared to C_{ox} [See Eq. (6)]. The larger the value for C_{ox}, the stronger this asymmetry will become. In the experimental measurements on Fig. 1 this asymmetry cannot be observed. A good fit could nevertheless be obtained, if one includes a large density of acceptorlike interface states inside the conduction band, with the shape and density as shown in Fig. 2. The interface state density inside the band gap, by the way, is in agreement with the density of states derived from applying the conductance method on the very same devices.[4,9]

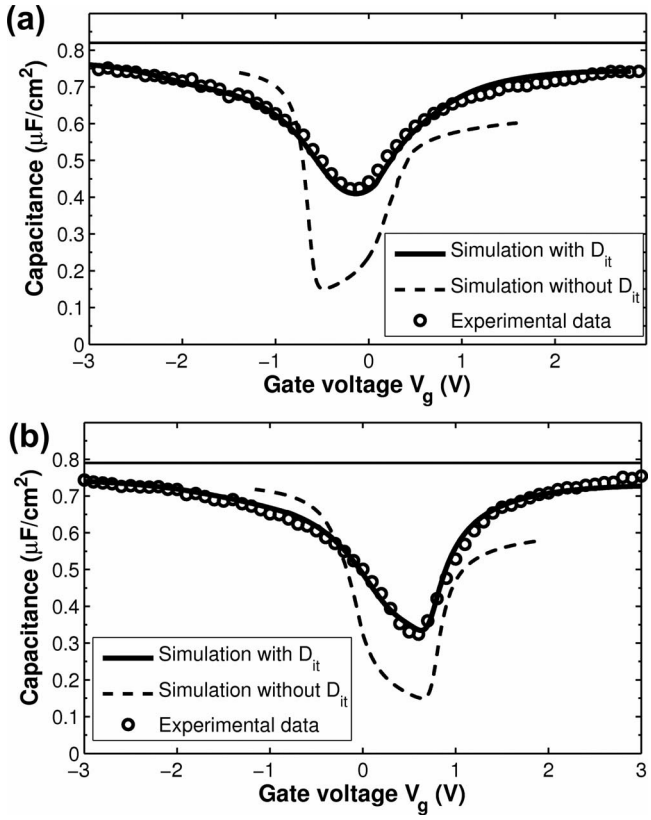

FIG. 1. Experimental (symbol) and simulated n-type (a) and p-type (b) $In_{0.53}Ga_{0.47}As$-10 nm Al_2O_3-Pt MOS *CV*-curves with the interface state density of Fig. 2 (solid line). An ideal, simulated *CV*-curve without any interface states is shown as well (dashed line).

Charge quantization effects and nonparabolic bands[16] are not included in this model. These two phenomena nevertheless have opposing effects on the capacitance, such that their

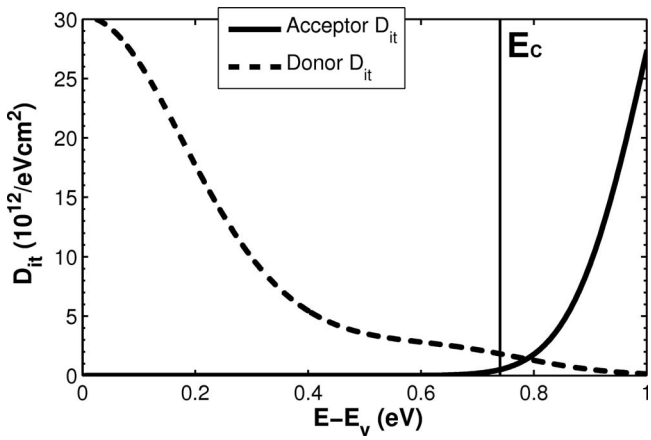

FIG. 2. The interface state distribution used for the calculations in Figs. 1, 3, and 4. Zero energy corresponds to the valence band edge energy.

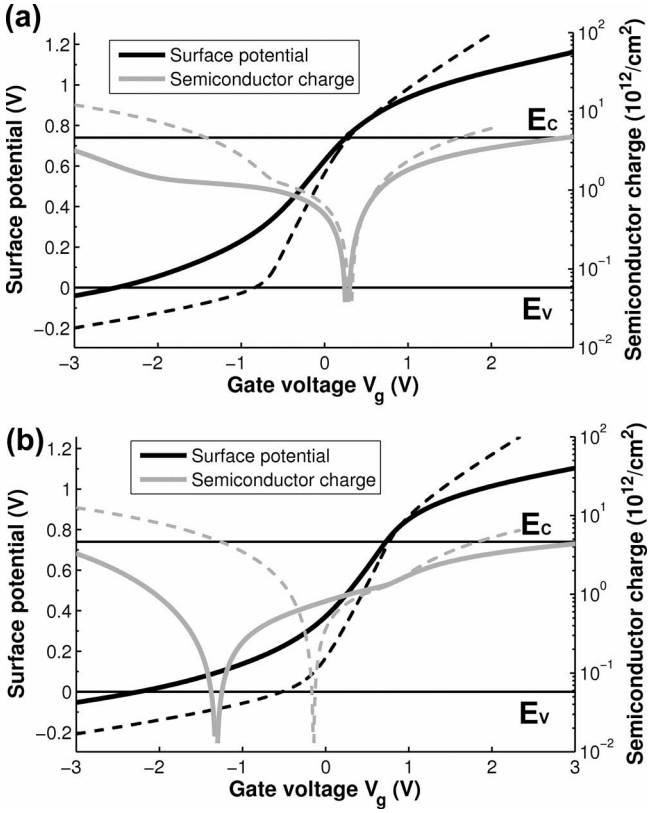

FIG. 3. Simulated surface potential (black line) and semiconductor charge (gray line) as a function of gate voltage for the n- (a) and p-type (b) $In_{0.53}Ga_{0.47}As$ MOS structures. Simulated curves for an ideal III-V oxide interface without any interface states are shown as well (dashed lines).

overall effect is most likely small. Future work could try to include these two effects into the simulations, in order to rule out any strong effect of these two phenomena on the *CV* curve.

Finally, Fig. 4 shows the calculated semiconductor charge and gate voltage as a function of surface potential, for a p-type $In_{0.53}Ga_{0.47}As$ MOS structure with an oxide capacitance of 4.5 $\mu F/cm^2$ and the interface state density as shown in Fig. 2 (solid lines). A simulation for the ideal case without any interface states is shown as well (dashed lines). The metal work function of 4.85 eV was chosen in order to place the zero bias surface potential at around the midgap energy. The figure shows that at $V_G=0.8$ V a mobile electron density of 3×10^{12} cm^{-2} can be obtained at the semiconductor surface, whereas about 10^{12} cm^{-2} carriers are lost into immobile interface states, and these ionized states will have a degrading effect on the mobility of the free carriers in the channel.

We have shown that agreement between modeled and experimental $In_{0.53}Ga_{0.47}As$ quasistatic *CV* curves can be achieved, if a large acceptorlike interface state distribution is positioned inside the $In_{0.53}Ga_{0.47}As$ conduction band.

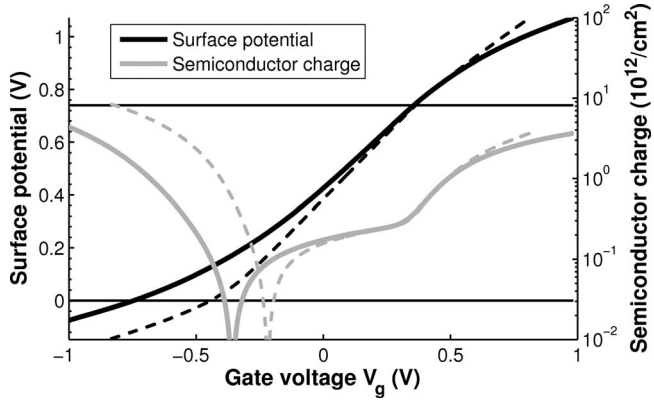

FIG. 4. Simulated surface potential (black line) and semiconductor charge (gray line) as a function of gate voltage for a p-type $In_{0.53}Ga_{0.47}As$ MOS structure with an oxide capacitance of 4.5 $\mu F/cm^2$. Simulated curves for an ideal III-V oxide interface, without any interface states are shown as well (dashed lines).

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