Bias-Dependent Admittance Spectroscopy of Thin-Film Solar Cells: Experiment and Simulation

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Bias dependent admittance spectroscopy of thin film solar cells: experiment and simulation.

Guy Brammertz, Thierry Kohl, Jessica de Wild, Dilara Gokcen Buldu, Gizem Birant, Marc Meuris, Jozef Poortmans, Bart Vermang

***Abstract*— In the present contribution we have measured and simulated room-temperature bias- and frequency-dependent capacitances of thin film solar cell devices. The results of both the simulations and experimental measurements were represented as two-dimensional contour plots showing the derivative of the capacitance with respect to the frequency multiplied by the frequency. These plots were called "loss maps", because responses in these contour plots correspond to responses of different non-idealities in the devices. Using a one-dimensional drift-diffusion solver (SCAPS), we have simulated the responses of different non-idealities of the solar cell devices, such as series resistance, bulk defects, interface defects, back contact barrier and absorber-buffer barrier. We have shown that some non-idealities have a quite recognizable trace in the loss map. Other non-idealities on the other hand show responses which look quite similar in the bias voltage and frequency space, making exact conclusions on the nature and position of the defect responses in thin film solar cells most of the times difficult. We have compared the simulated results to experimental measurements of one of our Cu(In,Ga)Se_2 solar cell devices and came to the conclusion that there is likely a bulk defect or a spike-like barrier at the CIGS-CdS interface present in our particular device. The loss map can in some cases be useful in order to analyze admittance spectroscopy data in a graphical and relatively intuitive way.**

***Index Terms* — admittance spectroscopy, thin film photovoltaics, CIGS, loss map.**

I. Introduction

Admittance spectroscopy is a relatively well understood and widely used technique to characterize metal-oxide-semiconductor (MOS) and pn-junction devices of all kinds [1-3]. It generally consists of the measurement of the differential capacitance of the device as a function of measurement frequency and temperature. The method has been used extensively on Cu(In,Ga)Se_2 [2, 4-13], $Cu_2ZnSnSe_4$ [14-20] and CdTe [21-22] thin film solar cells. Typical LCR-meters have the highest measurement accuracy for the capacitance when the current through the measured device is low [23]. Therefore, for pn-junction solar cells, the measurement is most of the time performed under short circuit conditions in the dark, which is the operation point where the current through the diode structure is the lowest. In general, the temperature dependency of the signal is measured, allowing for the extraction of the activation energy of the signal [2-22]. It is nevertheless also possible to measure the admittance of the structure under dark conditions at other bias points besides the short circuit condition, where the currents may not be minimal, but still low enough to allow for an accurate measurement of the differential capacitance. Additional information can be extracted from the bias dependency of the admittance signal [6,8,10,11]. In the present contribution we present a method for representing the bias and frequency dependent data in a graphical way and we will investigate to which extent this data can help in understanding the, sometimes complex, admittance response of thin film solar cells. We first present a room-temperature experimental measurement of a Cu(In,Ga)Se_2 (CIGS) solar cell, followed by a series of simulations in order to try to be able to identify the different defect responses that can be generated in typical thin film solar cell pn-junctions.

II. Experimental methods

The admittance data in this paper was acquired with an Agilent E4980A Precision LCR Meter, capable of measuring in the 20 Hz to 2 MHz frequency range. The tool is equipped with a built-in 40 V DC bias option, allowing for measurement of the LCR response of the device under different bias conditions. The LCR meter applies a DC bias on the device. In our measurements we have varied the bias voltage from -1.5V to +1V with 50 mV steps. On top of this DC bias voltage a small AC voltage is applied with a certain frequency f, in order to measure the differential capacitance and conductance of the sample. In our measurements we have fixed the AC voltage to 50 mV and the measurement frequency f was varied logarithmically from 100 Hz to 1 MHz with 50 different frequency steps. The tool was set to measure the values of an equivalent circuit consisting of a capacitance C_p and a conductance G_p in parallel, a setting that is very commonly used for this type of application. As a measurement result, we therefore obtain a matrix of values of the capacitance and conductance of the device as a function of DC bias voltage and frequency.

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The device that was measured for this work was a co-evaporated CIGS solar cell which presented a modest conversion efficiency of about 8 %. As a substrate soda lime glass with a 500 nm thick Mo back contact layer was used. The 700 nm thick absorber was co-evaporated with Cu/(In+Ga) = 0.9 and Ga/(In+Ga) = 0.3. On top of the absorber a 50 nm CdS buffer layer was deposited by chemical bath deposition, followed by a 120 nm thick intrinsic ZnO (i-ZnO) layer and a 250 nm Al-doped ZnO (AZO) layer deposited by sputtering. Finally, a 50/1000/50 nm Ni/Al/Ni top grid was deposited through a shadow mask and the 0.5 by 1 cm^2 device isolation was made with mechanical scribing.

The admittance simulations presented here were performed using the SCAPS software [24], which is a free one-dimensional drift-diffusion simulator. The structure that was simulated was a CIGS/CdS/i-ZnO/AZO heterojunction structure. The material parameters of all the layers were taken from Frisk et al. (Table 1) [25], only the layer thicknesses were adapted, since their device layout is similar to ours. The simulations in SCAPS were performed without external illumination. The capacitance and conductance of the heterojunction structure were calculated at the same operation points as for our experimental data, with 50 different frequencies varying logarithmically from 100 Hz to 1 MHz and with a bias voltage ranging from -1.5 V to +1 V with a voltage step of 50 mV.

III. Experimental Results

Figure 1a shows the room temperature capacitance versus frequency plot of the measured CIGS solar cell at zero bias voltage. This data as a function of device temperature is very often reported in publications and steps in the capacitance data in this figure generally relate to defect responses, series resistances in the device or carrier freeze-out [2-10]. Lately, the mere presence of the buffer layer has been shown to create a response in these curves [9]. All these effects lead to a variation of the capacitive response of the device as a function of applied AC voltage frequency.

In the case of the defects inside the band gap of the semiconductor, this frequency dependency arises from the time scale of charge carrier emission τ_e from the defect state [26]:

$$\tau_e = \frac{1}{2\pi f_e} = \frac{1}{\sigma v_t N_C} exp\left(\frac{\Delta E}{kT}\right), \quad (1)$$

where σ is the capture cross section, v_t is the thermal velocity of the carrier, N_C is the effective density of states in the corresponding energy band, k is the Boltzmann constant, T is the temperature and ΔE is the energy depth of the defect state with respect to the corresponding band edge energy (conduction band for electron traps and valence band for hole traps).

If the Fermi level crosses the defect state energy somewhere in the device, such as in the example of figure 4 at a distance of about 0.5 μm, the carrier will be able to follow the AC signal frequency only if the characteristic emission frequency f_e is higher than the AC signal frequency f. In this case the fixed charge of the defect state at a position of 0.5 eV is now adding to the differential capacitance of the circuit. On the other hand, if the characteristic emission frequency is lower than the frequency of the AC signal, the carrier will not be able to follow the AC signal and the charge of the defect will not add to the differential capacitance of the circuit. This effect therefore leads to a capacitance step at the frequency corresponding to the characteristic emission frequency f_e of the defect state.

If there is a resistance in series with our capacitive device, an RC circuit is created which has as a cut-off frequency $f_c = 1/2\pi RC$, also leading to a step in the capacitance plot at the cut-off frequency f_c. Making the distinction between the different responses (defect response, series resistance, carrier freeze-out, buffer layer) from the capacitance plots is not easy but can be achieved in some cases when taking the variation with temperature into consideration, although controversies still exist in the research community [4,6,8,9].

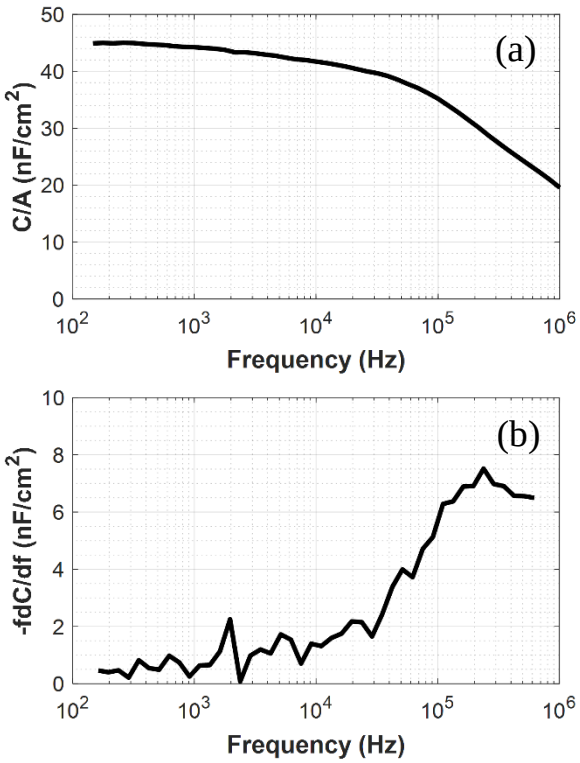

Fig. 1. Capacitance of the measured device at zero bias voltage as a function of frequency (a). -fdC/df of the same device at zero bias voltage as a function of frequency (b).

Figure 1b shows the same measurement, this time in a slightly different format, where now the derivative of the capacitance versus frequency, multiplied by the measurement frequency, is shown. Due to the derivative nature of the data, the figure is noisier, but generally peaks can be observed at the position of the capacitance steps, like the one observed at a frequency of about 250 kHz in our device. Similarly, the peaks in this graph

generally relate to defect responses, series resistances in the device, carrier freeze-out or buffer layers. In addition, with the help of an analytical model, the density of bulk defects can be calculated from the height of the peak in this graph [2].

These figures are very useful, and analysis of the behavior of these responses as a function of temperature can lead to very interesting results and insight into the different parasitic effects present in the devices, as has been shown numerous times already on different solar cell technologies [2-22].

There is nevertheless another dimension of the data, corresponding to the different bias voltages. If the DC bias voltage is changed, the width of the depletion region is changed. Also, the Fermi level position in the device is altered and consequently different defects in the device can be probed at different positions. It is, for example, possible that a defect exists in the device structure, but that at zero bias voltage the Fermi level is not crossing the energy level of the defect at any position inside the device. Therefore, the defect will not be charged and de-charged by the AC bias voltage, and thus, will not lead to a capacitance step in the measurement curve. By changing the DC bias, one could then force a situation in which the Fermi level is, this time, crossing the energy level of the defect, leading to a capacitance step. Observing the capacitance as a function of bias voltage, in addition to frequency, can therefore be an important factor, if one wants to maximize the chances of finding the different defects in the devices. In the following, we will therefore mainly analyze the shape of the -fdC/df curves as a function of frequency but also as a function of DC bias voltage. A relatively intuitive way to analyze this data as a function of two variables (bias voltage and frequency) is the use of two-dimensional contour plots. Figure 2 shows the corresponding data for our device.

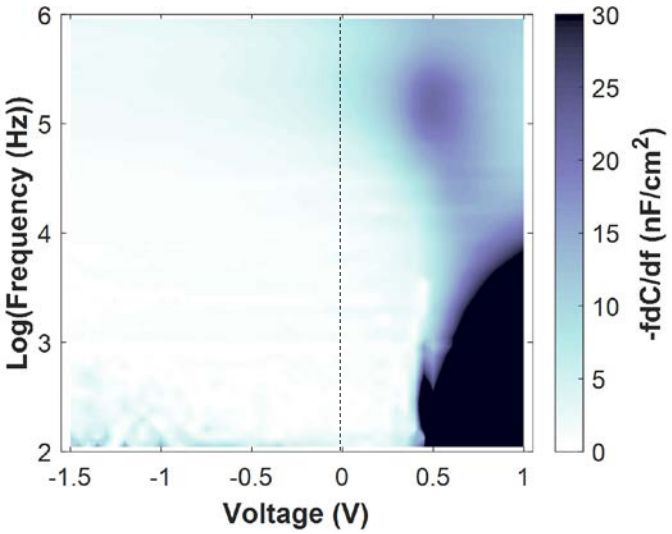

Fig. 2. *Loss map*: -fdC/df contour plot of the CIGS solar cell device as a function of DC bias voltage and the logarithm with base 10 of the frequency. The large black signal in the bottom right hand side corner and the noisy signal in the bottom left-hand side corner are due to DC currents passing through the device. The feature in the top right-hand side corner, also extending into the negative bias region but with lower intensity, is a parasitic response due to a non-ideality in the device. The dashed horizontal line highlights the zero bias voltage data, which is most often analyzed when the bias dependency is not taken into account.

On the horizontal axis the bias voltage is shown, whereas on the vertical axis the base 10 logarithm of the measurement frequency is shown. The data on the z-axis, which is shown as a contour plot, is the value of -fdC/df in nF/cm^2. The data which is shown in figure 1b can be found back in figure 2 as a vertical line at the zero bias voltage position. As in figure 1b, a peak can be identified at a frequency of about 250 kHz ($10^{5.4}$ Hz). The data in figure 1b is therefore only a small subsection of figure 2, which also contains the data for all the other bias voltages from -1.5 V in reverse bias all the way up to 1 V in forward bias.

In the following we will call the type of contour plot shown in figure 2 a "*loss map*", as the peaks in the contour plot will generally correspond to different loss mechanisms in the solar cell devices, such as electronic defect states, series resistances, carrier freeze-out and/or band edge misalignments, which reduce the conversion efficiency of the solar cells. In the ideal case, the map would be totally white, corresponding to no defect states or parasitic resistances in the measurement range. In the present case we have a peak in the loss map centered at a frequency of about 250 kHz and a bias voltage of about 0.5 V and it presents a large tail towards reverse bias. At -1.5 V a signal can still be detected. In the lower right-hand side of the figure we can see a region with an extremely large response, which is a region where the LCR meter cannot reliably measure the capacitance of the device, because the current flow through the device is too large. The solar cell structure is a diode and beyond the threshold voltage, which is in our case around 0.5 V, the currents flowing through the device are very large. Because of the large DC current component, the LCR meter has trouble accurately measuring the differential capacitance of the structure, especially at low frequency. A good metric that will allow us to estimate the regions in the loss map which could be affected by the large DC current is the unitless dissipation factor D, defined as [23]:

$$D = \frac{G_p}{2\pi f C_p} , \qquad (2)$$

where G_p and C_p are the measured values of the parallel conductance and capacitance respectively, and f is the measurement frequency. Figure 3 shows the dissipation factor for our CIGS solar cell device.

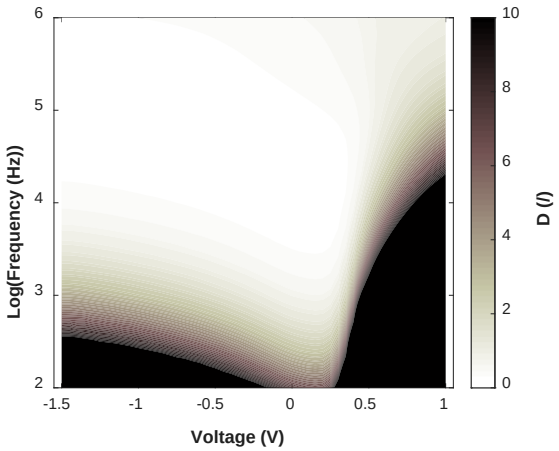

Fig. 3. Contour plot of the unitless dissipation factor D of our CIGS solar cell device as a function of DC bias voltage and the logarithm with base 10 of the frequency.

The black regions in figure 3 correspond to regions where the DC currents of the device are very large, compared to the capacitance, such that the device becomes mainly conductive, and an accurate measurement of the device capacitance cannot be guaranteed anymore. These regions should therefore be excluded from our analysis. What also becomes very visible in figure 3 is that the region around zero volt presents the widest frequency range with accurate measurements, because the currents through the device are particularly low in that bias region. In forward bias the accuracy is rather poor and especially beyond the threshold voltage and at frequencies below 10 kHz the measurement results are not reliable. On the other hand, in reverse bias at frequencies below 1 kHz some of the measurements become very noisy because the reverse leakage current is getting quite large compared to the sample capacitance.

In summary, we have defined a two dimensional “loss map” of our solar cell structure, showing -fdC/df as a function of bias voltage and the logarithm of the frequency. In some areas of the loss map the dissipation factor is very large, making capacitance extraction unreliable and these areas should be disregarded from our analysis. In the areas where the dissipation factor is lower than 10 [21,23], peaks in the map correspond to different parasitic loss mechanisms, such as defects, series resistances, carrier freeze-out or buffer layers. A priori we cannot make the distinction between the different parasitic effects just by analyzing the loss map, but in the next paragraph we will make device simulations where we will analyze the effect of different non-idealities on the shape of the loss map, in order to know if we can try to draw some basic conclusions on the nature of the non-idealities just from the basic shape of the loss map.

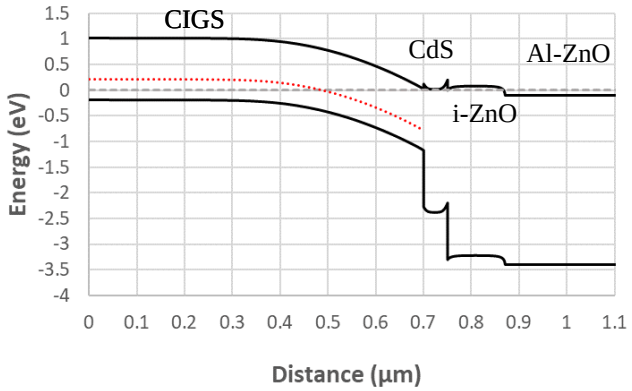

Fig. 4. Calculated band diagram of our solar cell structure at zero bias voltage. The Fermi level is indicated by a grey dashed line. As an example, the red dotted line shows the energy level of a bulk defect in the CIGS, positioned 0.4 eV above the top of the valence band edge energy.

IV. SIMULATION RESULTS

Figure 4 shows the band diagram at zero volt of our heterojunction device as calculated by the SCAPS software. For this calculation, no defects or parasitic resistances were added to the structure, such that this calculation represents the ideal case. The energy level of an eventual bulk defect in the CIGS absorber was added as a red dotted line, just as an example. It was not included for the calculation of this band diagram.

Thanks to the relatively good agreement between the work functions of CIGS, CdS and ZnO, there are no large discontinuities in the conduction band edge energy, allowing for efficient carrier extraction from the absorber.

We can now simulate the capacitance of the structure as a function of bias voltage and frequency. Plotting the simulated data in the same format as the loss map, i.e. -fdC/df as a function of bias voltage and the logarithm of the frequency, yields figure 5.

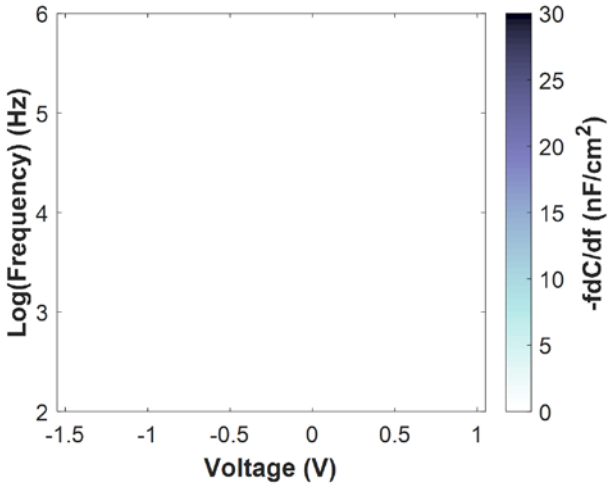

Fig. 5. Simulated loss map of the ideal heterojunction device: -fdC/df contour plot of the CIGS solar cell device without added defects as a function of DC bias voltage and the logarithm with base 10 of the frequency.

Clearly, there is no response that can be identified in the simulated loss map, which is of course due to the fact that we have not added any non-idealities in the structure. In the following we will now, one by one, add different non-idealities in our solar cell structure and simulate the effect that the non-ideality has on the loss map.

A. Series resistance

The first non-ideality that is frequently seen in solar cell devices is a non-zero series resistance. A typical value for the series resistance in a solar cell device is of the order of 1 Ω cm^2. We have varied the value of the series resistance from 1 to 1000 Ω cm^2 and calculated the effect of the variation on the loss map. Figure 6 shows the loss map for series resistance values of 1, 10, 100 and 1000 Ω cm^2.

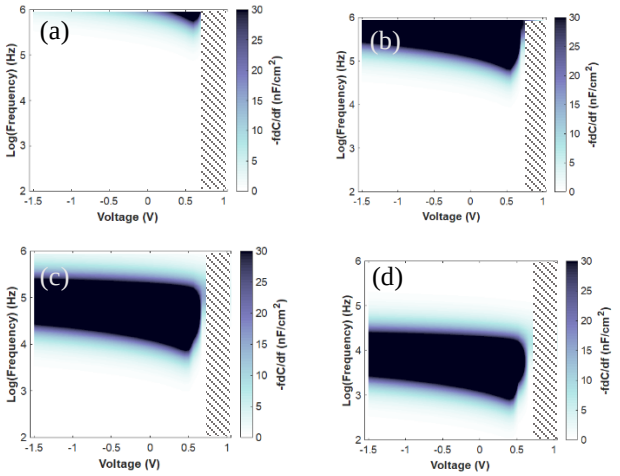

Fig. 6. Simulated loss map of the solar cell device with a series resistance of 1 Ω cm^2 (a), 10 Ω cm^2 (b), 100 Ω cm^2 (c) and 1000 Ω cm^2 (d). They grey hashed-out area highlights the forward bias region where the junction capacitance collapses, and the simulation results are not reliable.

The response due to the series resistance is very weakly dependent on the bias voltage and the maximum of the response moves down in the frequency range according to the cutoff frequency formula: $f_c = 1/2\pi RC$. A factor 10 increase in series resistance leads to a factor 10 reduction in the frequency at which the maximum of the signal occurs. According to the cutoff frequency formula the frequency of the response will also depend on the capacitance of the device and therefore on the absorber doping. For typical values of series resistance and doping encountered in high quality solar cell devices, the largest part of the series resistance response lies outside of the accessible measurement window, which typically goes only up to 1 MHz. For series resistances larger than 1 Ω cm^2 the high frequency region becomes completely dominated by the series resistance response. Beyond the threshold voltage at around 0.6 V, the signal goes to zero because the space charge region goes to zero, the junction capacitance collapses, and the device becomes purely conductive. In this region the simulation is not reliable, and we have highlighted this area in all the simulation plots using a grey hashed-out area.

B. Shunt resistance

The shunt resistance has no influence on the loss map, except that it increases the dissipation factor considerably and thereby makes the measurement of the capacitance less reliable in a larger voltage and frequency range. For every measurement the value of the dissipation factor should be observed, in order to know the area in the loss map where results can be safely analyzed.

C. Bulk defect in the CIGS absorber

Bulk defects are frequently seen in rather large densities in polycrystalline thin film solar cell devices. For the simulations here we have subsequently added 10^{16} cm^{-3} bulk defects at different energy positions in the CIGS band gap. In the lower half of the band gap, we have added acceptor-like defects, whereas in the upper half of the band gap we have added donor-like defects. In the band gap the defects were added at different energy levels above the valence band edge energy (acceptor-like defects) or below the conduction band edge energy (donor-like defects) of the CIGS. Depending on the energy position and the energy difference to the band edges the typical response frequencies of the defects can vary over orders of magnitude according to equation (1). Figure 6 shows the results of the calculation for 4 different positions of the acceptor-like defects in the lower half of the CIGS band gap, from 0.3 eV to 0.6 eV above the top of the valence band edge energy of the CIGS. If the defects are shallower than ~0.3 eV, no signal can be seen in the loss map at room temperature, as the response frequency is then faster than 1 MHz and cannot be observed according to equation (1). This exact response frequency also depends on the value of the capture cross section σ, which was chosen for the present simulation to be equal to 10^{-15} cm^2. These defects shallower than 0.3 eV are typically analyzed with low temperature admittance spectroscopy measurements [2-13].

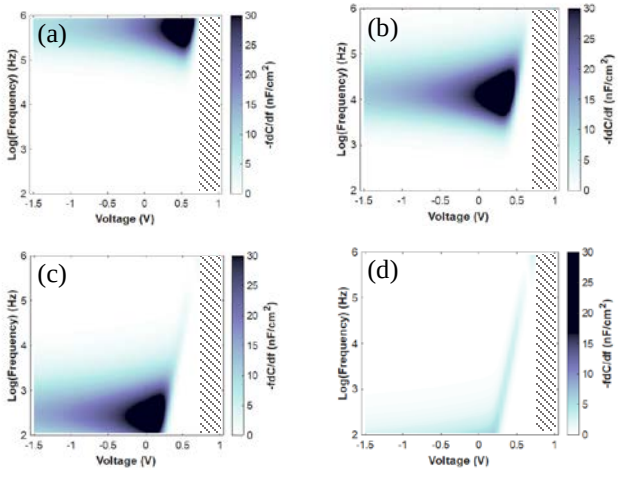

Fig. 7. Simulated loss map of the solar cell device with an acceptor-like bulk defect of 10^{16} cm^{-3} density at an energy position of 0.3 eV (a), 0.4 eV (b), 0.5 eV (c) and 0.6 eV (d) above the valence band edge energy of the CIGS.

Figure 7 shows that the bulk defect response moves to lower frequencies as the defect moves up in the lower half of the band

gap, according to equation (1). Here, ΔE is calculated with respect to the top of the valence band edge energy. The response itself shows a clear bias dependency due to the variation of the junction capacitance with bias voltage and the response is largest where the capacitance is largest. Nevertheless, except beyond the threshold voltage, the response is present over the full bias range. Even in very strong reverse bias a response can still be observed, as the Fermi level is still crossing the defect, thereby charging and discharging the defect level. As the defect is moved towards the mid-gap, it gets slower than 100 Hz and moves out of the measurement window of room temperature admittance measurements, at least for defects with a capture cross section of 10^{-15} cm^2 as assumed in our simulations. Mid-gap defects with a larger capture cross section will have faster response times and might still be visible in room temperature admittance measurements.

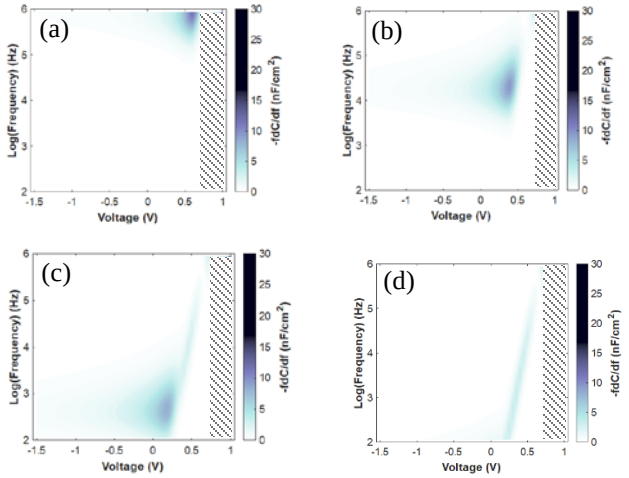

Fig. 8. Simulated loss map of the solar cell device with a donor-type bulk defect of 10^{16} cm^{-3} density at an energy position of 0.3 eV (a), 0.4 eV (b), 0.5 eV (c) and 0.6 eV (d) below the conduction band edge energy of the CIGS.

In the upper half of the band gap the defects are typically donor-like. Figure 8 shows the simulated loss map of the CIGS device with 10^{16} cm^{-3} donor like bulk defects added to the CIGS layer. Four different energy levels were simulated, 0.3 eV, 0.4 eV, 0.5 eV and 0.6 eV below the conduction band edge energy. In the upper half of the band gap the defects primarily exchange charges with the conduction band. As the CIGS absorber material is p-type, the number of electrons in the conduction band is low and the signal is now much reduced in intensity. Apart from that reduction in intensity, there are not many changes as compared to the case of the acceptor-like defects in the lower half of the band gap, as long as the electrostatics of the device remain the same. In other words: the fixed charge due to the defects needs to be much smaller as compared to the charge from the doping in the material. In that case the loss map of donor-type and acceptor-type defects show a similar behavior with respect their frequency and bias voltage dependency. The shape of the response in the loss map remains the same, with a signal moving down in the frequency domain, as it is positioned deeper inside the band gap. Also, the bias dependency is similar, with a weak bias dependency and a signal present even in strong reverse bias.

D. Interface defect at the CIGS/CdS interface

A second type of defect that is often encountered in thin film solar cell devices are interface defects at the absorber-buffer interface. We have simulated acceptor- and donor-like defects with a density of 10^{12} $eV^{-1}cm^{-2}$ and a capture cross section of 10^{-15} cm^2 at the CdS-CIGS interface. We have positioned the defects at different energy levels above the valence band edge energy (acceptor-like defects) or below the conduction band edge energy (donor-like defects) of the CIGS. Figure 9 shows the simulation results for acceptor-like defects with an energy position varying from 0.3 to 0.6 eV above the top of the valence band edge energy of the CIGS. At energies below 0.3 eV the simulation shows no response in the loss map, because the defect has a response frequency faster than 1 MHz. Such shallow defects can only be measured with low temperature measurements.

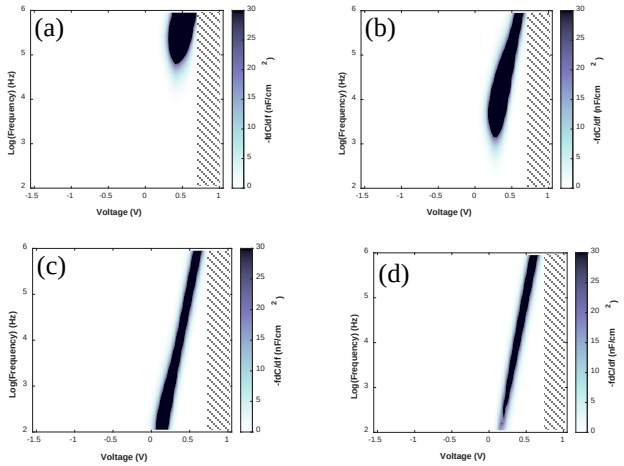

Fig. 9. Simulated loss map of the solar cell device with an acceptor-type interface defect at the CIGS-CdS interface with a density of 10^{12} cm^{-2} eV^{-1} and at an energy position of 0.3 eV (a), 0.4 eV (b), 0.5 eV (c) and 0.6 eV (d) above the top of the valence band edge energy of the CIGS.

In the case of interface defects the response in the loss map looks much more localized in the bias voltage space. As the bias voltage is swept the Fermi level moves over the defect level and leaves a response only in a small region of bias voltage. This is a quite typical response for a relatively low defect density at the interface.

If the defect density at the interface now increases above a certain threshold level, Fermi level pinning appears. As the Fermi level is moving through the defect, it leads to more and more fixed charges at that energy position, fixing the Fermi level at the interface at that position, leading to a broad response over the whole bias voltage range. Figure 10 shows the simulation results for a larger density of acceptor-like interface defects, 5 10^{12} $eV^{-1}cm^{-2}$, leading to Fermi level pinning, visible through the broad bias-independent response in the loss map.

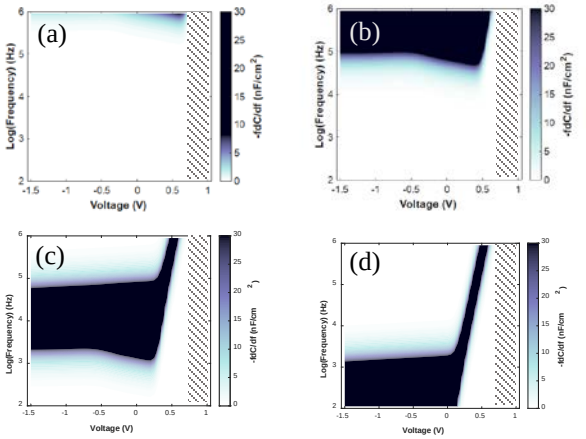

Fig. 10. Simulated loss map of the solar cell device with an acceptor-type interface defect at the CIGS-CdS interface with a density of 5 10^{12} cm^{-2} eV^{-1} and at an energy position of 0.3 eV (a), 0.4 eV (b), 0.5 eV (c) and 0.6 eV (d) above the top of the valence band edge energy of the CIGS.

For the case of donor-like interface defects at the CIGS-CdS interface no response can be seen, because at the CIGS-CdS interface the electron quasi-Fermi level remains stuck at the top of the band gap of the CIGS, due to the high n-type doping in the CdS. For all our simulations an n-type doping of 5 10^{17} cm^{-3} was assumed in the CdS buffer layer, a value large enough to effectively pin the electron quasi-Fermi level at that energy position at the CIGS-CdS interface. The donor-like interface defects are therefore at all moments filled and electrically neutral, not leading to any response in the admittance measurements. This situation changes as the doping in the CdS layer is subsequently lowered and the electron quasi-Fermi level becomes more free to move in energy at the CIGS-CdS interface. In that case a response becomes visible. Figure 11 shows the simulated loss map of the device with a 10^{12} eV^{-1} cm^{-2} donor-like interface defect response and a CdS doping of 10^{17} cm^{-3}. Four different energy positions of the defect in the upper half of the CIGS band gap were simulated.

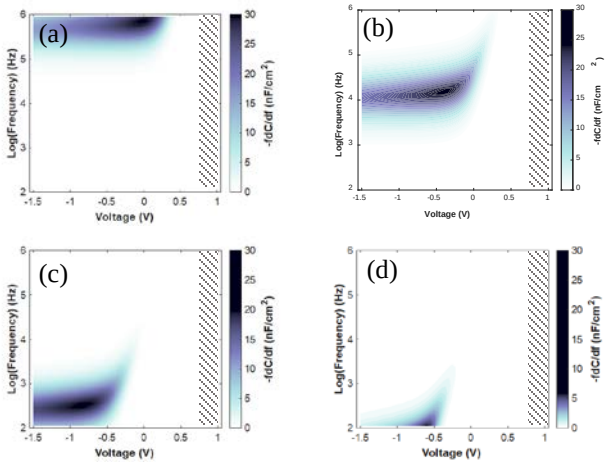

Fig. 11. Simulated loss map of the solar cell device with low CdS doping of about 10^{17} cm^{-3} and with a donor-type interface defect at the CIGS-CdS interface with a density of 10^{12} cm^{-2} eV^{-1} and at an energy position of 0.3 eV (a), 0.4 eV (b), 0.5 eV (c) and 0.6 eV (d) below the bottom of the conduction band edge energy of the CIGS.

Here the response becomes visible, as the Fermi level can travel to the energy position of the defect at the interface, leading to the response in the loss map. As the defect is positioned deeper inside the band gap, the response signal moves to lower frequency, as expected. At the energy position of the defect, the Fermi level gets pinned, leading to the bias voltage independent response in reverse bias.

E. Backside contact barrier

A likely non-ideality at the backside of the CIGS is a back-contact resistance. In this study we have simulated a back-contact barrier with a height varying from 0.2 eV to 0.5 eV by varying the work function of the back contact with respect to the valence band of the CIGS. Figure 12 shows the results of this calculation.

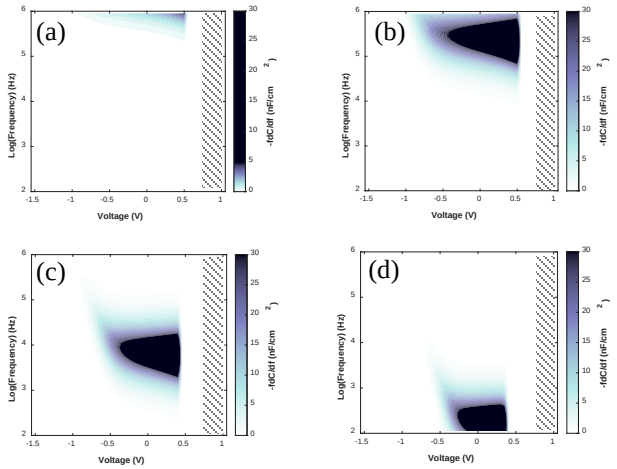

Fig. 12. Simulated loss map of the solar cell device with a contact barrier at the backside of the CIGS of 0.2 eV (a), 0.3 eV (b), 0.4 eV (c) and 0.5 eV (d).

Again, a strong response in the loss map becomes visible and moves to lower frequencies with increasing barrier height. A slight difference with respect to the other defect calculations is the rising tail in strong depletion, at bias voltages smaller than -0.5 V.

F. Barrier at the CIGS/CdS interface

The conduction band at the CIGS – CdS interface is generally also presenting a discontinuity, because the electron affinities of the two materials are not necessarily the same. Here we have simulated the effect of a spike-like barrier at the CIGS-CdS interface, by reducing the electron affinity of the CdS and ZnO layer, leaving the electron affinity of the CIGS unchanged at 4.3 eV. Figure 13 shows the results of the calculations with a spike like-barrier varying from 0.4 to 0.7 eV.

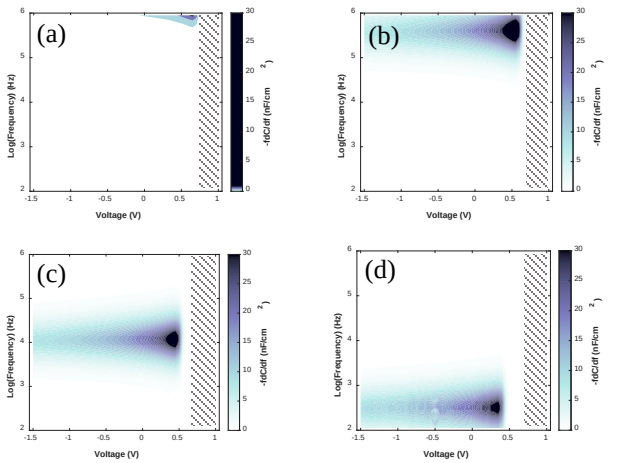

Fig. 13. Simulated loss map of the solar cell device with a spike-like barrier for electron flow at the CIGS – CdS interface of 0.4 eV (a), 0.5 eV (b), 0.6 eV (c) and 0.7 eV (d).

The response here is completely horizontal and has a slight bias dependency which is the same bias dependency as the junction capacitance. Again, as usual, it moves to lower frequency as the barrier height is increased.

G. Different defects simultaneously

In general, not only one type of defect is present in a given device. Adding different non-idealities in the samples will lead to a more complex loss map, where the different defect responses will be present all at the same time, making the picture much more complex. As an example, figure 13 shows a simulated loss map where three different non-idealities were added simultaneously: a series resistance of 1 Ω cm^2, an acceptor-like bulk defect with a density of 10^{16} cm^{-3} positioned 0.4 eV above the valence band edge energy of the CIGS and an acceptor-like interface defect at the CIGS-CdS interface with a density of 10^{12} eV^{-1}cm^{-2}, positioned at an energy of 0.3 eV above the CIGS valence band edge energy.

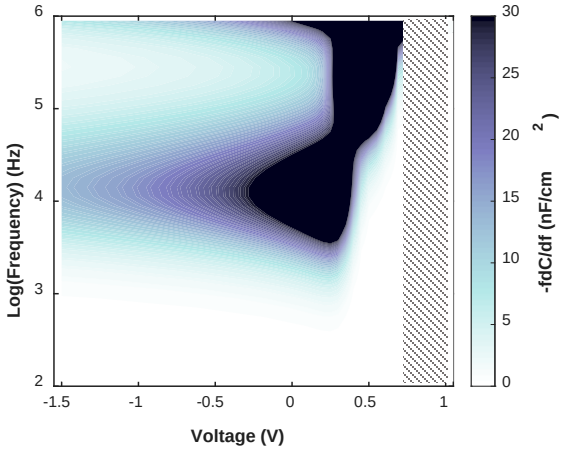

Fig. 14. Simulated loss map of the solar cell device with three simultaneous defects: series resistance, bulk and interface defects.

As becomes visible in figure 14, the loss map is the sum of the three individual loss maps, figures 6(a), 7(b) and 9(a). Therefore, to first order, as long as the Fermi level remains free to move in the device, the responses of the different defects add up in the loss map. If one of the defects leads to Fermi level pinning, the additionality of the defect responses is not guaranteed anymore. Figure 14 shows an example of such a situation, where a simulation was made for a device with three different non-idealities: a series resistance of 1 Ω cm^2, an acceptor-like bulk defect with a density of 10^{16} cm^{-3} positioned 0.4 eV above the valence band edge energy of the CIGS and an acceptor-like interface defect at the CIGS-CdS interface with a higher density of 5 10^{12} eV^{-1} cm^{-2}, positioned at an energy of 0.3 eV above the CIGS valence band edge energy.

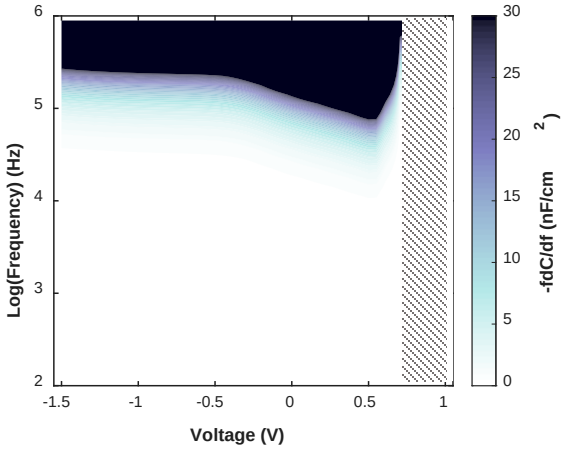

Fig. 15. Simulated loss map of the solar cell device with three simultaneous defects: series resistance, bulk and a high density of interface defects leading to Fermi level pinning.

Figure 15 is now only a sum of figures 6(a) and 10(b), the response from figure 7(b) not appearing anymore, as the Fermi level is pinned at the interface defect energy position, not able to move to the bulk defect energy position anymore. Therefore, despite of being present in the structure, the bulk defect is not visible in the loss map anymore.

V. Discussion

First, the simulations of section IV show why the derivation of exact conclusions on the nature and position of the defect is difficult for room-temperature admittance measurements of thin film solar cell devices. Although some of the non-idealities show a quite recognizable trace in the loss map, such as the backside contact barrier with its rising edge in reverse bias (Fig. 12) or an interface defect not leading to Fermi level pinning with its very localized response in bias voltage space (Fig. 9), most of the non-idealities show responses in the loss map which are quite similar, as for example the case of the series resistance (Fig. 6) and the interface defect with Fermi level pinning (Fig. 10). Also, not all possible defects, defect levels, intensities and defect combinations were simulated here, as the amount of possible combinations is very large. Therefore, even if a response in the loss map looks like a simulated one, it can not be excluded that another configuration exists which would lead to a similar loss map.

Nevertheless, the simulations of section IV also show that in some cases the loss map can be a very useful tool for analyzing

the admittance data of thin film solar cells in a more graphical way, allowing in some cases at least to derive some basic directions on how to improve the devices.

For the case of our experimental measurements it seems that the response observed in the loss map looks like either a bulk defect response (Fig. 7 or 8) or a barrier response at the CIGS-CdS interface (Fig. 13). In the following we have simulated it with a bulk defect in the CIGS. Both donor-like defects in the top half of the band gap and acceptor-like defects it the bottom half of the band gap will lead to a response that resembles the one in Figure 2. Figure 16 shows the case of the simulated response of our device with an acceptor-like, 3 10^{15} cm^{-3} defect density added at an energy position of 0.33 eV above the valence band edge energy of the CIGS. A capture cross section of 10^{15} cm^{-2} was assumed. In order to derive the real value of the capture cross section, temperature-dependent measurements and an Arrhenius plot should be made, which would then also allow to derive the accurate energy position in the band gap. The loss maps can then of course also be generated at different temperatures, which would add another dimension to the data, but this goes beyond the scope of this paper.

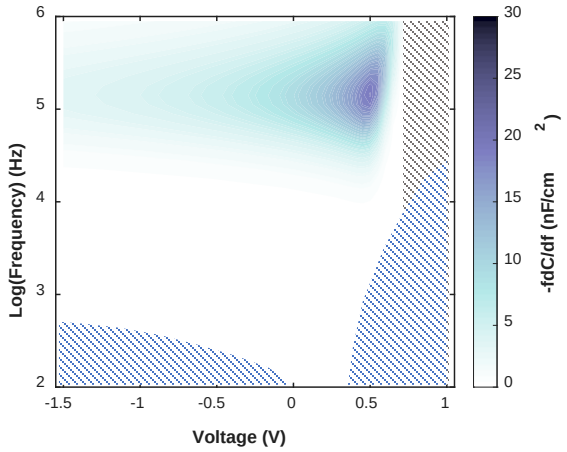

Fig. 16. Simulated loss map of the solar cell device with an acceptor-like bulk defect density of 3 10^{15} cm^{-3} positioned 0.33 eV above the valence band edge energy of the CIGS. This data can be compared to the experimental data in Figure 2. The hashed-out regions indicate regions where either the experimental data is not accurate due to a high dissipation factor (blue), or where the simulation is not accurate due to the collapse of the depletion capacitance (grey). These regions should be excluded from the analysis.

Figure 16 should be compared to the experimental measurement in figure 2. The experimental results can be quite closely reproduced, neglecting the large response in forward bias which is purely due to the large diode currents and dissipation factor in that bias region, leading to inaccurate capacitance measurements. This region should be neglected for the analysis.

VI. Conclusions

The simulations and experimental measurements show the possibilities and limitations of room-temperature admittance spectroscopy of thin film solar cell devices. The "loss maps" presented in this paper are an intuitive tool which allow to map the responses of different defects in the bias voltage and measurement frequency space. We have shown that although some defects show a recognizable response in the loss map, other defects have responses that look quite similar in the bias voltage-frequency space. This leads to difficulties for the extraction of exact conclusions on the position and nature of the defects in the solar cell structure from room-temperature measurements alone. By comparing the experimental results to the simulation results, we concluded for our experimental CIGS solar cell device, that the response observed is either due to a bulk defect in the CIGS absorber layer or due to a barrier at the CIGS-CdS interface. Therefore, the loss map can be a useful tool for analyzing admittance spectroscopy data of thin film solar cells, both for room-temperature and low-temperature measurements.

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Dr. Meuris authored and co-authored more than 450 scientific publications and as an inventor holds more than 45 patents

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Afterwards he joined the photovoltaics group, where he became responsible for the group Advanced Solar Cells. Within this frame he started up the activity about thin-film crystalline Si solar cells at IMEC and he has been coordinating several European Projects in this domain during the 4th and 5th European Framework Program. At the moment he is Scientific Director of the PV-activities at imec . As a Board Member of EUREC agency and member of the Steering Committee of the EU PV Technology Platform he became involved in the preparation of the Strategic Research Agenda for Photovoltaic Solar Energy Technology of the European PV Technology Platform. He also acted as General Chairman of the 21st European Photovoltaic Solar Energy Conference & Exhibition and of the SiliconPV 2012 Conference.
Dr. Poortmans has authored or co-authored more than 500 papers that have been published in Conference Proceedings and technical journals. Since 2008 he is also part-time Professor at the K.U.Leuven, where he teaches courses on photovoltaics and materials in electrical engineering. Since 2013 he is also imec Fellow.

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