A grey box model for shunting-type potential induced degradation in silicon photovoltaic cells under environmental stress

Arnaud Schils[1], Robbe Breugelmans[2,3], Jorne Carolus[2,3], Julián Ascencio-Vásquez[4], Andreas Wabbes[5], Emmanuelle Bertrand[5], Bader Aldalali[6], Michael Daenen[2,3], Eszter Voroshazi[1], Stijn Scheerlinck[5]
[1] imec (partner inEnergyVille), Thorpark 8320, B-3600 Genk, Belgium
[2] Institute for Materials Research (IMO), Hasselt University (partner in EnergyVille), 3590 Diepenbeek, Belgium
[3] IMOMEC, imec (partner in EnergyVille), 3590 Diepenbeek, Belgium
[4] 3E sa, Quai à la chaux 6, B-1000 Brussels, Belgium
[5] Engie Laborelec, Rodestraat 125, B-1630 Linkebeek, Belgium
[6] Kuwait University, College of Engineering and Petroleum, Khaldiya, Kuwait

Topic 4.1 PV Module Design, Manufacture, Performance and Reliability
PV module design, module manufacturing processes. Type approval testing, degradation, ageing and lifetime; new and improved measurement and characterisation methods, correlation between laboratory testing and field performance, energy yield, energy rating.

ABSTRACT: This paper proposes a grey box model for cell-level simulation of potential induced degradation of the shunting type (PID-s) by extending a physics-based energy yield simulation framework. The leakage current is first computed using a physics-based approach based on an equivalent frame-to-cell electric circuit composed of temperature and humidity dependent resistances. Then, the increase of PID-s degradation due to leakage current is retrieved from measurements of PID-s evolution performed on poly-cSi cells. Finally, IV-curves of cells affected by PID-s are approximated by modifying the IV-curve of a PID-free cell using measurements of short circuit current and open-circuit voltage decrease with PID-s. A first comparison of simulated versus measured final PID-s levels is reported for a PV string after nine years of operation. The advantage of our grey box model over an empirical model is the possibility to investigate changes in material properties without the need for new measurements and to provide quantitative energy yield loss estimates depending on climate and system design.

Keywords: potential induced degradation (PID), reliability, high voltage stress (HVS)

1 INTRODUCTION

Estimating accurately the power produced by photovoltaic (PV) systems is critical for many applications such as financial assessment of PV projects and design of energy management systems [1]. During the past decade, this need motivated the development of new physics-based models for PV systems energy yield simulation [2]. Despite their accuracy over the first year of PV system operation, results over lifetime are often too optimistic: a recent solar risk assessment report states that predicted P90 production is reported to occur more than 1-in-3 years instead of 1-in-10 [3]. One of the causes is the absence of accurate models for degradation mechanisms.

Among possible degradation types, potential induced degradation (PID), in particular of the shunting type (PID-s), is one of the most common and severe reliability issue of crystalline silicon PV cells in the field [4]. PID-shunt occurs due to migration of sodium cations (Na^+) from the module tempered glass ($Na_2O.3SiO_2$) into small defects of the cell silicon lattice, creating stacking faults.

When many PV modules are connected in series, a high potential difference builds up between cells and frames of PV modules, which are grounded for safety reasons. Sodium cations drift from the front glass to the silicon nitrate (SiN) layer under the effect of the electric field. If the potential drop across the SiN layer of the cell is higher than 10V, sodium cations goes through the SiN potential barrier and then diffuse into small defects of the cell silicon lattice.

The first and main impact of this degradation on cell electric properties is the decrease of the shunt resistance R_{SH} [4]. At a more severe degradation stage, open circuit voltage (V_{OC}), short-circuit current (I_{SC}), operating point voltage (V_{MPP}), current (I_{MPP}) and power (P_{MPP}) are all drastically reduced.

The current state of the art for PID simulation relies on empirical models [5,6] which have their advantages but also come with the following shortcomings. Firstly, the model requires experimental input of any new PV module to properly fit the parameters of the models. Therefore, these models do not allow to perform "what if" simulations. Secondly, to ease the test matrix the model assumes a quadratic and linear evolution of PID with time and voltage, respectively, while measurements report logistic dependencies [7]. Finally, these models do not

consider the cell-level differences in PID evolution due to different frame to cell distances.

This work is a first step to extend the imec's PV energy yield coupled optical, thermal and electrical simulation framework introduced in [2,8-10] with a cell-level model to predict the evolution of PID-s and its impact on cell current-voltage (IV) curve, power and temperature. The model takes as input climatic data (up to 1 min temporal resolution), thermoelectrical and optical module properties from datasheets and geometrical parameters.

The PID-s model is composed of three steps. Firstly, the computation of the Na^+ leakage current (I_{leak}) depending on environmental conditions. For now, only I_{leak} flowing through the front glass surface and then through the cell thickness, reported to be the most detrimental in outdoor conditions [11], is considered. Secondly, the computation of the PID-s level (power loss at STC) increase due to degradation by I_{leak}. Finally, the IV curve of the solar cell depending on its PID-s level is obtained.

2 LEAKAGE CURRENT

The current I_{leak} is computed by solving an equivalent electrical circuit modelling the path of Na^+ cations [12] (see Figure 1). The effect of environmental stress factors on PID-s evolution is modelled by varying, at each timestep and for each cell, the electrical resistances.

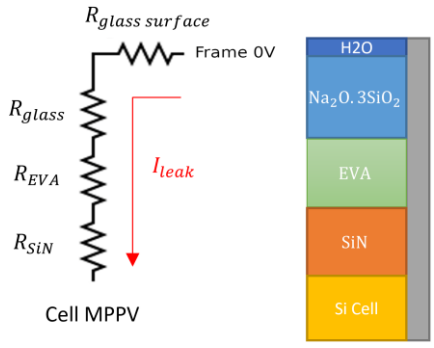

Figure 1: Simplified equivalent electric circuit for the Na^+ path from the grounded frame to a solar cell operating at V_{MPP} at the front side of a PV module [12]. From top to bottom, the four electrical resistances model the glass surface, the tempered glass, the encapsulant (EVA) and the silicon nitrate.

2.1 Frame to cell voltage drop

The frame being grounded, the frame to cell voltage drop can be inferred knowing operating voltages of all cells in the string electric circuit and the position of the zero-voltage point. The imec's PV energy yield framework computes the IV curves and V_{MPP} of the string and each solar cell using cell-level single diode model (see [2,8-10] for details). Module bypass diodes, installed in parallel of substrings, are also modelled by their IV curve in the string electric circuit (see Figure 2). Bypass diodes prevent decrease of the string I_{SC} when only a part of string is affected by PID.

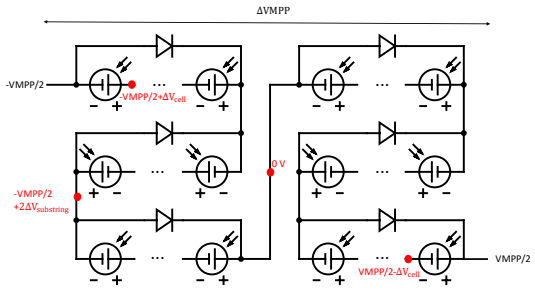

Figure 2: Electric circuit modelling a two modules string. Voltage differences with the frame are indicated in red.

The frame to cell voltage drops are retrieved going through the electric circuit from the negative towards the positive plug and incrementally adding up the voltage drops across each component of the circuit (see Figure 2).

2.2 Glass, EVA and SiN electrical resistances

The ionic electrical resistances of tempered glass and EVA as a function of layer thickness, temperature, water content and humidity are implemented using measurements reported by Takata et al. [13] and Mon et al. [14]. Accurate glass and EVA temperatures are computed by the imec's PV energy yield framework thermal model. The SiN layer being very thin, its ionic electrical resistance can be safely neglected [12]. The consideration of the impact of the SiN electronic conductivity on cell susceptibility to PID, reported by Naumann et al. [15], is a future work.

2.3 Glass surface electrical resistance

The glass surface electrical resistance models the propagation of Na^+ ions through a thin layer of humid air at top of the module front glass. The electrical resistivity of this layer is provided as a function of glass surface humidity by Naumann et al. [12]. The glass temperature T_{glass} is retrieved from the energy yield framework and is used to compute the glass surface humidity from relative ambient humidity [16, 17].

A different glass surface resistance is obtained for each cell by modelling the frame to cell glass surface as a conductor connecting the frame rectangular equipotential ($0V$) to a second rectangular equipotential (V_{stack}) inner to both the cell glass surface and the frame rectangles. This process is performed many times for each cell through a finite difference method.

This approach, even if being an extension of the model introduced by Naumann et al. [12], nevertheless remains an approximation whose accuracy on I_{leak} needs to be assessed [18]. An example of obtained I_{leak} spatial variation is presented in Figure 3. More formal modelling is possible using 3D FEM, at the cost of slower computation.

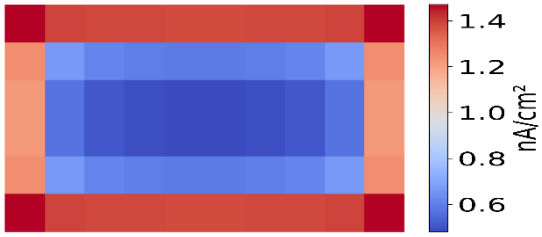

Figure 3: I_{leak} in a 60 cells module. Voltage drop between frame and cells set to 1000 V, temperatures of all layers set to 60°C, glass surface and EVA RH set to 60% and water content in tempered glass set to 0%.

3 LEAKAGE CURRENT IMPACT ON PID-SHUNT DEGRADATION

The PID-s level evolution with time for three different constant voltage V_{stack} (200 V, 600 V and 1000 V) applied with the foil method on multi-crystalline one-cell laminates has been measured by J. Carolus [19-21] at 60°C and 60% ambient temperature and relative humidity (RH), respectively. Since the foil method is used, the voltage V_{stack} is applied around the bulk glass, EVA and SiN resistances in Figure 1 (i.e. no glass surface resistance). Evolution of PID-s with I_{leak} is obtained by dividing the stack voltage by the stack resistance at the lab temperature and RH,

$$R_{stack} = R_{glass} + R_{EVA} + R_{SiN}, \quad (1)$$

$$I_{leak} = \frac{V_{stack}}{R_{stack}(60°C,\ 60\%\,RH)} \quad (2)$$

The measurements are well fitted by a two parameters logistic function [19],

$$PID_s(t_{lab}) = \frac{100\%}{1 + \exp\left(-k * (t_{lab} - t_0)\right)} \quad (3)$$

The parameters $k(I_{leak})$ and $t_0(I_{leak})$ are obtained by linear interpolation over the three I_{leak} points allowing to evaluate Equation (3) for any I_{leak} (see Figure 4). The derivative of Equation (3) w.r.t. t_{lab} multiplied by the timestep of the simulation Δt yields PID-s level increase during Δt due to any constant I_{leak} applied since a time t_{lab} on an initially PID-s free cell.

An approach like the one proposed by Annigoni et al. [6] is used to extend the model to time-varying I_{leak} in outdoor conditions: the effective time t_{lab} is obtained by computing the inverse of Equation (3), i.e. $t_{lab}(PID_s)$, with PID_s being the PID-s level of the cell at the end of the previous timestep.

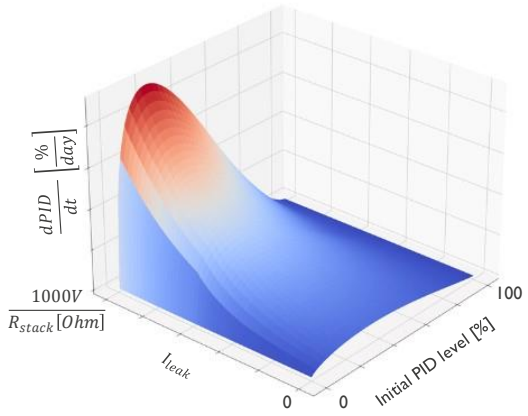

Figure 4: PID-s derivative at any leakage current I_{leak} and for any initial cell PID-s level.

4 IV-CURVES OF PID-SHUNTED CELLS

The estimation of PID-s level is the basis to reconstruct the full IV curve of a PID-s affected cell at specific irradiance and temperature. Because no analytical expression is available for the IV-curve of a PID-s affected cell, this is approximated applying a geometrical algorithm on the IV-curve of a PID-free cell. Operating powers of the full string and cells are then computed using these IV curves.

First, the I_{sc} and V_{oc} are scaled using evolution of these quantities with PID-s level measured by J. Carolus [19-21]. A geometrical algorithm then decreases the distance between each (V,I) point and the straight line passing by I_{sc} and V_{oc} by PID-s level % (see Figure 5): the higher the PID-s level, the closer to a straight line the IV curve will be.

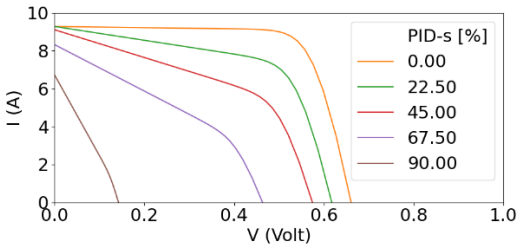

Figure 5: Solar cell IV-curves for different PID-s level.

Accuracy of this approach has been assessed comparing obtained P_{MPP} with expected P_{MPP} in view of the PID-s level (see Figure 6).

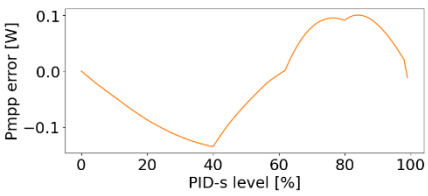

Figure 6: Absolute error on cell P_{MPP} comparing with expected P_{MPP} corresponding to cell PID-s level. The P_{MPP} at STC and 0% PID-s is 4.5W.

5 RESULTS AND VALIDATION

First validation is conducted on a 22 modules string located south of France, oriented south and tilted by 25°. The PV polycrystaline 60-cells modules in the system are rated for 235 Wp and have three bypass diodes distributed among three substrings. The front glass and EVA encapsulant thicknesses are considered to be 3.2 mm and 0.3 mm, respectively.

The time period between the 25/03/2011, i.e. the first day of operation of the string, and the 06/10/2019 was simulated using a 1h time resolution. Input in plane irradiance and ambient temperature were measured onsite, at the exception of 157 days of missing measured data filled with the ERA5 climatic dataset [22]. Wind speed, wind direction and ambient RH are retrieved from the same ERA5 dataset for the nine years time period.

The simulated maximum DC power among one year drops quickly from 5 to 3 kW during the first two years and then keeps slowly decreasing to reach ~1.5 kW at the end of the nine years (see Figure 7).

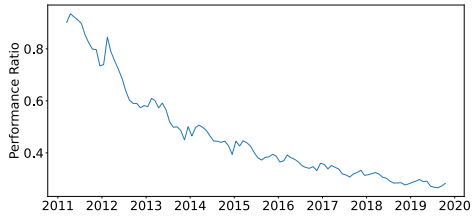

Figure 7: Simulated monthly PR for string DC power decreases from 0.935 to 0.284 due to PID-s.

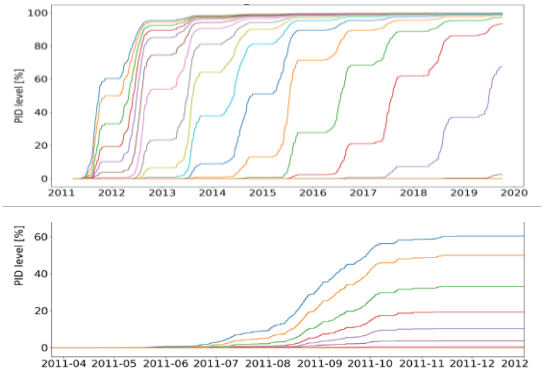

Figure 8: Evolution of per module average of the cells PID-s levels in order of distance from negative polarity of the inverter.

As expected, modules undergoing higher frame to cell voltage drops suffer from faster PID-s evolution (see Figure 8). Modules PID-s levels increase sharply during summer but remain constant during winter. This is explained by the high ambient RH (on average 69% RH during daylight over the nine years) in the region, which makes the glass surface resistance negligible compared to the EVA resistance. Therefore, PID-s evolution is mainly driven by the EVA temperature which increases highly during summer (see Figure 9). Due to higher temperatures, the EVA electrical resistance is up to 10 times lower in summer explaining the fast increase of PID-s during this period.

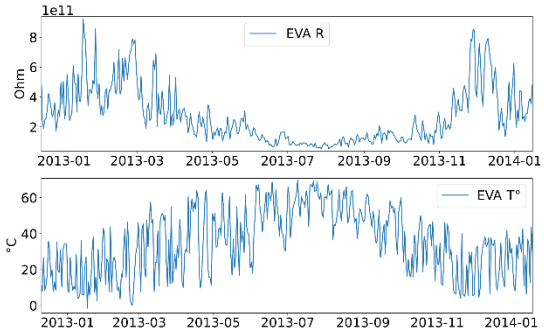

Figure 9: daily maximum of the EVA electrical resistance and temperature in year 2013.

At the end of the nine years simulation, five modules end up not being affected by PID-s, four have a PID-s level between 1% and 99% and 13 reached a 100% PID-s level. A comparison between measured and simulated final modules PID-s levels for six modules is presented in Table 1. From this comparison it appears that simulation overestimates the impact of PID-s degradation. A possible explanation is the lack of model for PID regeneration.

Position	Final PID-s levels	
	Measured	Simulated
Most +	0%	0%
2nd most +	2%	0%
4th most -	53%	100%
3rd most -	78%	100%
2nd most -	100%	100%
Most -	100%	100%

Table 1: Measured versus simulated final PID-s levels for the two and four modules closest to the positive and negative voltage inverter plugs, respectively.

6 CONCLUSION AND FUTURE WORK

An advantage of the presented grey-box approach over fully empirical models is the possibility to investigate the effect of changes in the module layers properties without experimental data to calibrate. First results of obtained PID-s levels for the studied string show interesting correlations between PID-s degradation and environmental stress factors. Future work will be to further validate the model, to implement a water ingress model, spontaneous PID-s recovery and assess the generality of the empirical part of the model for different Si cells (PID-s evolution with I_{leak}, V_{OC} and I_{SC} evolution with PID-s level).

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