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Mechanisms of Charge Carrier Transport in Polycrystalline Silicon Passivating Contacts

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Abstract. We use temperature-dependent contact resistivity (ρ_c) measurements to systematically assess the dominant electron transport mechanism in a large set of poly-Si passivating contacts, fabricated by varying (i) the annealing temperature (T_{ann}), (ii) the oxide thickness (t_{ox}), (iii) the oxidation method, and (iv) the surface morphology of the Si substrate. The results show that for silicon oxide thicknesses of 1.3-1.5 nm, the dominant transport mechanism changes from tunneling to drift-diffusion via pinholes in the SiO_x layer for increasing T_{ann}. This transition occurs for T_{ann} in the range of 850°C–950°C for a 1.5 nm thick thermal oxide, and 700°C–750°C for a 1.3 nm thick wet-chemical oxide, which suggests that pinholes appear in wet-chemical oxides after exposure to lower thermal budgets compared to thermal oxides. For SiO_x with t_{ox} = 2 nm, grown either thermally or by plasma-enhanced atomic layer deposition, carrier transport is pinhole-dominant for T_{ann} = 1050°C, whereas no electric current through the SiO_x layer could be detected for lower T_{ann}. Remarkably, the dominant transport mechanism is not affected by the substrate surface morphology, although lower values of ρ_c were measured on textured wafers compared to planar surfaces. Lifetime measurements suggest that the best carrier selectivity can be achieved by choosing T_{ann} right above the transition range, but not too high, in order to induce pinhole dominant transport while preserving a good passivation quality.

Keywords:

Poly-Si
Passivating contacts
Tunneling transport
Pinhole transport
Contact resistivity
Transfer length method

1. Introduction

Polycrystalline silicon (poly-Si) passivating contacts have recently attracted the interest of the photovoltaic community because they simultaneously enable low contact resistivity and good passivation quality [1,2], leading to high carrier-selectivity, thereby facilitating silicon solar cell efficiencies up to 26.1% [3]. However, the understanding of the underlying transport mechanism of this contact structure is still incomplete. In the literature, two different models have been proposed to describe the transport of charge carriers through the SiO_x layer in poly-Si passivating contacts (Fig. 1(a)): direct tunneling across the oxide barrier and drift-diffusion through local discontinuities (pinholes) in the oxide [1,4,5]. It has been demonstrated that tunneling transport prevails in the case

of ultrathin oxides (t_{ox} < 2 nm) whereby T_{ann} is sufficiently low to preserve the integrity of the oxide layer, whereas transport through pinholes becomes dominant if T_{ann} is sufficiently high to induce the formation of pinholes in the oxide [1,4]. The formation of pinholes upon thermal annealing has been experimentally confirmed in several recent works by means of various techniques, such as transmission electron microscopy (TEM) [5-9], electron-beam-induced current (EBIC) measurements [8], selective etching in TMAH followed by optical microscopy and scanning electron microscopy (SEM) [10], and, indirectly, by I-V measurements on micrometer-sized passivating contacts [11]. Visualization of pinholes has also been attempted by means of conductive atomic force microscopy (c-AFM) [9,12], although the areal density of the localized conduction paths in the c-AFM current maps does not seem to correlate with the actual pinhole density [13]. Parameters such as the oxide thickness, the oxidation method, the annealing temperature (T_{ann}), and the surface morphology are expected to have an impact on the charge carrier transport. However, no systematic study has been conducted to our knowledge to establish how these parameters affect the physical mechanisms of charge carrier transport through the SiO_x.

The aim of this work was to build a comprehensive understanding of the impact of several parameters on the transport mechanisms through the SiO_x in poly-Si passivating contacts, in order to provide guidance for optimization of solar cells incorporating this type of contact structure. We carried out a systematic investigation for a wide range of n-type poly-Si passivating contact designs, fabricated using different surface morphologies, annealing temperatures, oxidation methods, and oxide thicknesses. While in previous studies mirror-polished wafers were mostly used [14,15], in this work we used industrially relevant Czochralski-grown (Cz) wafers featuring different surface morphologies: two types of flat surfaces, namely chemically-polished and saw-damage removed (SDR), and a textured surface featuring random pyramids (TXT). Concerning the impact of the annealing process, we chose to vary the annealing temperature while maintaining a fixed annealing duration of 30 min. As the impact of the annealing duration was not thoroughly investigated in this study, it cannot be excluded that a longer or shorter annealing step might also induce variations in the dominant transport mechanisms through the poly-Si passivating contact. Regarding the silicon oxide layers, we chose to work with oxidation methods and oxide thicknesses that might be of interest for industrial applications. To identify the dominant transport mechanisms, we performed temperature (T)-dependent contact resistivity (ρ_c) measurements by means of the transfer length method (TLM). Fitting of the results with analytical models based on the above-mentioned transport mechanisms allowed elucidation of the dominant transport mechanism, and identification of the range of annealing temperatures in which a transition from tunneling to pinhole dominant transport occurs, for each type of oxide and surface morphology studied.

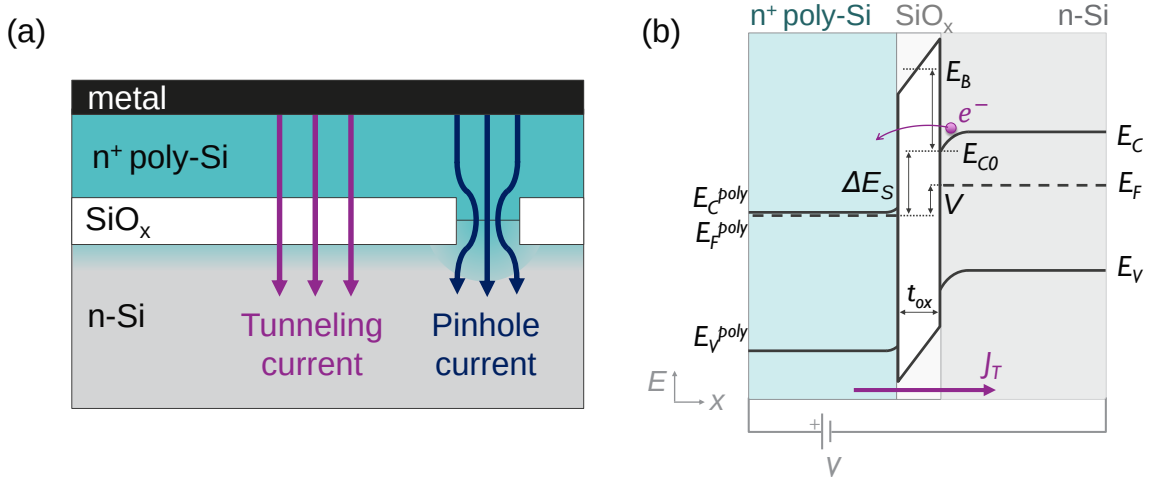

FIGURE 1. (a) Schematic representation of the two main transport mechanisms in an n-type poly-Si passivating contact. The shaded region underneath the oxide layer represents dopant diffusion from the poly-Si into the substrate resulting from thermal treatment. (b) Schematic band diagram, not to scale, of a positively-biased n-type poly-Si passivating contact. The current density (J_T) due to electron tunneling through the oxide barrier is indicated by an arrow. The energy levels indicated by E_C^{poly}, E_V^{poly}, E_C, and E_V represent the conduction and valence band in the doped poly-Si layer and in the wafer, respectively. The other parameters are described in Section 2.1. Notice that the Fermi level in the poly-Si (E_F^{poly}) approaches the conduction band (E_C^{poly}) due to heavy doping. The difference between E_F^{poly} and the Fermi level in the n-Si (E_F) is equal to the applied voltage (V) and becomes negligible at the contact resistance measurement condition (V=0).

2. Theory

The use of *T*-dependent contact resistivity (ρ_c) measurements, which was proposed in recent studies [14,15], is based on the observation that the two models for tunneling and pinhole-mediated transport predict opposite trends of ρ_c as a function of the measurement temperature (*T*): decreasing ρ_c over *T* in case of tunneling-dominant transport and increasing ρ_c over *T* in case of pinhole-dominant transport. Contact resistivity ρ_c ($\Omega \cdot cm^2$), also known as specific contact resistance, is the area-normalized resistance associated with the whole metal/n^+ poly-Si/SiO_x/c-Si contact stack and is an important figure of merit which is widely used in the semiconductor field to assess the quality of contacts [16,17]. In the following, we consider ρ_c as that of the n^+ poly-Si/SiO_x/c-Si stack alone, as the resistance associated with the electron transport through the metal/poly-Si interface is negligible compared to that through the silicon oxide layer and its interfaces with poly-Si and c-Si.

2.1 Tunneling Model

The first mechanism proposed to describe charge carrier transport through the SiO_x film in poly-Si passivating contacts is direct tunneling. Other mechanisms of quantum mechanical transport across an energy barrier, such as thermionic emission or trap-assisted tunneling [18], might also play a role, but they are neglected here for simplicity. Direct tunneling is generally described by means of the metal-insulator-semiconductor (MIS) model. In a poly-Si passivating contact, the poly-Si layer is treated as a metal (M) due to its heavy-doping which causes the Fermi level to approach the conduction band. The SiO_x layer corresponds to the insulator region (I), and the n-Si substrate is the semiconductor region (S). It should be mentioned that a more sophisticated model for poly-Si/SiO_x/c-Si junctions has recently been published where the poly-Si is not treated as a metal [19]. In this work, we based our analysis on the MIS theory. According to the MIS theory, the tunneling contact resistivity $\rho_{c,t}$ at zero bias can be described by [15]:

$$\rho_{c,t} = \frac{n\, k_B}{qA^*TP_T} \cdot \exp\left(\frac{\Delta E_S}{k_B T}\right) \tag{1}$$

where *T* is the absolute temperature, *n* is a factor accounting for non-idealities, k_B is the Boltzmann constant, *q* is the electron charge, and $A^*=4\pi q m^* k_B^2/h^3$ is the effective Richardson constant, which depends on the electron effective mass in the semiconductor (m^*). The term P_T is the tunneling probability, which can be written as [15]:

$$P_T = \exp\left(-t_{ox}\sqrt{\frac{8m_t E_B}{\hbar^2}}\right) \tag{2}$$

where m_t is the tunneling mass, corresponding to the electron effective mass in the oxide conduction band, and $\hbar$ is the reduced Planck constant. The other parameters are depicted in Fig. 1(b): E_B is the average energy barrier height with respect to the conduction band edge at the SiO_x/n-Si interface (E_{C0}), ΔE_S is the energy barrier seen from the poly-Si, i.e. the difference between E_{C0} and the poly-Si Fermi level ($E^{poly}{}_F$), and t_{ox} is the barrier width, which we assume equal to the oxide thickness. The temperature dependence in the tunneling model derives from the Boltzmann approximation of the Fermi-Dirac distribution, which is introduced when the tunneling probability is integrated over all available electron energy states [20]. Notice that $\rho_{c,t}$ decreases with increasing *T*. This is because, according to the Boltzmann statistics, at higher *T* there is a higher chance to find electrons in high energy states. The thermally excited electrons see an energy barrier with a lower effective height and can therefore tunnel more easily through the oxide barrier, resulting in a larger tunneling current and thus lower values of $\rho_{c,t}$ at high *T*.

2.2 Pinhole Model

The second model for charge carrier transport in poly-Si passivating contacts is drift-diffusion through pinholes in the oxide layer. As suggested in [15], an oxide layer with pinholes can be treated as a field of circular openings of effective radius r_P and areal density N_P. Current flow from the poly-Si constricts through the pinholes, and diverge into the c-Si substrate, introducing two spreading resistance terms. However, the first term is negligible due to low bulk resistivity of the heavily doped poly-Si. The resistive term for the current spread into the substrate can be

calculated using the model proposed by Cox and Strack [21]. By combining the pinhole density with the spreading resistance of each pinhole, we can then obtain the total contact resistivity as [15]:

$$\rho_{c,p} = \frac{1}{N_P} \cdot \frac{\rho_B(T,N_D)}{2\pi r_P} \cdot \arctan\left(\frac{2t}{r_P}\right) \quad (3)$$

where r_P is the pinhole effective radius, N_P is the pinhole areal density, ρ_B is the weighted average of the bulk resistivity in the c-Si region within depth t, and t is the thickness of the c-Si layer below the pinhole within which the current spreading occurs. The bulk resistivity of the substrate depends on both T and N_D, which is the dopant density in the semiconductor region. A complete model for ρ_B can be found in the work by Klaassen [22,23]. The doping concentration in the c-Si below the poly-Si/c-Si interface is expected to be non-uniform due to in-diffusion of dopants from the poly-Si layer during annealing. The temperature dependence of ρ_B can thus be qualitatively different for the range of N_D within the considered substrate region [23]. For our samples, we expect average N_D values in the range of $10^{15} - 10^{17}$ cm^{-3}, as estimated from doping concentration profiles obtained by scanning spreading resistance microscopy (SSRM). For N_D within this range, Klaassen's model predicts qualitatively similar profiles corresponding to an increase of ρ_B with increasing T, which is mainly due to increased scattering events between the electrons and various types of scattering centers, such as donor impurities, lattice sites, and holes [22,23]. Notice that $\rho_{c,p}$ depends on T only through ρ_B. As a consequence, $\rho_{c,p}$ increases with increasing T, showing an opposite behavior as compared to $\rho_{c,t}$.

3. Methods

3.1 Sample Fabrication

The sample structure used for the temperature-dependent contact resistivity measurements is schematically represented in Fig. 2(a) and (b). The main fabrication steps are summarized in Fig. 2(c). N-type crystalline Si Cz wafers were used featuring three different surface topographies (Fig. 3), namely random pyramid textured (TXT) and two types of flat surfaces: polished and saw-damage removed (SDR). The SDR surface typically consists of flat craters on the Si surface, produced by etching away the surface damage resulting from diamond wire sawing, in a 20% potassium hydroxide (KOH) solution. Random pyramid textured surface is the industry standard surface texture, produced by anisotropic etching of (100) Si wafers in 1.5% KOH solution in the presence of additives, which renders Si pyramids with a base size of 3-5 µm with (111) facets. The polished surfaces have the smoothest surface of the three under study, and are produced by isotropic etching of Si wafers with random pyramid textured surfaces in a mixture of hydrofluoric acid (HF) and nitric acid (HNO_3).

Four different interfacial SiO_x layers were grown as reported in Table 1: (i) a 1.3 nm thick wet-chemical SiO_x grown in ozonated (O_3) de-ionized water (H_2O) at room temperature, (ii) a 1.5 nm thick thermal SiO_x grown in a low-pressure tube furnace at 610°C, (iii) a 2 nm thick thermal SiO_x grown in a tube furnace at 820°C at atmospheric pressure, and (iv) a 2 nm thick thermal SiO_x grown by plasma-enhanced atomic layer deposition (PEALD) at 300°C by using a Si precursor and an O_2 plasma generated by an RF power of 600 W. The oxide thicknesses were measured by ellipsometry and cross-section transmission electron microscopy (TEM), yielding consistent values. In the following analysis, the oxide thickness values obtained from TEM were used. Next, a ~150 nm thick *in situ* phosphorus (P) doped polycrystalline silicon (poly-Si) layer was deposited by low pressure chemical vapor deposition (LPCVD). A wet-chemical oxide layer was grown in H_2O:O_3 on top of the poly-Si layer right before annealing to prevent dopant effusion [24]. Samples were then subjected to thermal anneal in a nitrogen flow for 30 min at different T_{ann} (700–1050°C). For T_{ann} up to 800°C, 5 min were added before the annealing step to reach thermal equilibrium. For T_{ann} above 800°C, the 30 min annealing step was preceded by a +5°C/min ramp up and followed by a -3.3°C/min ramp down of the temperature to a base value of 800°C. For the annealing conditions which are most promising to achieve a high carrier selectivity, symmetrical samples were prepared by depositing SiN_x:H by plasma enhanced chemical vapor deposition (PECVD) onto the poly-Si/SiO_x stacks on both sides of the samples.

Metal contacts for transfer-length method (TLM) measurements were realized by electron-beam (e-beam) evaporation of titanium (Ti) and aluminum (Al) through a shadow mask with the design depicted in Fig. 2(b). The metal pads had a size of 0.5×2 mm^2, with increasing spacing from 0.5 mm to 8 mm. To ensure good contacting, the samples were dipped for 1 minute in 5% HF:H_2O right before metallization to remove the chemical oxide layer on the poly-Si surface grown before annealing. The test structures were then dry-etched in a mixture of SF_6, CF_4, and

O_2 at 0.3 mbar to selectively remove the poly-Si/SiO_x stack between the contact pads (Fig. 2(a)). This would ensure that the current between contact pads will flow through the oxide layer during ρ_c measurements. Based on the etching rate, we estimate that a portion of c-Si as deep as 200 nm from the SiO_x/c-Si interface would be removed during the etch process. Samples were then laser-diced at all four edges to avoid artifacts in the TLM measurements related to lateral current spreading or to shunt paths caused by residues of evaporated metal at the edges of the samples.

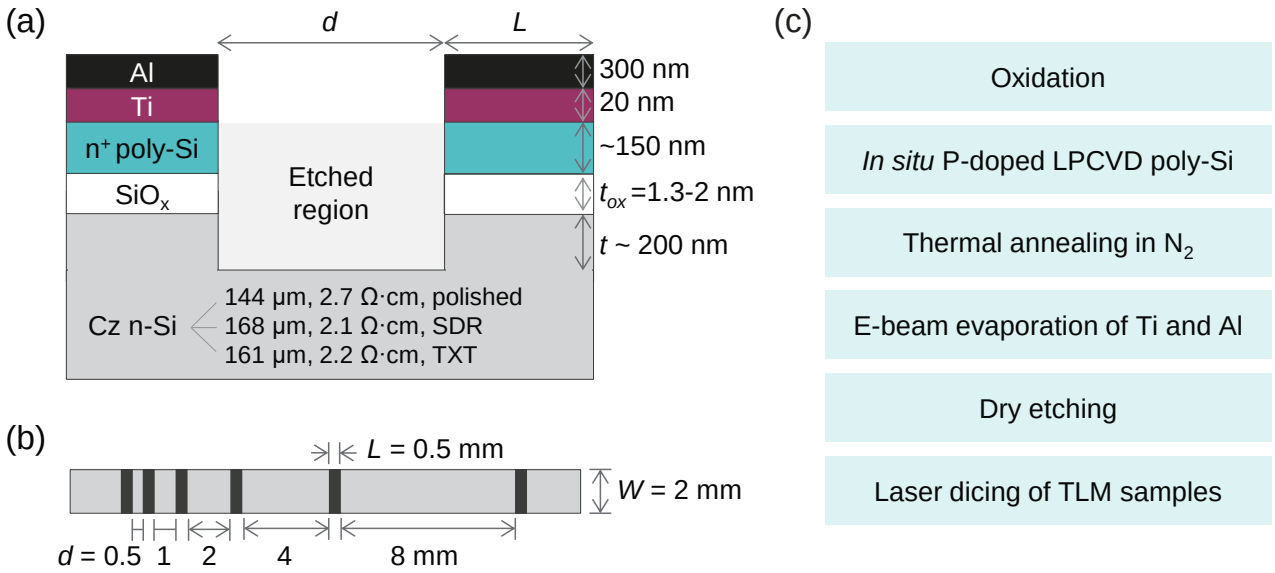

FIGURE 2. (a) Schematic cross section (not drawn to scale) for a single contact pair and (b) top view of a sample prepared for *T*-dependent TLM measurements. (c) Summary of the main fabrication steps.

TABLE 1. Summary of the different SiO_x layers used in this work.

Oxidation method	**Process details**	**Thickness (nm)**
Wet-chemical	H_2O:O_3 at 25°C	1.3
Thermal	low-pressure tube furnace at 610°C	1.5
Thermal	atmospheric-pressure tube furnace at 820°C	2
Plasma-enhanced atomic layer deposition (PEALD)	Use of a Si precursor and O_2 plasma at 300°C	2

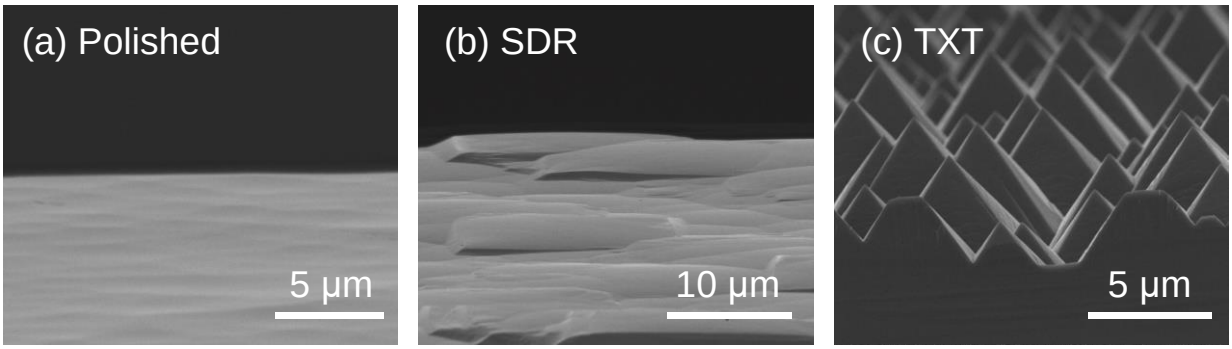

FIGURE 3. Scanning electron microscopy (SEM) images of the three wafer types used in this work featuring a (a) polished, (b) saw-damage removed (SDR), or (c) random pyramid textured (TXT) surface.

3.2 Determination of contact resistivity by Transfer Length Method (TLM)

The contact resistivity in our samples was determined by means of the transfer length method (TLM) at various measurement temperatures. TLM measurements consist of measuring *I-V* curves between several pairs of adjacent contacts situated at increasing contact spacing (Fig. 2b). The resistance between each pair of contacts, extracted from the *I-V* curves, is expected to increase linearly with the contact spacing due to the lateral resistance in the semiconductor. According to the theory of TLM, the contact resistivity can be extracted from the intercept of a linear fit, whereas the sheet resistance of the substrate can be extracted from the slope [16].

T-dependent four-terminal TLM measurements were carried out in a broad range of *T* (78–473 K) using two setups: one setup with a temperature-controlled chuck for measurements in the temperature range of 273–473 K at atmospheric pressure, and one setup with a liquid nitrogen-cooled cryostat for measurements in the temperature range of 78–295 K performed under vacuum to avoid ice formation. A Keysight B1500A parameter analyzer was used in both setups for obtaining the *I-V* curves. During each measurement, the chuck temperature was maintained within ±0.05 K from the target temperature. Data were then analyzed based on the TLM procedure. The total resistance (R_{tot}) between each pair of contacts was extracted from the slope of a weighted linear fit to the corresponding *I-V* dataset with weights derived from the systematic uncertainties of *I* and *V*, estimated from the precision of the parameter analyzer. The fit was restricted to the 21 closest data points to zero bias, corresponding to the voltage range (-10 mV, 10 mV). TLM plots were then obtained by plotting R_{tot} against the contact distance *d*. The TLM plots showed different behaviors and were thereby classified into two types: Type I plots showed linear increase of R_{tot} over *d* (Fig. 4(a)) as expected from the TLM theory, whereas Type II plots showed no significant increase of R_{tot} over *d* (Fig. 4(b)) due to very high contact resistance values, which resulted in a negligible contribution of the lateral transport to the R_{tot} measured. In the analysis of type II plots, we neglected the resistance of the semiconductor between the contacts and considered each R_{tot} value to be an independent measurement of two times the contact resistance of a contact pad.

As the contact resistivity (ρ_c) may not be extracted following a single method for the two types of plots, selection criteria were established to classify the plots into the two categories: a plot was considered of type I if R^2 of a linear fit was > 0.99, and of type II if $R^2 < 0.99$ and the standard deviation of R_{tot} was < 5% of its mean value. To extract the contact resistivity (ρ_c) in type I plots, we solved the implicit equation derived by Eidelloth and Brendel to account for the 2-D current flow in the wafer [25]. The formula for the 2-D correction requires a finite value of the slope; therefore, it could only be used for type I plots, but not for type II plots. As type II plots were observed only for high ρ_c values above 1 Ω cm^2, the correction due to the 2-D current flow can be considered negligible.

To extract the contact resistivity (ρ_c) in type II plots, we first extracted the contact resistance (R_C) from the mean value of R_{tot} as suggested in [15], then we solved the implicit equation derived from the transmission line model [26]:

$$R_C = \frac{\sqrt{R_S \rho_C}}{\mathrm{W}} \cdot \coth\left(L\sqrt{\frac{R_S}{\rho_C}}\right) \tag{4}$$

, where W = 2 mm and L = 0.5 mm are the width and length of the contact pads as shown in Fig. 2(a), and R_s is the sheet resistance of the c-Si substrate, which might vary as a function of depth due to the possible in-diffusion of dopants from the n^+ poly-Si film into the wafer during annealing. Even though values of R_s were measured by means of four-point probe on the wafers prior to processing, such values could not be used to extract the contact resistivity as they do not account for the possible in-diffusion of dopants mentioned above. Moreover, the value of sheet resistance could also not be extracted from the type II TLM plots as the measurement was not sensitive to the resistive contribution of the lateral transport, resulting in approximately zero slope. Therefore, for type II plots, we estimated ρ_c as the average of three calculations considering three different values of sheet resistance (1, 50, 100 Ω/sq), arbitrarily chosen in the range of values obtained from type I plots on similarly fabricated samples. This choice is justified since some preliminary calculations showed that the resulting value of ρ_c does not depend significantly on the sheet resistance value in case of type II plots. The error introduced by this approach, estimated as the semi-difference between the maximum and minimum value among the three calculated, is within 1.2% of the average value. Error bars were obtained by adding this error to the experimental uncertainty by root sum squared. It should be noted that, in addition to type I and type II plots, for certain samples and measurement temperatures the behavior of R_{tot} was neither linearly increasing with nor independent of d but showed a non-linear trend instead (see Fig. 4(c)). As no contact resistivity could be extracted from non-linear plots, these data were discarded.

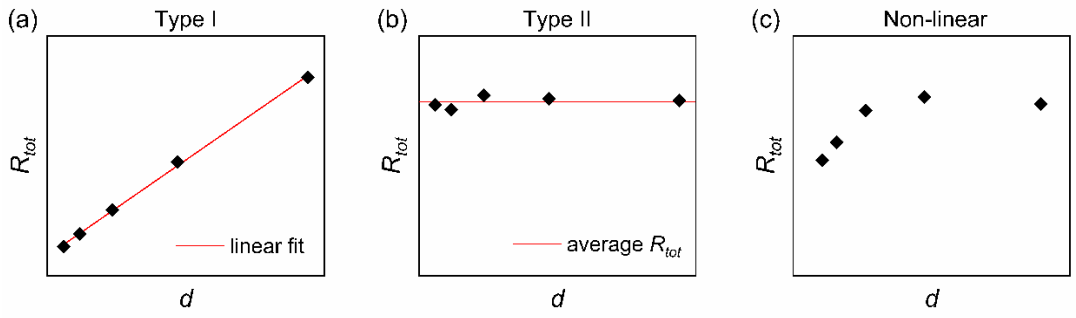

FIGURE 4. Examples of TLM plots, i.e. plots of the total resistance (R_{tot}) between each pair of contacts of TLM structures as a function of the contact distance (d). (a) Type I plots show linear increase of R_{tot} over d, while (b) Type II plots show no significant increase of R_{tot} over d. (c) Non-linear plots which could not be classified as Type I or Type II were discarded.

3.3 Uncertainty Evaluation

Error bars associated with ρ_c were obtained from a Monte Carlo evaluation of uncertainty distributions as advised by the Guide to the Expression of Uncertainty in Measurements [27]. Simple propagation of errors could not be used, since ρ_c was derived by numerically solving a non-linear implicit equation (Eq. (4)). In the Monte Carlo simulations, we assumed that the input parameters of our model – namely R_{tot}, the contact distance (d), length (L) and width (W) – were normally distributed around their measured values. The uncertainty (Gaussian widths) in d, L, and W was obtained from the standard deviation of the contact dimensions measured by optical microscopy, and determined to be 20 µm. The width of the R_{tot} distribution was estimated from a propagation of the systematic errors in I and V in case of type I plots, and from the standard deviation of the measured values for all pairs of contact pads in case of type II plots. The Monte Carlo simulations were repeated 1000 times for each ρ_c value. At each iteration, random values of $\{R_{tot}, d, L, W\}$ were generated according to the probability distributions and then used to calculate ρ_c. Error bars were then obtained as the standard deviation of the 1000 simulated ρ_c values.

3.4 Fit to the models

The data obtained were finally fitted to the two transport models by means of a weighted least-squares minimization. For the tunneling model, Eq. (1) was used, assuming n = 1 and A^* = 120 $cm^{-2}K^{-2}$ [18]. The oxide thickness t_{ox} was set to the average value obtained from TEM images, and the energy barrier E_B was set to 3.2 eV, estimated from the difference between the electron affinity of c-Si and of SiO_x in the ideal case of defect-free interfaces [18]. The fit for the tunneling model was performed by varying the tunneling mass (m_t) and ΔE_S in the ranges 0–1 (units of the free electron mass m_0) [30] and 0–1 eV, respectively, with starting values of 0.3 m_0 and 0.04 eV, respectively, based on the findings reported in [14].

For the pinhole model, Eq. (3) was used. As described above, the quantity t in Eq. (3) is the distance that the electrons travel vertically in the c-Si layer below the pinholes for current spreading to be complete. This quantity could not be determined experimentally. However, as already pointed out in [15], Eq. (3) saturates for sufficiently large t due to the arctangent function in the formula. For our samples, we calculated that the saturation of $\rho_{c,p}$ occurs for t above 50-60 nm. This means that any value of t above the saturation point would introduce only negligible variations in the calculated $\rho_{c,p}$. In the absence of a more reasonable estimate, we assume that the current spreading takes place over the entire depth of the etched region below the SiO_x/c-Si interface and terminates where the electrons reach the etch depth and start traveling horizontally to the next contact pad. This simplified picture leads us to assume t equal to the depth of the etched c-Si, which we estimated as 200 nm (Fig. 2(a)). To perform the fit to the pinhole model, we varied the other parameters in Eq. (3), namely r_P, N_P, and N_D, in the intervals of 2–20 nm [6], 10^5–10^8 cm^{-2} [10], and 10^{15}–10^{17} cm^{-3}, respectively.

3.5 Lifetime measurements

Minority carrier lifetime measurements were performed to assess the selectivity of the poly-Si passivating contacts under study. The measurements were carried out on the annealed samples using a BT Imaging equipment. From the lifetime data we extracted the implied open circuit voltage (iV_{oc}) as well as the recombination current density (J_0). The J_0 values were obtained by the Kane and Swanson method [28] at an injection level of $\Delta n = 10^{16}$ cm^{-3}.

4. Results and Discussion

4.1 Thermal Oxide, 1.5 nm Thick

Figure 5 shows the results of T-dependent ρ_c measurements performed on samples with a 1.5 nm thick thermal oxide fabricated on chemically-polished, SDR, and TXT surfaces, annealed at T_{ann} = 850°C (Fig. 5(a)), T_{ann} = 900°C (Fig. 5(b)), and T_{ann} = 950°C (Fig. 5(c)). Most of the ρ_c values were extracted from type I linear TLM plots (Fig. 4(a)), with the exception of the data points measured at $T \leq 225$ K on the polished sample annealed at T_{ann} = 900°C (Fig. 5(b)), which were extracted from TLM plots of type II (Fig. 4(b)). Solid lines in Fig. 5(a) and Fig. 5(c) represent the best curves obtained from a least-squares fit to Eqs. (1) and (3), respectively. The behavior in Fig. 5(b) could not be modeled by either of these equations as it probably results from a superposition of both transport mechanisms.

By comparison of the results in Fig. 5 with the models reported in Eq. (1) and (3), it can be concluded that direct tunneling is the dominant transport mechanism in our poly-Si passivating contacts featuring a 1.5 nm thick thermal oxide annealed at T_{ann} = 850°C, whereas drift-diffusion through pinholes prevails at the higher T_{ann} = 950°C. A coexistence of both mechanisms is probably present in the samples annealed at the intermediate T_{ann} = 900°C. From this, we can infer that a continuous transition from tunneling-dominant to pinhole-dominant transport is induced by increasing T_{ann}. Such a transition is likely due to structural modifications in the oxide layer during the annealing process. For T_{ann} below the transition, the oxide is expected to have remained continuous and thus tunneling prevails, whereas higher T_{ann} probably led to local thinning and formation of nanopits and pinholes in the oxide. Compared to the tunneling-dominant regime (Fig. 5(a)), a significant drop in ρ_c occurs in the pinhole-dominant regime (Fig. 5(c)). This shows that, for the thermal SiO_x under study, transport through pinholes is more efficient than tunneling. Measurements performed on samples annealed at even higher T_{ann} (not shown here) confirm that ρ_c continues to decrease further with increasing T_{ann}, which is attributed to increased pinhole formation, increased average size of the poly-Si crystal grains [7], and increased diffusion of dopants from the poly-Si into the substrate [29], which might in turn lead to enhanced tunneling [30]. While the drop in ρ_c with increasing T_{ann} is desirable, very high T_{ann} leads to very high pinhole densities. Since pinholes are essentially unpassivated regions, very high pinhole densities result in poor passivation quality, thus leading to a trade-off between ρ_c and passivation quality [31]. The results of lifetime measurements, reported in Section 4.5, show that a low ρ_c and good passivation quality for samples with a 1.5 nm thick thermal oxide can be achieved for T_{ann} in the range of 900–950°C.

Interestingly, the ρ_c-T trends in Fig. 5 are independent of the wafer type, which indicates that the dominant transport mechanisms are not affected by the surface morphology. Nevertheless, a significant drop in ρ_c by a factor of 3–4 at 300 K was observed on TXT surfaces in the tunneling regime (T_{ann} = 850°C), while the ρ_c values were

similar in both SDR and polished samples. This drop could be partly explained by the increased actual contact area on TXT wafers compared to planar surfaces by a geometrical area factor of ~1.7. However, as the drop in ρ_c is greater than the one resulting from a ~1.7 times larger contact size, we speculate that additional structural modifications in the SiO_x, such as local thinning or poorer thickness uniformity [32,33,34], might occur in TXT samples leading to (locally) enhanced electron tunneling.

The parameters extracted from the fits of Fig. 5 are in reasonable agreement with the literature, which corroborates the validity of the considered transport models. Nevertheless, the reader should be aware that the values extracted from the fit may not be precise, as they are prone to error and very sensitive to the values of the input parameters, which are not known precisely. For the three tunneling samples (Fig. 5(a)), we obtained an average tunneling mass m_t = 0.46 m_0, which is larger than 0.23–0.25 m_0 reported in similar works [14,15], but lies in the range of 0.3–0.95 m_0 indicated in [30]. The values of ΔE_S were between 20 meV and 49 meV, in agreement with [14]. For the three pinhole samples (Fig. 5(c)), we extracted r_P in the range of 7–19 nm and N_P in the range of 5.0×10^{6}–1.1×10^{7} cm^{-2}, similarly to the values reported in [6] and [10], respectively. The values obtained for N_D, in the range of 2.5×10^{15}–1.5×10^{16} cm^{-3}, were slightly larger than the dopant concentration of the substrate, which we estimated as 2×10^{15} cm^{-3} from sheet resistance measurements. The larger values of dopant concentration might be caused by the diffusion of dopants from the poly-Si into the substrate during the annealing treatment, as mentioned above.

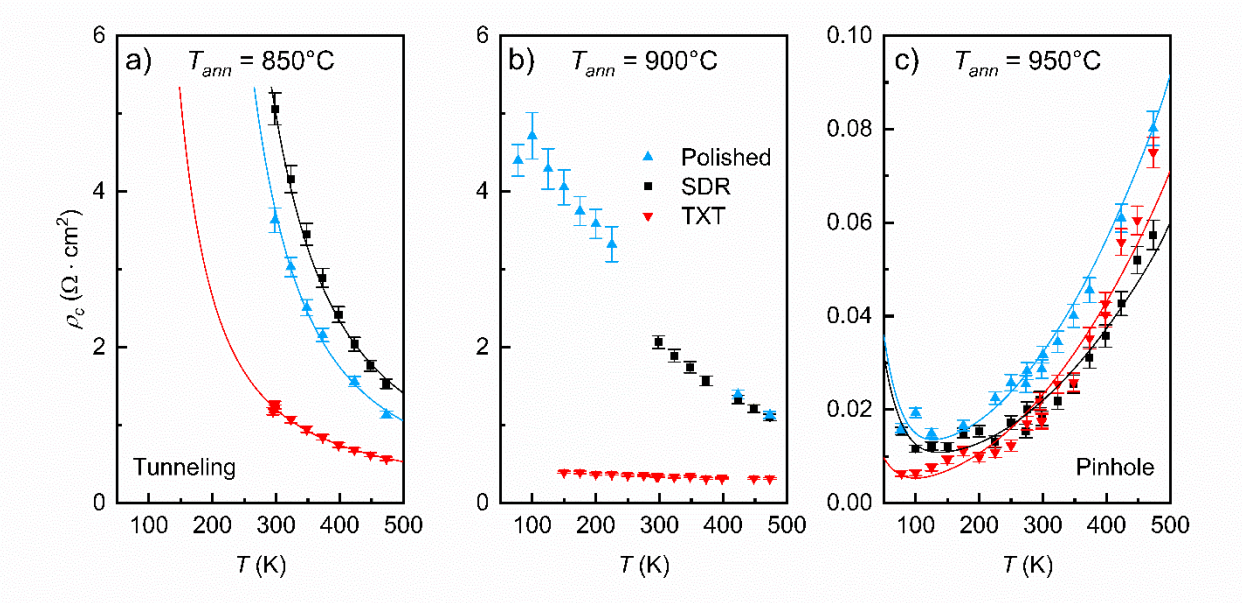

FIGURE 5. Contact resistivity (ρ_c) as a function of measurement temperature (T) for samples with a 1.5 nm thick thermal oxide on polished, SDR, and TXT wafers. The samples were annealed at different annealing temperatures (T_{ann}): (a) 850°C, (b) 900°C, and (c) 950°C. Solid lines in (a) and (c) show the best fit to Eqs. (1) and (3), respectively.

4.2 Wet-chemical Oxide, 1.3 nm Thick

Figure 6 shows the T-dependent ρ_c results for poly-Si passivating contacts featuring a 1.3 nm thick wet-chemical oxide. The ρ_c values measured at $T \leq 150$ K on the two samples annealed at T_{ann} = 700°C (Fig. 6(a)) were extracted from TLM plots of type II (Fig. 4(b)), whereas all the other data points were obtained from TLM plots of type I (Fig. 4(a)). Solid lines in Fig. 6(a) represent the best fit to Eq. (1) while those in Fig. 6(b) and Fig. 6(c) are fitted using Eq. (3). A transition from tunneling-dominant to pinhole-dominant transport was observed for increasing T_{ann}, similarly to the samples with a 1.5 nm thick thermal oxide (Fig. 5). However, the transition occurred at remarkably lower T_{ann}, as a thermal treatment at 750°C was sufficient to induce pinhole-dominant transport across the wet-chemical oxide, compared to the 950°C required in case of the 1.5 nm thick thermal oxide. This result suggests that wet-chemical oxides are less resistant to thermal annealing compared to thermally grown SiO_x. It should be noted that the wet-chemical SiO_x under study was slightly thinner than the thermal oxide, which could partly explain why

pinholes might have formed at a lower thermal budget. However, a different stoichiometry between wet-chemical and thermal oxides due to the different oxidation methods might have also contributed to modify the oxide structural properties [35].

Interestingly, the contact resistivity measured on the TXT tunneling sample annealed at 700°C seems to change behavior for $T > 350$ K, showing an increase which is typical of increased electron scattering (inset in Fig. 6(a)). This anomaly was not observed on the SDR sample annealed at the same temperature. The origin of such increase is unclear. On the one hand, such a trend cannot be the result of the superposition of both transport mechanisms, i.e. tunneling-dominant transport at low T and pinhole-dominant transport at high T, because the two contributions should be added as resistors in parallel [15], which would lead to a shape with the opposite convexity. On the other hand, the observed trend could be compatible with a superposition of two resistive contributions in series: the ρ_c due to tunneling transport through the oxide, which leads to the increase at low T, and the series resistivity ($\rho_B(T)$) of the c-Si, which might become the limiting mechanism at high T due to increased electron scattering. However, the absence of such series contribution in the otherwise identical SDR sample does not support this interpretation. Therefore, no model can be currently provided that thoroughly describes the observed behavior.

From the fit to the tunneling model we extracted an average tunneling mass $m_t = 0.44\ m_0$ and ΔE_S in the range of 39–53 meV, which are in agreement with [30] and [14], respectively. From the fit to the pinhole model we obtained r_P in the range of 6–17 nm and N_P in the range of 5.2×10^6–7.0×10^7 cm^{-2}, which are comparable with the values reported in [6], [10], respectively. The fitted values of N_D were in the range of 1.3×10^{15}–9.7×10^{15} cm^{-3}, which is slightly larger than the measured dopant concentration of our wafers, in agreement with the hypothesis of in-diffusion from the poly-Si layer. As expected, higher pinhole densities are achievable in wet-chemical oxide layers at lower temperatures, as compared to the thermal oxide.

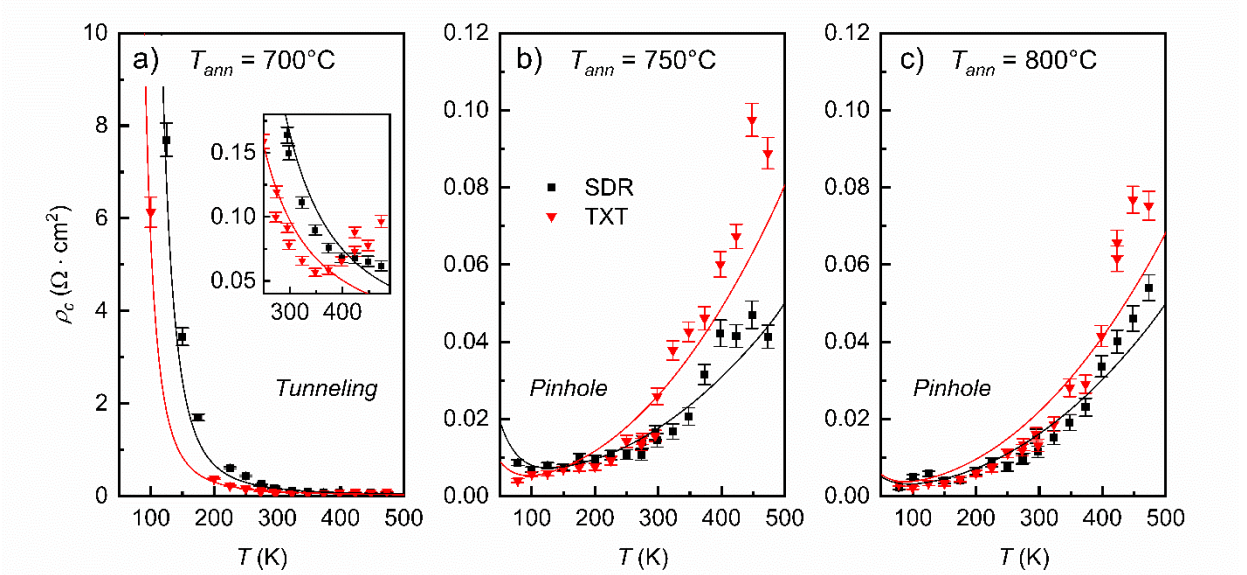

FIGURE 6. Contact resistivity (ρ_c) as a function of measurement temperature (T) for samples with a 1.3 nm thick wet-chemical oxide on SDR and TXT wafers. The samples were annealed at different annealing temperatures (T_{ann}): (a) 700°C, (b) 750°C, and (c) 800°C. Solid lines in (a) show the best fit to Eq. (1), while solid lines in (b) and (c) show the best fit to Eq. (3). The inset in (a) is a magnified view of the plot from 250 K to 500 K. The increase of ρ_c for $T > 350$ K was only observed in the TXT sample and is not well understood yet.

4.3 Thermal and PEALD Oxides, 2 nm Thick

From T-dependent ρ_c measurements it was found that 2 nm thick SiO_x layers, grown either thermally (Fig. 7(a)) or by plasma-enhanced atomic layer deposition (PEALD) (Fig. 7(b)), are more robust to annealing compared to thinner oxides, as they show pinhole-dominant transport only for very high T_{ann} = 1050°C. A higher annealing temperature is needed to enter the pinhole regime in this case because thicker oxides require a higher amount of energy to activate their lattice reorganization compared to thinner oxides. In samples with 2 nm thick oxides annealed at T_{ann} = 1000°C or below, no significant current through the SiO_x could be measured, similarly to the

findings of previous works [29, 36]. This result suggests that neither tunneling nor pinholes offer an efficient current path for charge carrier transport across 2 nm thick oxides annealed at $T_{ann} \leq 1000$°C. On the one hand, thermal treatments at $T_{ann} \leq 1000$°C seem not to provide sufficient energy to activate the reorganization of a 2 nm SiO_x layer, probably resulting in a pinhole density that is too low and yielding negligible pinhole current. On the other hand, the tunneling current across 2 nm thick oxides is negligible compared to similar samples with thinner oxides, as the tunneling probability decreases exponentially with the oxide thickness (see Eqs. (1) and (2)). A significant charge carrier transport through 2 nm thick oxide layers can therefore be achieved only by annealing at 1050°C or more to induce a sufficiently large pinhole density.

The ρ_c values shown in Fig. 7 were all extracted from TLM plots of type I (Fig. 4(a)). Comparing the data for the 2 nm thick thermal oxide (Fig. 7(a)) to the pinhole model, we obtained r_P, N_P, and N_D of about 9 nm, 5.7×10^6 cm^{-2}, and 7.6×10^{15} cm^{-3}, respectively. Although the $\rho_c - T$ plot for the PEALD oxide shows a clear increase indicating pinhole behavior, the best fit to the pinhole model did not match the data well, leading to a poor quality of fit and it is thus not shown (Fig. 7(b)). Therefore, no values of r_P, N_P, and N_D can be reported for the PEALD sample.

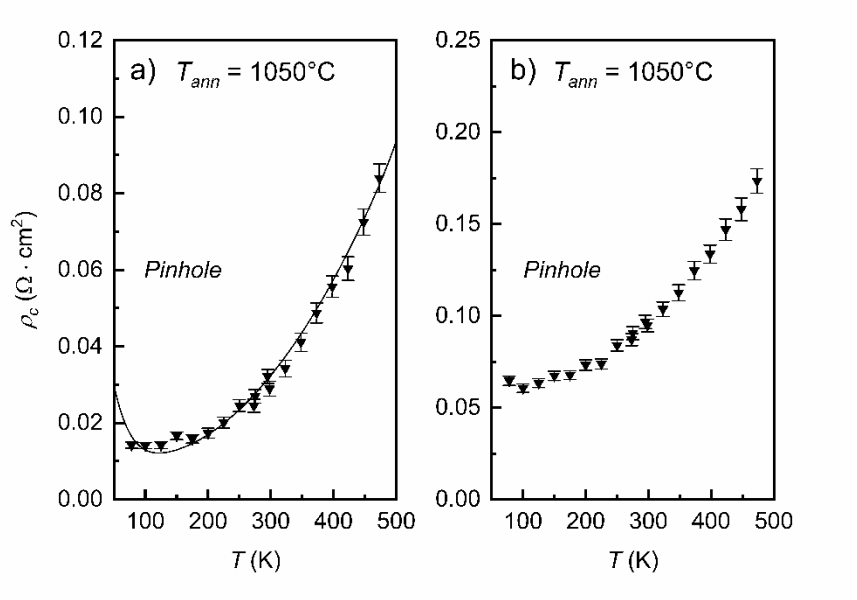

FIGURE 7. Contact resistivity (ρ_c) as a function of measurement temperature (T) for textured samples with a 2 nm thick oxide, grown (a) thermally and (b) by plasma-enhanced atomic layer deposition (PEALD). The samples were annealed at 1050°C. The solid line shows the best fit to Eq. (3). The best fit of the data in (b) to Eq. (3) is not shown as only a poor fit quality could be achieved.

4.4 Summary of the transport mechanisms

A summary of the results of T-dependent ρ_c measurements on all samples fabricated with different oxides is given in Table 2. It can be observed that the dominant electron transport mechanism through a poly-Si passivating contact depends on the oxide type and thickness as well as T_{ann}. At low T_{ann}, tunneling is the dominant charge transport mechanism, provided a low enough SiO_x thickness < 2 nm to facilitate current flow by tunneling. For 2 nm thick oxides, no significant carrier transport occurred at low T_{ann}. Beyond a certain threshold in the T_{ann}, which depends on the oxide type and thickness, it is possible to induce pinhole dominant transport for all types of SiO_x films studied, leading to a significant drop in ρ_c compared to that in the tunneling dominant regime.

TABLE 2. Summary of the dominant electron transport mechanisms through four types of SiO_x films in poly-Si passivating contacts. The transitions between the two mechanisms described in the two right-most columns were observed in the range of T_{ann} reported in the third column.

Oxide type	**Thickness (nm)**	***T_{ann}* at transition**	**Dominant electron transport mechanism**	
			Below transition	**Above transition**

Wet-chemical	1.3	700°C – 750°C	Tunneling	Pinhole
Thermal	1.5	850°C – 950°C	Tunneling	Pinhole
Thermal	2	1000°C – 1050°C	None	Pinhole
PEALD	2	1000°C – 1050°C	None	Pinhole

4.5 Passivation results

Figure 8 shows the results of the lifetime study performed on the samples with thermal and wet-chemical oxides, annealed at various T_{ann}. It is important to note that no hydrogenation was applied to these samples, as these were not optimized for the lifetime study, leading to relatively high values of J_0 and low values of iV_{oc}. In particular, the sample with a 1.5 nm thick thermal oxide annealed at 1050°C and the samples with a wet-chemical oxide could not reach an injection level of 10^{16} cm^{-3} during the lifetime measurements. Hence, no J_0 but only iV_{oc} values are reported for these samples in Fig. 8. For the other samples, both iV_{oc} and J_0 values are shown. The passivation quality of the samples with the PEALD oxide was not assessed, as passivating contacts incorporating the PEALD oxide were found to not show promise for application in high-efficiency solar cells due to the corresponding contact resistivity remaining very high, above 94.7 mΩ cm^2.

The results in Fig. 8 show that the passivation quality improves with increasing T_{ann} even when the carrier transport mechanism through the oxide becomes pinhole dominant. Nevertheless, deterioration of the passivation quality is expected for extremely high T_{ann}, as demonstrated by the result of the sample with a 1.5 nm thick thermal oxide annealed at 1050°C.

The results of the lifetime and contact resistivity measurements show that a good trade-off between low ρ_c and low J_0 can be achieved with the samples with a 1.5 nm thick thermal oxide annealed at 950°C. To demonstrate the full potential of the passivating contact fabricated with these process parameters, the lifetime measurement was repeated on such samples after hydrogenation, fabricated on polished and TXT wafers (Fig. 8). As expected, the hydrogenation leads to a significant improvement of the passivation quality. For the textured sample we obtained J_0 = 2.4 fA cm^{-2} and iV_{oc} = 745 mV, while for the polished sample we measured J_0 = 0.8 fA cm^{-2} and iV_{oc} = 755 mV, which correspond to selectivity values at room temperature of S_{10} = 14.8 and S_{10} = 15, respectively, using the definition of carrier selectivity proposed in [37].

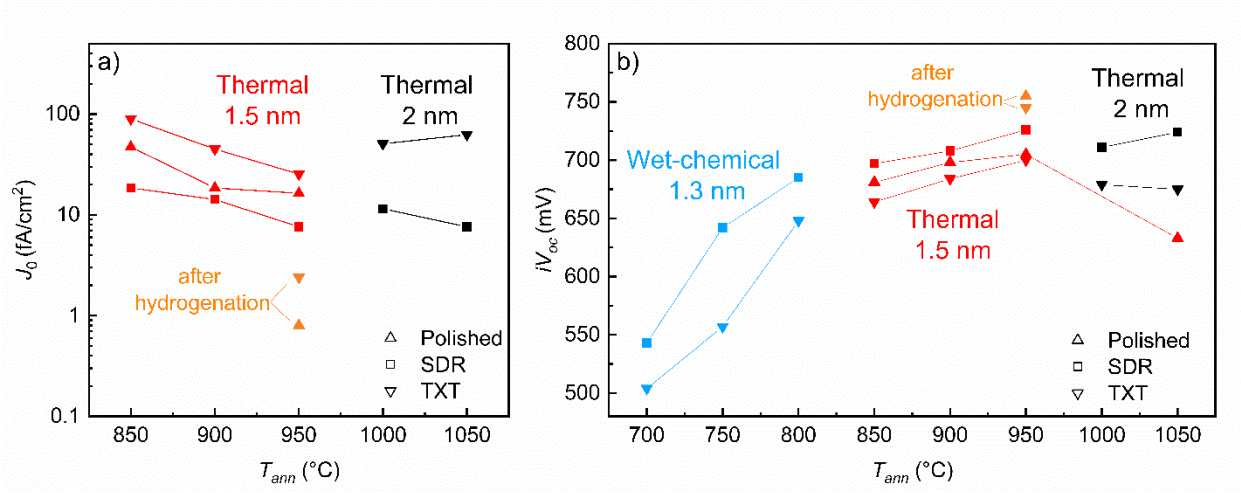

FIGURE 8. (a) Saturation current density (J_0) and (b) implied V_{oc} (iV_{oc}) as a function of the annealing temperature (T_{ann}) for polished, saw-damaged removed (SDR), and textured (TXT) samples with a 1.3 nm thick wet-chemical oxide, and 1.5 nm and 2 nm thick thermal oxides. The solid lines are guides to the eye. The injection level in the sample with a 1.5 nm thick thermal oxide annealed at 1050°C and in the samples with a wet-chemical oxide did not reach 10^{16} cm^{-3}, hence no J_0 values are reported. The samples were not hydrogenated, unless otherwise specified. Notice that the passivation quality keeps improving with increasing T_{ann} even in the pinhole dominant regime. Nevertheless, a deterioration of the passivation quality is expected at extremely high T_{ann}.

5. Conclusion

In this work, a systematic investigation was carried out to provide insights on the charge carrier transport mechanisms through different SiO_x layers in poly-Si passivating contacts. *T*-dependent ρ_c measurements, performed by means of TLM in the temperature range of 78–473 K, show that the nature of the prevailing transport mechanism is affected by the annealing temperature (T_{ann}), the oxide thickness, and the oxidation method, but not by the surface morphology. A transition from tunneling-dominant to pinhole-dominant transport can be induced in poly-Si passivating contacts featuring a thin oxide (1.3–1.5 nm) by increasing the annealing temperature. Interestingly, a lower thermal budget (T_{ann} = 750°C) is sufficient to induce pinhole dominant transport in samples with a 1.3 nm wet-chemical oxide, compared to those featuring a 1.5 nm thermal oxide (T_{ann} = 950°C). This result suggests that wet-chemical oxides are less resistant to thermal annealing compared to thermally grown oxides, probably due to their different stoichiometry, although the difference in thickness might have also played a role. For thicker oxides (t_{ox} = 2 nm), grown either thermally or by PEALD, higher annealing temperatures (T_{ann} = 1050°C) were required to enable pinhole-dominant transport, whereas no significant current could be detected for lower T_{ann} up to 1000°C. Overall, the dominant transport mechanisms were not affected by the substrate morphology, although, in the case of tunneling-dominant transport, a drop in ρ_c was observed on textured wafers compared to SDR and polished wafers, which in turn yielded similar ρ_c values. Further investigations are still needed to understand the impact of texturing on the oxide thickness uniformity and the formation of pinholes, which might have contributed to this difference in ρ_c. Furthermore, it was found that the ρ_c was much lower in the pinhole-dominant regime compared to the tunneling-dominant regime, which suggests that the former is the preferred charge transport mode for poly-Si passivating contacts, provided excellent passivation quality can be maintained. The results of lifetime measurements showed that an excellent passivation quality can be obtained in the pinhole regime, leading to a selectivity of S_{10} = 15 for the polished sample with a 1.5 nm thick thermal oxide annealed at 950°C. In conclusion, the results of this work indicate that the dominant transport mechanism through poly-Si passivating contacts and thus the ρ_c can be engineered by choosing the appropriate value of T_{ann} according to the oxide type and thickness.

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