Master's Thesis Engineering Technology

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Design of an integrated digital controller for a buck converer

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Problem

The CoDiCApp project aims to design a functional power converter combining all components and control logic for the converter into a single package.
A digital controller should be designed to operate with this novel power converter on a package. Fig. 1. shows the role and location of this controller in the project.

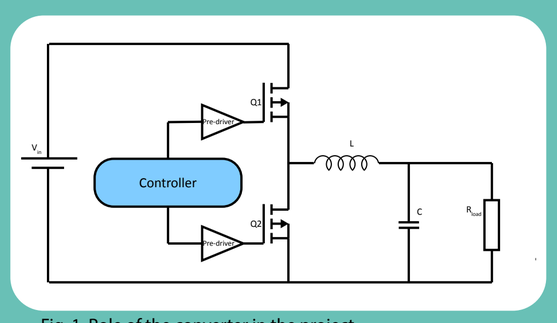

Fig. 1. Role of the converter in the project

Goals

This thesis aims to design a VHDL implementation of a control architecture that can control one or multiple buck converter designs.

This controller should be able to control the buck converter under various loads

It should use as few resources as necessary to result in a compact ASIC implementation

It should control the converter via two PWM signals with a switching frequency of 1 MHz and some dead time to ensure the two signals never overlap and both transistors are never controlled simultaneously

Method

A VHDL implementation of a PID controller with a setpoint filter and a DPWM modulator was designed to achieve the goals mentioned above. This design was then verified using MATLABs Simulink and ModelSim co-simulation.

A well-tuned PID controller allows for stabilising the output voltage for all resistance loads in the power range of 1 nW to 100 W

During the design, careful consideration was given to a resource-efficient implementation

An analysis between a sawtooth based PWM generator both with and without dithering solutions like a Σ–Δ generator was given to obtain the maximum possible output resolution given the available clock frequency and required switching frequency.

Result

The chosen design to control the buck converter can be seen in Fig 2. This design takes four voltage samples per switching period, takes the average value, and feeds this to the PID controller. This value is compared to a reference value, which runs through a setpoint filter. A fitting duty cycle is obtained and transmitted to the DPWM modulator in another clock domain through a clock-synchroniser.

The controller stabilises for the power range of 1 nW to 100 W, as can be seen in the step responses shown in Fig. 3.

The ASIC implementation of the controller in the 180 nm BCD technology from the TSMC foundry requires a total surface area of 74 727.402 µm^2 using the correct clock periods

As dithering solutions caused too many variations on the output signal, a simple sawtooth based DPWM generator was chosen. The maximum clock frequency of 444 MHz resulted in a control resolution of 0.225 V at a switching frequency of 1 MHz assuming a nominal input voltage of 100 V. The resulting steady-state signal can be seen in Fig. 4. showing the ripple of the buck converter as only oscillation

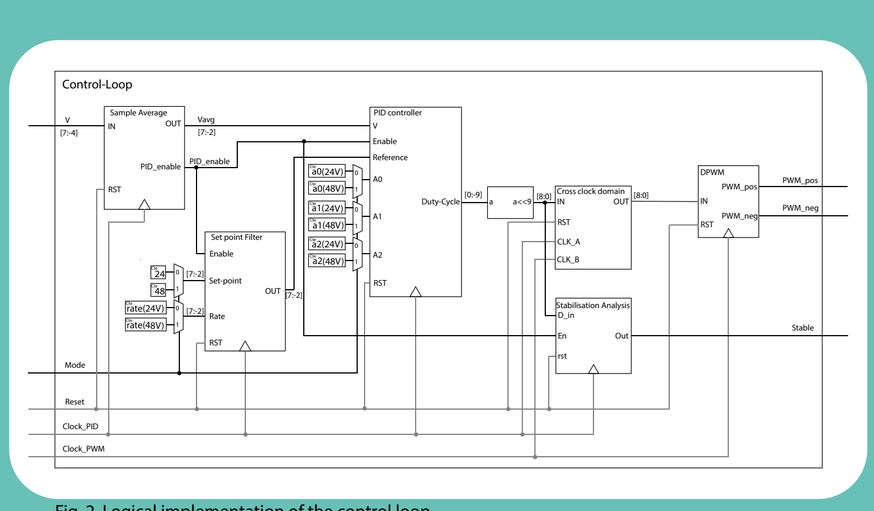

Fig. 2. Logical implementation of the control loop

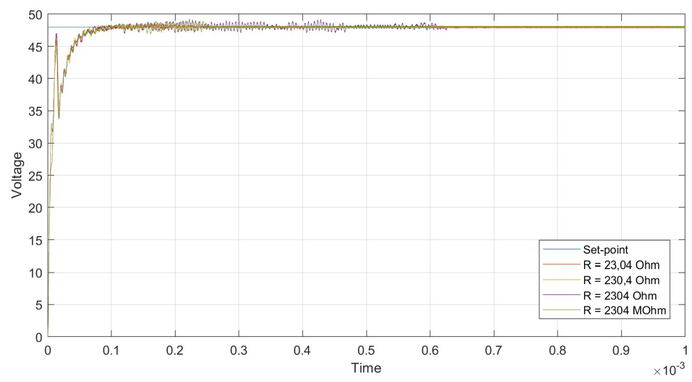

Fig. 3. Step responses of the 48 V Buck converter under various loads

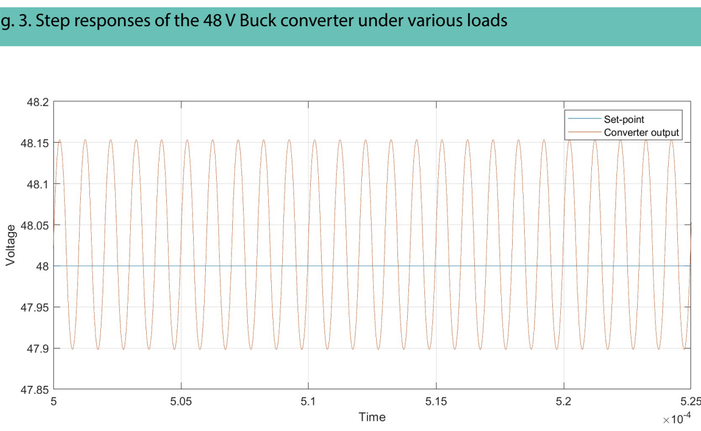

Fig. 4. Steady-state oscillation close-up of the 48 V buck converter under various loads

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