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# Dielectric Front Passivation for $Cu(In,Ga)Se_2$ Solar Cells: Status and Prospect

*Jessica de Wild,* Romain Scaffidi, Guy Brammertz, Gizem Birant, and Bart Vermang*

**$Cu(In,Ga)Se_2$ (CIGSe) solar cells are among the most efficient thin-film solar cells on lab scale. However, this thin-film technology has relatively large upscaling losses for commercial technology. To tackle this, paradigm shifts are proposed that allow for simpler, cost-effective, and efficient CIGSe solar cells. Front passivation using dielectric layers is one of the options being investigated as this is widely used in Si technology. Research on front passivation for CIGSe is in an early stage and no improvements are made yet. A close comparison with silicon technology is made to understand why it seems to be more difficult for CIGSe solar cells. In general, chemical passivation is less effective, resulting in higher interface defect densities than seen for Si. Also, field-effect passivation requires positive charges, which have not been implemented yet on the CIGSe front surface. Finally, for Si passivation, often a high-temperature annealing step is applied, which is not possible for CIGSe. It is proposed to apply a dielectric tunneling layer with positive fixed charges in combination with an electron transport layer to move forward. A list of potential dielectric layers that could be suitable for CIGSe is provided.**

## 1. Introduction

Photovoltaics (PV) is gaining increasingly more attention on renewable electricity generation. PV installations account for almost 1000 TWh electricity production, which is 3% of the total electricity generation.[1] The majority of PV is based on Si technology and about 6% is coming from thin-film technologies.[2] At this stage, the thin film is more expensive than Si technology, though it may be used for various applications, like building- or vehicle-integrated PV or semitransparent and flexible applications, and it can be lightweight. Thus, the thin film can be applied in addition to Si PV, implying that it does not have to compete with Si for land or roof availability. A high share of thin-film technology can thus be part of the renewable electricity generation. Increasing the efficiency of thin film cost-effectively remains of importance to really have a significant contribution of the thin film in the PV share. Commercially available thin-film technologies like CdTe and $Cu(In,Ga)Se_2$ (CIGSe) reached efficiencies of 21% and 23.4% for lab-scale solar cells respectively.[3,4] Perovskite (Pk) solar cells are beyond that with 25.5%.[5] Though the wet-processing approach to reach these high efficiencies makes it hard to commercialize, the more industrial viable option using sequential vacuum evaporation has reached a certified efficiency of 22.6%, thus similar to CdTe and CIGSe.[6] For flexible or semitransparent architectures, the efficiency is lower, but the multifunctionality may allow for reduced efficiencies. **Figure 1**a presents the efficiencies of the aforementioned thin-film technologies and their record efficiency for rigid, flexible, and semitransparent applications.[7–12] The values for Pk are taken from review papers and thus an average is plotted. At cell level, CIGSe is superior for rigid, flexible, and semitransparency compared to CdTe. Pk is added as emerging technology; however, commercializing is further down the road compared to CIGSe and CdTe as most of these high efficiencies are obtained on very small scale and by wet processing.[13,14] In the end, the potential for large-scale application of a PV technology is not only dependent on efficiency, but also on the use of industrial scalable techniques and therefore it is important that new concepts can be applied with industrially viable and scalable methods. Figure 1b presents efficiencies for various areas of Si and the commercial thin technologies CdTe, CIGSe, and vacuum-processed Pk.[3,6] In this case, CdTe is the superior thin-film technology as module efficiencies are the highest. Presented here are the record

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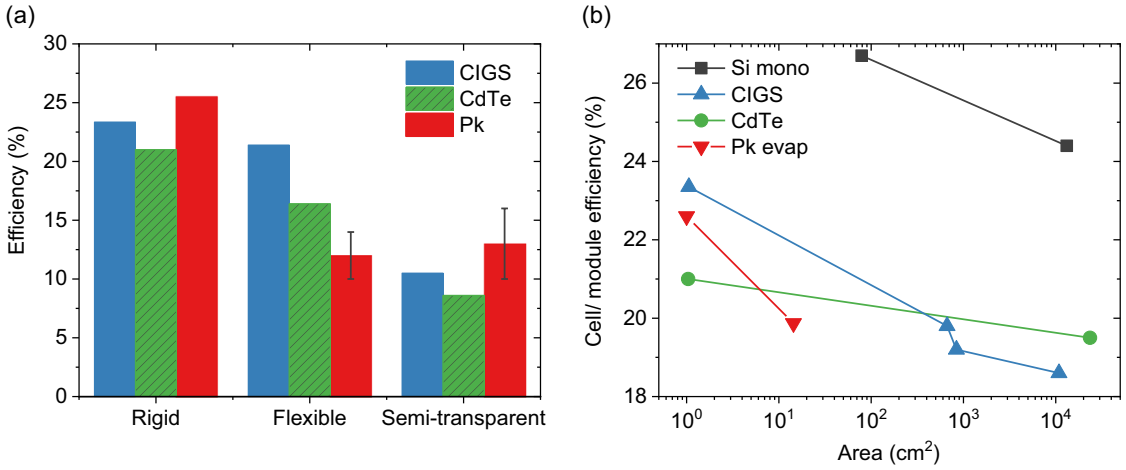


**Figure 1.** a) Record efficiencies for various commercial and emerging thin-film technologies on rigid and flexible substrates and for semitransparent architectures. b) The effect of upscaling for commercial and scalable PV technologies.

efficiencies, but in general upscaling losses are smaller for CdTe than for CIGSe. Average cell-to-module losses vary between 3% and 4% for Si, 3% and 6% for CdTe, and 4% and 8% for CIGSe.[15,16] The main reason for the higher losses for CIGSe is assumed to come from the rather complex structure of the CIGSe absorber layer, which is sensitive to lateral inhomogeneities. The CIGSe absorber layer consists of well-tuned in-depth elemental gradients to enhance the absorption in the bulk and reduce recombination at the interfaces. As these gradients are rather complex, lateral variations are easily present while the least optimal part determines the final efficiency in a module.

To tackle these limitations that seem to limit further improvements, some paradigm shifts have recently been proposed. That is, a CIGSe solar cell based on a simple absorber layer without elemental gradients, passivated/selective front and back contacts, and photon recycling.[17,18] These technologies are seen in Si PV and III/V materials, which are the most efficient PV technologies to date. Especially Si, which is the market leader in PV and thus provides industrially viable solutions, can be used as an example to improve CIGSe technology further. On top of this, to improve the efficiency further cost efficiently, it is also worth to replace the CdS buffer layer (BL) as it still contains the toxic Cd and has a low bandgap, resulting in absorption losses. In addition, it is known that thin-film solar cells suffer from dark/light crossover reducing the $V_{oc}$.[19,20] For CIGSe, this is often attributed to light-sensitive defects at the CIGSe/CdS interface and in the BL. Thus, not only would changing the CdS by a passivation layer be of interest for increased light absorption, but potentially also could reduce the $V_{oc}$ losses and be beneficial for long-term stability.

In this contribution, the option of replacing CdS by dielectric passivation layers at the front instead of high-bandgap semiconducting BLs like Zn(O,S), InSe, or MgZn(O,S) is explored. Passivation of the front interface using dielectrics is at a very early stage. Studies based on absorber/passivation structures have revealed passivating properties showing the potential of dielectric passivation of the front surface.[21–25] Though, to date no improvements in solar cells have been observed.[26–32] Often fill factor (FF) losses and problems with current extraction arise. Complications of implementing dielectric layers may be due to the roughness of the CIGSe surface, annealing steps required that are not compatible with CIGSe technology, or general incompatibility with deposition of the buffer or window layers. Examples of passivation layers applied on the front CIGSe surface will be summarized, and technical difficulties will be assessed. Finally, a way forward is proposed and the benefits for other types of CIGSe layers are discussed.

## 2. CIGSe Solar Cells

An assessment on the quality of the CIGSe absorber layer and how to improve further was done by Ochoa et al.[17] It was concluded that the quality of the absorber layer has reached the level that photon recycling could be applied, implying that the carrier lifetime is so high and overlap between emission and absorption spectra high enough that the emitted photons can be reabsorbed. Another strong conclusion was that the absorber layer is too complex and further improvements should involve a simplified absorber layer without gradients and with selective contacts.[17] The more simpler absorber layer is close to stoichiometry to reduce electrostatic losses, has large grains to reduce the density of grain boundaries of which some can be detrimental, and goes through the copper-rich step to annihilate planar defects.[33–35]

A typical state-of-the-art CIGSe solar cell is shown in **Figure 2**a. Commonly, CIGSe is grown in a substrate configuration on a Mo back contact. The two most efficient methods to grow the CIGSe layer is either selenization of the metallic stack (Cu, In, Ga) or coevaporation of the metals on heated substrate.[36] After growth of a 2–3 µm-thick CIGSe absorber layer, n-type BL is deposited. Most used technique for this is chemical bath deposition (CBD), though sputtering or atomic layer deposition (ALD) may also be used.[37,38] The top layers consist of a resistive layer (RL) and transparent contact oxide (TCO). The cells are finalized with grids. Interfaces, and especially the buffer/CIGSe interface, is optimized using various elemental gradients, which are described below.

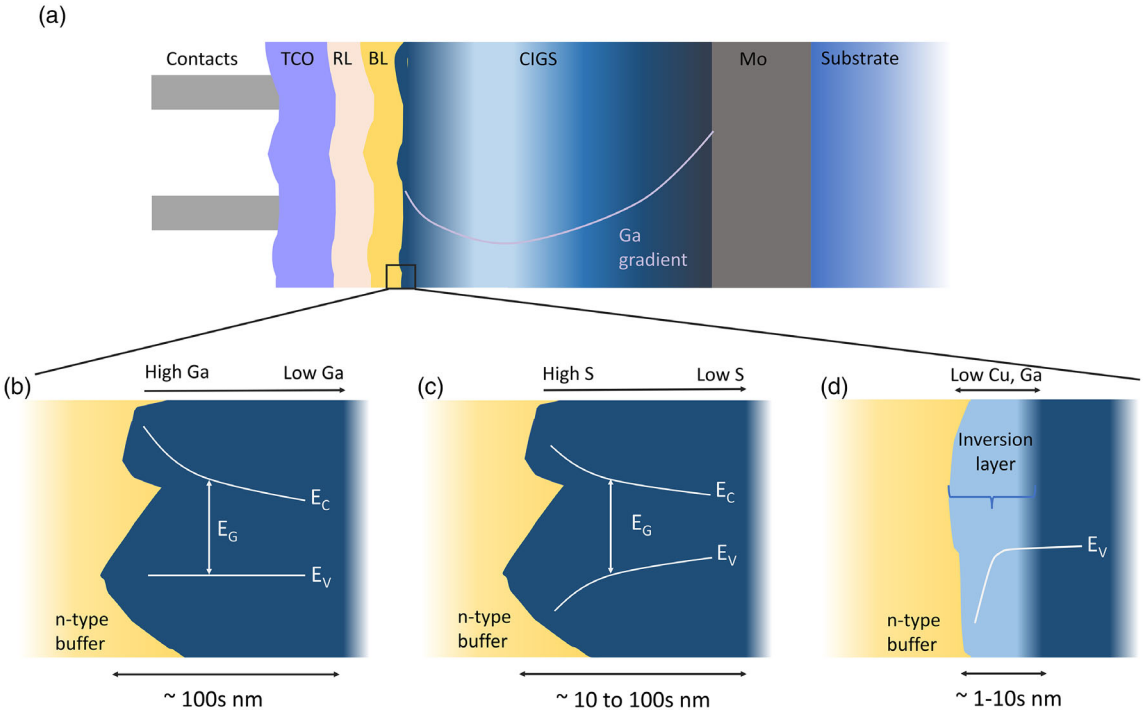


**Figure 2.** a) Typical state-of-the-art highly efficient CIGSe solar cell. BL-buffer layer; RL-resistive layer. b) Zoom-in of the CdS/CIGSe interface and effect of front Ga gradient. c) S gradients at CIGSe surface. d) Inversion layer at CIGS surface.

### 2.1. Surface Gradients

State-of-the-art CIGSe solar cells contain various in-depth gradients, which have led to high efficiencies, but also make the absorber layer very complex. This complexity of the CIGSe absorber layer makes it also harder to specify where the losses and improvements come from. For instance, the Ga gradients, standard applied in state-of-the-art CIGSe absorber layers, reduce recombination at the back, but also induce stress in the layer due to increased dislocations and reduced grain size with increasing Ga content.[39] While in general Ga gradients at the back are beneficial, it cannot be excluded that these gradients will limit the efficiency in the end. At the front also a Ga gradient may be applied, but also S and Cu gradients are implemented. These alterations of the surface and the conduction/valence band modifications are shown in Figure 2b, c and d.

#### *2.1.1. Gallium Gradient*

Increasing the amount of Ga causes a rise in the conduction band and thus widens the bandgap. At the back this is beneficial as it reduces the concentration of electrons further toward the back contact, which is the hole contact. Both commercially applied CIGSe growth processes, that is selenization of the metals or coevaporation process, have Ga gradient at the back. During selenization of the metal stack, Ga tends to stay at the back. During the three-stage coevaporation process, a Ga gradient at the front and the back arise due to the variations of the elemental fluxes during the three stages.[40] Absorber layers made with the sequential process have often no Ga gradient at the front and may be applied afterward by a postdeposition treatment.[41] The Ga gradient at the front reduces thermalization losses due to the wider gap and cause a beneficial conduction spike at the CdS/CIGSe interface.[42] A spike is beneficial for the $V_{oc}$, but when the spike is too high, it will cause a blocking effect. There is some resilience against variations in height of the spike and up to 0.4 eV is theoretically without losses.[43] The conduction band offset between CISe/CdS was experimentally determined to be 0.3 eV.[44] This offset will reduce with increasing Ga content as the conduction band goes up and even becomes negative for pure Ga.[45] A cliff will always reduce the $V_{oc}$ due to reduction of Fermi-level splitting.

As the increase of the conduction band toward the p–n junction is also a barrier for the electrons, the net effect is highly dependent on the depletion width, starting point of the incline (notch), and height of this Ga gradient.[46] The typical length scale from notch to buffer is about hundreds of nanometers, as shown in Figure 2b. This is usually within the depletion region and thus the electric field will compensate for the increase in potential the electrons have to overcome. Though, based on theoretical studies, small changes in height of the Ga gradient or the notch position can easily lead to 1% difference in efficiency.[47] Experimentally, all these variations in Ga gradient have led to variations up to 3% from cell to cell.[48] This is more than theoretical, which might be because at the back changes can occur as well. It reveals though, how difficult it is to control these Ga gradients.

#### *2.1.2. Sulfur Gradient*

Another way to get a front gradient is using sulfur. This method is often applied for sequentially grown absorber layers since the

front Ga gradient is absent. Substituting selenium by sulfur increases the bandgap due to both conduction and valence band widening. Especially the valence band widening reduces the hole concentration near the p–n junction, thereby reducing recombination. A sulfur gradient is applied on finished CIGSe samples in which sulfur is deposited on the CIGSe absorber layer during or followed by heat treatment.[49–52] The effect is different depending on the conditions and both increase and decrease in efficiencies are observed.[51,53,54] The scale of the S gradient is in the order of 10–100 nm, thus again within the depletion zone, see Figure 2c. In general, the $V_{oc}$ is improved due to the bandgap widening at the p–n junction and reduced hole concentration. However, when the elemental (S and Ga) gradients are not smooth, mainly due to the heat treatment, other parameters like FF may decrease.[51] Similar to the Ga gradient, it reveals the difficulties to control these gradients during the growth and thereby likely impacts the large-scale homogeneity.

#### 2.1.3. Surface Inversion

Finally, the CIGSe surface is adjusted by heavy alkali treatments. Alkali treatments are performed on bare CIGSe absorber layers by depositing alkali salts on the surface and an anneal. During the anneal, the alkali diffuses into the absorber layer and modifies the grain boundaries and surface. In general, the alkali treatments improve the solar cell efficiency, but sometimes with FF losses due to impaired current transport.[55–57] While the improvements are also attributed to improved absorber layer lifetime, we will only summarize the effects at the surface. Alkali treatment cause surface bandgap widening, and alkali–InSe compounds may form on the surface.[58] For KF treatment specifically, Ga and Cu depletion has been measured which is assumed to lead to an inverted surface.[59–61] Thus the hole concentration at the CIGSe surface is lower than the electron concentration and the p–n junction is shifted into the CIGSe absorber layer. The hole concentration is thus drastically reduced at the buffer/CIGSe interface and thereby the recombination. Though record efficiencies are observed using alkali treatments, problems with FF due to impaired current transport are still not completely understood.

Ga- and Cu-depleted surface may also be implemented without alkali treatments by explicitly adding a copper deficient layer.[62–64] Improvements are generally observed in $V_{oc}$ and are attributed to similar low concentration of holes near the buffer/CIGSe interface and possibly shifting the p–n junction into the CIGSe layer due to complete inversion. This inversion is usually in the first few nanometers of the CIGSe layer, as shown in Figure 2d.

### 2.2. Buffer Layers

The BL has two functions: providing the n-type layer and protecting the CIGSe surface against sputtering of the top layers. As mentioned earlier, the p–n junction may be just below the n-type BL, reducing the presence of holes near the buffer/CIGSe interface. After BL deposition, more changes occur. The most commonly used BL is CdS, with Zn(O,S) as a close follow-up. These layers are commonly deposited by CBD. During deposition, Cd/Zn species diffuse into the top surface layers of the CIGSe absorber. When Cd or Zn goes into the CIGSe lattice, they can occupy copper sites and act as donors.[65,66] Thus, the BL itself may reduce the hole concentration near the surface even further. However, copper diffuses also into the CdS layer forming CuS phases, which in turn can be harmful for the performance as CuS is p-type.[67] From a time-resolved photoluminescence (PL) study, the recombination velocity between CdS/CIGSe was determined to have an upper limit of $1.4{\cdot}10^3\,\mathrm{cm\,s^{-1}}$ without Ga gradient.[68] Theoretical predictions show that this can be reduced to $100\,\mathrm{cm\,s^{-1}}$ when Ga gradient is present.[69]

High-bandgap materials with n-type conductivity have also been applied as passivation between buffer and CIGSe absorber. In the case of the Zn(O,S) BL, a thin ZnS layer of few-nm thick improved the $V_{oc}$. It was deduced that the hydroxide in the Zn(O,S) layer causes tunneling recombination at the interface which is reduced using ALD-deposited ZnS.[70]

## 3. Front Passivation Using Dielectric Layers

The p–n junction of a typical state-of-the-art CIGSe solar cells is thus complex, with interaction between the BL and the elemental gradients at the CIGSe surface and even diffusion of elements between the two layers. These gradients change the concentration of the holes or electrons and/or increase the bandgap, all resulting in lower recombination and higher $V_{oc}$. These methods appeared to be very efficient on laboratory samples, and very high lifetimes of 400 ns have been achieved.[71,72] While effective on small scale, these gradients are hard to control and very sensitive for small variations in notch, height of the gradient, annealing conditions, and may impair the current flow and lower the FF. As it appears to be hard to upscale these methods and to obtain a large-scale homogeneous absorber layer, other concepts are being proposed that are simpler, without front gradients, and include passivation using dielectric layers.[17,18]

Passivation of interfaces and contacts is a standard concept in Si technology. Materials that are applied are oxides, nitrites, but also hydrogenated amorphous Si (a-Si:H).[73,74] In silicon heterojunctions, the p–n junctions are passivated using a-Si:H. In silicon homojunctions, the contacting layers are passivated using oxides or nitrides. In the case of CIGSe which is p-type, the p–n junction needs to be passivated. This requires that the top layers are still n-type and that the deposition of these top layers is compatible with the dielectric passivation layer. The required properties of the passivation layer will be assessed in the next section.

### 3.1. Surface Recombination Velocity and Effective Lifetime

Recombination at the interfaces or contacts is defect assisted and described by Shockley–Read–Hall (SRH) recombination and can be adapted for interfaces. The recombination rate depends on the surface carrier concentration $n_s$ and $p_s$ (in $\mathrm{cm^{-3}}$), intrinsic carrier concentration $n_i$, and the electron recombination and hole capture velocity $S_{p0}$ and $S_{n0}$ ($\mathrm{cm\,s^{-1}}$). These depend on the interface defect concentration $D_{it}$ ($\mathrm{eV^{-1}\,cm^{-2}}$) and is given by $S_{n0/p0} = \nu_{th} D_{it} \sigma_{n/p}$, with $\sigma_{n/p}$ the electron/hole capture cross

section ($cm^2$). For an interface, the recombination rate $U_s$ ($cm^{-2}\,s^{-1}$) is given by

$$U_s = \frac{n_s p_s - n_i^2}{\frac{(n_s - n_i)}{S_{p0}} + \frac{(p_s - n_i)}{S_{n0}}} \quad (1)$$

The total recombination velocity at the surface $S_{eff}$ ($cm\,s^{-1}$) is then given by $U_s/\Delta n_d$, with $\Delta n_d$ the excess minority carrier density at the surface. Reduction of the recombination rate $U_s$ can be achieved by reducing the defects ($D_{it}$) and/or the carrier concentration ($p_s$ or $n_s$) at the interface. The effect of $D_{it}$ is straightforward as the recombination velocities $S_{p0/n0}$ linearly depend on $D_{it}$. Reduction of $D_{it}$ can be achieved by chemical passivation. Reducing one of the carriers $n_s$ or $p_s$ at the interface is done by "field-effect passivation". In this case, the applied dielectric layer has a fixed charge concentration $Q_f$ that causes carriers with opposite sign to accumulate at the interface. This results into a large imbalance between the carrier concentrations $p_s/n_s$ near the surface, reducing the recombination.[75,76]

There is no simple solution for the impact of fixed charges on the surface recombination velocity $S_{eff}$. An algorithm to determine the impact of the fixed charges involves solving the surface charges at both interfaces and the corresponding electric fields.[77] An approximation in the case for very high and low fixed charges and low injection was derived by McIntosh.[78] The result of this approximation is presented in **Figure 3**a. The shaded area in the middle is the area where the approximation varies more than 10% from the more complex algorithm. What we find is that for high fixed charges, the surface recombination velocity $S_{eff}$ can reach values much lower than for chemical passivation only. It has to be mentioned that $S_{eff}$ is also dependent on the doping concentration and capture cross section and the absolute values are only representative for the assigned doping and capture cross section values. High doping mainly reduces the influence of $Q_f$ on $S_{eff}$ in the low $Q_f$ range, while $D_{it}$ is linearly related to the cross section. Examples for high doping and higher cross section are shown in the Supporting Information.

The recombination at the surface impacts the total minority carrier lifetime. The surface lifetime is given by $\tau_s = d/S_{eff}$, in which $d$ is the width of the absorber. There are more accurate descriptions taking into account the fact that carrier generation is dependent on the depth and thus diffusion of these carriers should also be taken into account.[79] This requires several assumption on the absorption, generation, and depletion as well. In here we apply the simplified equation as this will represent the trend between bulk lifetime and surface recombination well. The total lifetime is the sum of the inverse bulk lifetime and surface contribution.

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_b} + \frac{1}{\tau_s} = \frac{1}{\tau_b} + \frac{S_{eff}}{d} \quad (2)$$

In here $\tau_b$ is the bulk lifetime which is the inverse sum of the SRH lifetime and radiative lifetime ($1/\tau_b = 1/\tau_{SRH} + 1/\tau_{rad}$). The radiative lifetime is about 1.7 µs for CIGSe.[68]

In Figure 3b, a map is plotted for the effective lifetime of a CIGSe absorber layer thickness of 2 µm depending on $\tau_b$ and $S_{eff}$. The back interface was assumed to be negligible, which may be appropriate with a good Ga gradient.[68] Such a gradient reduces drastically the amount of electron toward the back and thus the recombination is really low. Highlighted is a 400 ns line, this is the highest lifetime measured on various CIGSe absorber layers to date.[71,72] In these cases, the absorber layers were treated with an alkali postdeposition treatment. Assuming that the bulk lifetime was 400 ns, the surface recombination velocity has to be about 100 $cm\,s^{-1}$ or less. From Figure 3a, we find that $S_{eff}$ values of 100 $cm\,s^{-1}$ can be achieved by reducing the $D_{it}$ to $10^{10}\,eV^{-1}\,cm^{-2}$ for low fixed charge concentration. As this is extremely low and hardly achieved on the most ideal Si interface, it is more likely that the surface inversion induced by the alkali treatment lowered the hole concentration to such an extent that the improvements come from this and not from chemical passivation.

## 4. Passivation Schemes of CIGSe

The effect of passivation can be examined prior to making a solar cell. Two methods have been used in the case of CIGSe and these are PL on absorber/oxide structures and capacitance voltage (CV)

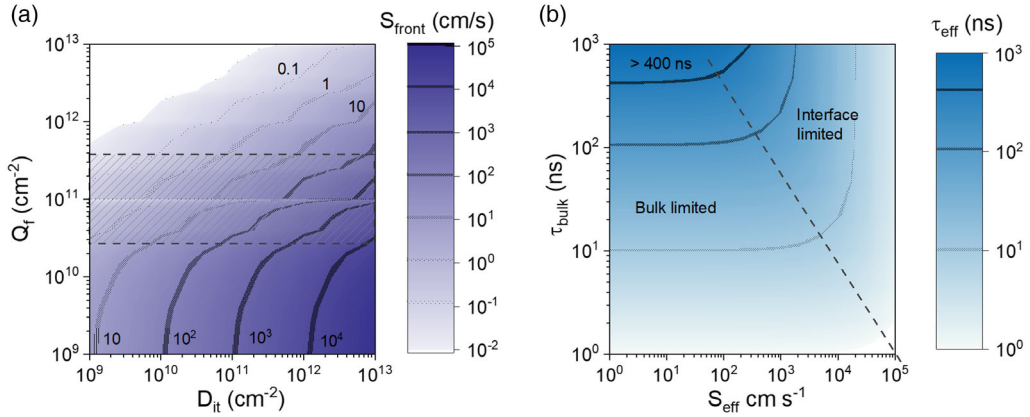


**Figure 3.** a) The effective surface recombation velocity calculated with the methods described in ref. [78] Acceptor concentration of $5.10^{15}$ $cm^{-3}$ and electron capture cross section of $10^{-15}$ $cm^2$ are used. b) The effective lifetime for a CIGSe layer of 2 µm thick using Equation (2). $S_{back}$ was assumed to be 1 $cm\,s^{-1}$. Also shown is the highest lifetime measured for CIGSe absorber layers (≈400 ns).

**Table 1.** Passivation quantification on CIGSe/oxide structures.

| Passivation layer | ALD Deposition Temperature [°C] | Thickness [nm] | Postdeposition | $Q_f$ [e cm$^{-2}$] | $D_{it}$ [eV$^{-1}$ cm$^{-2}$] | PL (intensity increase) |
|---|---|---|---|---|---|---|
| $AlO_x$[21] | 250 | 5–50 | | | | 10–200x[a] |
| $AlO_x$[23] | 300/400 | 15 | | | | 40–70x[a]<br>4x[b] |
| $AlO_x$[22] | 300 | 22.5 | – | $+(8.1–33)\times10^{11}$ | $(1.2–3.4)\times10^{12}$ | |
| $AlO_x$[22] | 300 | 22.5 | 510 °C, Se atmosphere | $-(9.4–20)\times10^{12}$ | $(8.1–15)\times10^{11}$ | |
| $AlO_x$[24] | 100 | 5 | | $-(11\pm5)\times10^{9}$ | $(1.5\pm0.4)\times10^{11}$ | |
| $AlO_x$[24] | 100 | 25 | | $-(7\pm3)\times10^{9}$ | $(3\pm3)\times10^{11}$ | |
| $AlO_x$[25] | 300 | 20 | – | $-1.4\times10^{12}$ | $(1.8–2.9)\times10^{11}$ | |
| $HfO_x$[25] | 250 | 30 | – | $-5.8\times10^{12}$ | $(5.8–7.8)\times10^{11}$ | |
| $AlO_x/HfO_x$[25] | 300/250 | 50 | | $-(2.2–2.5)\times10^{12}$ | $(2.9–8.5)\times10^{11}$ | |
| $AlO_x/HfO_x$[25] | 300/250 | 50 | 300 °C, $N_2$ | $-(1.2–1.3)\times10^{12}$ | $(2.2–5)\times10^{11}$ | |

[a]Compared to bare absorber; [b]compared to CdS, after air exposure.

measurements of metal–insulator–semiconductor (MIS) structures. The results of these studies are summarized in **Table 1**.

A first study was performed in which various thicknesses of $AlO_x$ layers were tested and PL yield was measured. The PL yield is a measure for nonradiative processes in the bulk and at the interfaces. Reducing the nonradiative channels increases the yield. In this case, it was assumed that the CIGSe absorber was the same and all changes were due to surface passivation. It was found that thicker $AlO_x$ layers led to higher PL yield. It was further deduced that the main mechanism was field-effect passivation due to negative fixed charges.[21] Another study though, showed no improvements with thicker $AlO_x$ layers and it was concluded that a subnanometer thin $AlO_x$ layer has the same passivation properties as a 20 nm-thin $AlO_x$ layer.[27] Also the stability of $AlO_x$ passivation was investigated. The PL yield was measured over time and shown to increase. It even became higher than with the CdS layer, of which the yield was stable over time.[23] In this study a CIGSe layer without Ga gradients was used.

Electrical characterization was done on MIS structures, and $D_{it}$ and $Q_f$ values have been determined. For CIGSe this has been done using $AlO_x$ and $HfO_x$ passivation layers.[22,24,25] The $D_{it}$ values determined from CV measurements were somewhere between $10^{11}$ and $10^{12}$ eV$^{-1}$ cm$^{-2}$. This is a moderate reduction of interface defects, but not enough to reduce the effective lifetime to 100 cm s$^{-1}$. This corroborates the study done by Hsu,[21] in which it was deduced that the passivation effect comes from field-effect passivation. The fixed charges were, except for one study, negative.

The $D_{it}$ values determined in these studies for $AlO_x$ are about one order higher than that of Si/$AlO_x$ for which $D_{it}$ values of $<10^{11}$ eV$^{-1}$ cm$^{-2}$ are achieved.[74] This may have to do with the way the interface is passivated. That is, at the Si surface, a thin interfacial $SiO_x$ layer is formed during deposition and the presence of hydrogen in the ALD-deposited layers passivates the dangling bonds. Also, annealing between 350 and 450 °C in an inert or forming gas needs to be done to achieve these good passivation properties. Whether hydrogen in the dielectric passivation layer has a similar effect on the CIGSe surface needs to be investigated. Some studies show that hydrogen anneal reduces the doping or even makes CIGSe n-type and creates a copper-poor surface.[80–82] This could be a beneficial effect.

### 4.1. Front Passivation of CIGSe Solar Cells

Based on CV and PL measurements of CIGSe/oxide structures, oxides provide moderate passivation properties. The applied layers were in the order of tens of nanometers thick. When applying a dielectric passivation layer in a solar cell structure, the current extraction should not be inhibited. Like Si, there are various approaches that allow for current extraction. The easiest is application of a thin passivation layer that covers the complete surface and where carriers can tunnel through. Another option is to apply a thicker layer with contact areas for carrier flow. These options are presented in **Figure 4**. For full-area passivation, the buffer and RLs can be omitted and the TCO layer can directly be deposited on the passivation layer. This is presented in Figure 4b. In the second case, the passivation layer is thicker, and openings are required. Thicker layers may have better passivation properties, as can be seen in the previous table, but come with the disadvantage that openings need to be created. To passivate the contact areas, a BL still needs to be deposited as well. This can be done over the full area or only in the openings. These schemes are predicted in Figure 4c and d. In **Table 2**, studies that investigated front passivation in CIGSe solar cells are summarized. In this table, we only added dielectric layers that are deposited on top of the CIGSe surface. Considering the multilayer structure of a thin-film solar cell, more options are possible. For instance, Keller et.al. reduced the CdS BLs thickness and used $AlO_x$ between the ZnO/CdS layer to allow for the thinner CdS layer.[83] Also, the option to use high-bandgap materials, for instance, ZnS in the case of Zn(O,S) BL, is not added here.

#### *4.1.1. Full-Area Passivation*

Ultrathin tunneling layers as passivation are also being applied in Si.[84] For tunneling, the layer can only be about 1 nm thick.

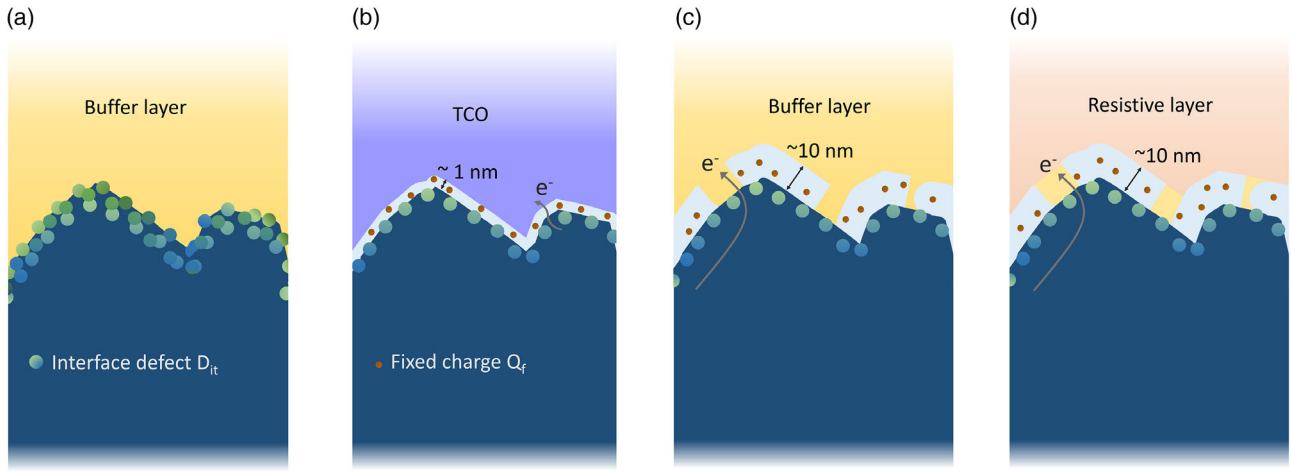


**Figure 4.** Passivation schemes for CIGSe surface. a) standard state-of-the-art buffer/CIGSe interface; b) full-area passivation using tunneling layer; c) thick passivation layer with contact openings and full coverage of BL; and d) thick passivation layer with contact openings and BL only in the openings.

**Table 2.** Implemented CIGSe surface passivation schemes. The changes in solar cell parameters are compared to reference cells from the respective paper. See text for more details.

| Passivation method | Passivation layer | Thickness [nm] | Deposition | Opening | Buffer | $V_{oc}$ | FF | $J_{sc}$ |
|---|---|---|---|---|---|---|---|---|
| Tunneling[26]a) | $Ta_2O_3$ | 2 | ALD | NA | NA | – | – | – |
| Tunneling[26]a) | $AlO_x$ | 1 | ALD | NA | NA | + | +/– | +/– |
| Tunneling[27]b) | $AlO_x$ | <1 | ALD | NA | NA | NA | NA | NA |
| a-Si[28] | a-Si | 20–60 | e-beam evaporation | NA | NA | – | – | – |
| Point contact[29] | $AlO_x$ | 5.3 | ALD | $SiO_x$ nanosphere | NA | – | – | +/– |
| Point contact[30]c) | $HfO_x$ | 10 | ALD | NaCl pattern | CdS | – | – | + |
| Point contact[31,32] | $AlO_x/HfO_x$ | 15 | ALD | NaCl pattern | CdS | + | – | – |

a)reference is without CdS; b)no reference cell was prepared; c)only cells where $HfO_2$ is deposited on the CIGSe surface.

Yousfi et al. applied $AlO_x$ and $Ta_2O_3$ as tunneling layers on CIGSe that were 1–2 nm.[26] The reference solar cell was without CdS and ZnO was directly sputtered on top of the CIGSe surface. The solar cell with $AlO_x$ had the best $V_{oc}$, while $Ta_2O_3$ had lower efficiency compared to the reference. The FF was considered to be too low though and no further investigation was performed. The high $V_{oc}$, nevertheless, showed potential to use $AlO_x$ at the front. Werner et. al. also applied $AlO_x$ at the front.[27] Comparing PL yield, it was shown that subnanometer-thick $AlO_x$ had the same yield as a 20 nm-thick $AlO_x$, implying that passivation can be achieved with ultrathin $AlO_x$ layers. Solar cell devices were prepared by sputtering an AZO layer on top, but a large extraction barrier was formed, resulting in low $V_{oc}$ and FF. This degradation was attributed to Zn diffusion into the CIGSe layer as the $AlO_x$ layer was subnanometer thick and no full coverage could be guaranteed.

One other example that can be mentioned here is the use of a-Si:H.[28] This is a semiconductor and widely used in Si as passivation layer. The advantage is that it cannot impair current flow and has low deposition temperature. Similar to dielectric oxides, it also passivates the surface of a Si wafer very well due to hydrogen termination of the dangling bonds. The conduction band offset between CIGSe/a-Si is slightly below 400 meV and thus a favorable spike can be expected.[43] In this study, a-Si was deposited by e-beam evaporation from an n-type Si wafer up to 60 nm thick. There was no mentioning of any n-type conductivity or hydrogenation of the a-Si layer. No improved parameters were observed, but it seemed to be more suitable for higher-bandgap CIGSe.[28]

#### 4.1.2. Passivation with Contact Openings

When thicker layers are applied, point contacts are required. Also, a BL is still required to "passivate" the openings. The BL can be deposited on top of the oxide or only in the contact areas, see Figure 4c and d. Few theoretical studies have been published on the effect of point contact opening, the required separation between the contacts, the area of the contacts, and effect of fixed charges for the CIGSe front contact.[85,86] The size and distribution are in the range from nenometers to submicrometers, while the field effect relaxes the requirements of the pitch width and point contact opening size.[86] When the distance between the point contacts becomes too large though, the FF will decrease as the carriers need to travel lateral, thereby increasing the series resistance.[87]

The difficulty of implementing thicker dielectric layers is making small openings with a suitable pitch and area. Few experimental studies have been performed using contact openings. A first trial was done in which $SiO_x$ nanoparticles were deposited on top of the CIGSe surface using a Langmuir–Blodgett (LB) trough, and $AlO_x$ was deposited with ALD on top of the nanospheres.[29] The $SiO_x$ nanoparticles were then removed using ultrasound sonification. Only very small openings were left, no CdS BL was applied, and ZnO was directly deposited using ALD. The solar cells improved compared to ZnO directly but not compared to the CdS reference.[88]

Another approach to make contacts in thicker dielectric layers was achieved using alkali salt patterns. This was based on the finding that when an alkali postdeposition was applied, the alkali salts form submicrometer patterns on the CIGSe surface.[89] In a first trial, CIGSe samples were merged in supersaturated alkali salts, leaving micrometer structures on the surface.[30] $HfO_x$ was then deposited on top of the salts. After ultrasound sonification and washing of the salts, the opening appeared. CdS was deposited in the contact openings by CBD. Compared to the reference, only $J_{sc}$ improved, due to thinner and localized CdS in the point contacts. It is worth mentioning here that the CIGSe absorber layers had a Ga gradient at the front which could have had impact on the fact that no $V_{oc}$ improvement was observed.[90] Also, $HfO_x$ was shown to have higher $D_{it}$ than $AlO_x$ which might also reduce the effectiveness. $HfO_x$ was used though, because this layer is resistant to the CBD of the CdS layer, while $AlO_x$ will be etched away. In another study using salt patterns, a multilayer stack was applied where $AlO_x$ was deposited on an ungraded CIGSe absorber layer for chemical passivation and $HfO_x$ on top of the $AlO_x$ to protect the $AlO_x$ against the CdS CBD. In this study, $V_{oc}$ was improved but the current extraction was impaired and FF lower likely due to the nonoptimal contact distribution in the dielectric layer stack.[31,32]

## 5. Outlook for Dielectric Front Passivation

Assuming simpler absorber layers can be made reproducibly on large scale with lifetimes of few hundreds of ns, $S_{eff}$ at the front should be about 100 cm $s^{-1}$ or less to be not limiting the effective lifetime. It implies a $D_{it}$ of $10^{10}$ $eV^{-1}$ $cm^{-2}$ when there is only a low concentration of fixed charges present. From Table 1 we found that $D_{it}$ is in the order of $10^{11}$–$10^{12}$ $eV^{-1}$ $cm^{-2}$ and thus chemical passivation itself will not be sufficient. Field-effect passivation is required to reach $S_{eff}$ of about 100 cm $s^{-1}$. To gain efficient carrier extraction, the preferred choice is to have positive fixed charges, which attract the electrons and reduce the hole concentration without impairing the electron flow.

When depositing the passivation layer, some care needs to be taken with the deposition temperature and postannealing since the CIGSe layer contains mobile ions like Na which tend to accumulate at the front surface. Usually, excess Na is washed away during the CBD, which is not possible during deposition of the oxide. Generally, when accumulation is still present, reduced FF is possible due to injection barrier.[57,91] How this would affect the performance in the case of a passivation layer is not known, but it would be beneficial if the passivation is deposited at low temperature and a postanneal can be omitted or is also at low temperature. Dielectric layers with positive charges and deposition methods compatible with CIGSe are presented in **Table 3**.

Positive charges are commonly achieved with $SiN_x$ and $SiO_x$.[74] The best layers are made using Si from the wafer while reacting with oxygen and nitrogen gasses at high temperatures. Since high temperature is generally unfavorable, low-temperature deposition methods have been developed of which plasma enhanced chemical vapor deposition (PECVD) is commercially most successful for $SiN_x$. The deposition temperature is between 300 and 500 °C and could be suitable for CIGSe. The PECVD $SiN_x$ deposited layers have intrinsically positive charges that can be controlled by the deposition parameters. Though the positive fixed charges are coming from the structural mismatch between the Si wafer and amorphous $SiN_x$ layer,[92] it is unclear how this will develop when deposited on a CIGSe surface. $SiN_x$ may also be deposited by reactive sputtering, though electrical parameters are not known as this has not been used for Si.[93,94]

As deposited $AlO_x$ can also have positive charges.[22,95] Especially the $AlO_x$ deposited at lower temperature on Si revealed very suitable properties, that is, high positive $Q_f$ of $\approx 10^{12}$ e $cm^{-2}$ and moderate $D_{it}$ of $\approx 10^{11}$ $eV^{-1}$ $cm^{-2}$. A careful calibration of $AlO_x$ deposition by ALD could thus be beneficial for CIGSe front surface passivation. $AlO_x$ is also shown to have positive fixed charges when annealed at low temperature under light.[96] The deposition was at 150 °C in this case. Recently, a combined stack of $PO_x$ and $AlO_x$ revealed very high $Q_f$ between $10^{12}$ and $10^{13}$ e $cm^{-2}$ and $D_{it}$ of $10^{10}$ $eV^{-1}$ $cm^{-2}$ for as-deposited layers.[97] $HfO_x$ is another oxide that can have positive charges depending on annealing conditions and precursors used.[98] Finally, ALD-deposited AlN is also shown to have positive fixed charges.[99] $D_{it}$ is still rather high though. Nevertheless, suitable passivation layers with positive charges that could be used on CIGSe are yet available.

The other option to consider is which passivation scheme to use. Some studies show better passivation properties with increasing thickness,[21] but difficulties arise as it also requires openings. At this stage, no feasible method has been applied to create these small openings with a suitable pitch and large FF losses have been measured. Full-area passivation has therefore more potential. These layers need to be thin enough for tunneling though. While sometimes studies show better passivation properties upon thicker layers, it is important to understand the requirements of the passivation layer. Considering $S_{eff}$ of less than 1 cm $s^{-1}$ are achieved with high fixed charges and low $D_{it}$, the requirements for CIGSe surface are less stringent due to lower bulk lifetime. In other words, $S_{eff}$ of $<100$ cm $s^{-1}$ should be sufficient to have an effective lifetime that is bulk limited. Whether this can be achieved with a tunneling layer needs to be investigated. Until now the results on tunneling layers were not very promising. Two reasons can be considered here. First, there was no focus on the presence of positive fixed charges, and they were probably negatively charged as $AlO_x$ tends to be negative. Second, standard TCO layers were deposited on top of these thin passivation layers. This was done by sputtering and it is not assessed how this may have affected the properties of the very thin passivation layers. Layers that are deposited on top of such a thin passivation likely require some sort of adaptation.

Commonly, tunneling layers are used in passivated contact structures preferably in combination with selective contacts.[84]

**Table 3.** Suitable passivation layers for CIGSe front surface (positive charge and low temperature) values for Si surface passivation.

| Passivation layer | Deposition method | Deposition temperature [°C] | $Q_f$ [e cm$^{-2}$] | $D_{it}$ [eV$^{-1}$ cm$^{-2}$] | Post-treatment |
|---|---|---|---|---|---|
| $SiN_x$[74] | PECVD | 300–500 | $\approx 10^{12}$ | $\approx 10^{11}$ | Hydrogenation during and after deposition |
| $AlO_x$[22a)] | ALD | 300 | $(8–33) \times 10^{11}$ | $(1–3) \times 10^{12}$ | As deposited |
| $AlO_x$[95] | ALD | 100 | $\approx 10^{13}/(1–6) \times 10^{12}$ | $\approx 10^{11}/ < 10^{11}$ | As deposited/5 min, 200 °C in $N_2$ |
| $AlO_x$[96] | ALD | 150 + light | $10^{12}$ | – | 1 min, 250 °C in $H_2$ |
| $PO_x/AlO_x$[97] | ALD | 25/100 | $(3–5) \times 10^{12}$ | $\approx 3 \times 10^{10}$ | 10 min, between 250 and 450 °C in $N_2$ |
| $HfO_x$[98] | ALD | 200-300 | $5 \times 10^{11}$ | $3.6 \times 10^{10}$ | 350 °C forming gas |
| AlN[99] | ALD | 200 | $2 \times 10^{12}$ | $>10^{12}$ | As deposited |

a)AlOx deposited on CIGSe layer.

For the front of a CIGSe solar cell, this is the electron contact. The use of selective contacts is very well established in Pk technology.[100] The selective contact layers are thin either have very low or very high bandgap to avoid parasitic absorption and either have high work function to have the selective carrier properties. Selective contacts without passivation have been applied in CIGSe. In this case a 15 nm $TiO_x$ was deposited with ALD on the CIGSe layer.[101] The $V_{oc}$ and $J_{sc}$ improved, but not the FF. The lower FF was attributed to increase $R_s$ and adapting deposition properties could reduce the resistance of the $TiO_x$ layer. What was notable was that over time the efficiency improved, and the FF became better than the reference with CdS. Thus, changing the BL may improve the efficiency over longer time as well.

Finally, it is worth noticing that when CdS is replaced by a passivation layer, other options open up as well. Two examples will be mentioned here. High lifetime absorbers are generally grown using a copper-rich stage during growth and have a composition just below stoichiometry.[33–35] While copper-poor absorber layer resulted in record device efficiencies, it is known that copper-rich layers have actually excellent absorber layer quality.[102] Solar cells made of these layers, however, lack behind due to deep interface defects and high recombination rate at CdS/CIGSe interface.[102] Application of a suitable passivation layer here could eliminate and/or passivate these defects and allow for inversion simultaneously. Thus, revision of stoichiometric CIGSe in combination with a suitable passivation layer could be of interest. Similar aspect is also applicable for high-bandgap CIG(S,Se). Higher-bandgap materials can be used as a top cell in tandem application or as a semitransparent device. However, the CdS BL has been shown to be unsuitable for high-bandgap CIGSe due to a cliff in the conduction band. Other BLs may be applied, like $ZnSnO_x$ or Zn(O,S).[103,104] This sensitivity on conduction band alignment with the BL though can be reduced by applying a passivation layer in combination with an electron-selective contact.

## 6. Conclusion

To have a high share of thin-film PV, specifically CIGSe-based PV, some paradigm shifts have been proposed to enhance the efficiency of CIGSe further in an industrially viable way. One of the most complex parts of the CIGSe solar cell is the front contact and p–n junction, which should be made easier without losses. For this, the option of using dielectric passivation is explored. The status of applying dielectric passivation layers at the front is assessed for various passivation schemes. To date, no improvements have been observed in solar cell devices compared to CdS. A few culprits are determined that could be responsible for the lack of improved device efficiency in the case of passivation layer application. Most notable are the lack of suitable methods to apply nanosized openings and pitch, the lack of positive charges in the passivation layer, and the less effective chemical passivation compared to silicon. Since the requirements for front passivation are less stringent for CIGSe than for Si due to lower bulk lifetime, dielectric passivation may still be beneficial when field effect is present. It is recommended to focus on full-contact passivation, in combination with a selective electron contact. Various suitable passivation layers that are compatible with CIGSe technology and have positive fixed charges have been summarized. Passivation also possibly allows for different types of absorber layers. Stoichiometric or slightly higher copper content and high-bandgap CIGSe are limited in their efficiencies when CdS is applied, which could be eliminated in the case of a suitable passivation scheme.

## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

$AlO_x$, Cu(In,Ga)$Se_2$, dielectric passivations, passivated contacts, thin-film solar cells

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