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DEPAUW, Valerie; Courtois, Guillaume; Cho, Jinyoun; Dessein, Kristof; Porret, Clement & Loo, Roger (2023) 'There and Back again': Reusable Germanium Wafers with Ge-on-Nothing Structures for Triple-Junction Solar Cells. In: 2023 IEEE 50TH PHOTOVOLTAIC SPECIALISTS CONFERENCE, PVSC, IEEE, p. 1 -3.

DOI: 10.1109/PVSC48320.2023.10359633
Handle: http://hdl.handle.net/1942/42646

‘There and Back again’: Reusable Germanium Wafers with Ge-on-Nothing Structures for Triple-Junction Solar Cells

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***Abstract* — Germanium-on-Nothing is proposed as a lift-off method to fabricate thin and lower-cost germanium templates for multijunction solar cells. This contribution presents how such foils, that are thickened epitaxially, can replace bulk wafers as III-V epitaxy seed, mechanical support, and bottom solar cell junction. Furthermore, by detaching large-area foils from reconditioned wafers, it demonstrates that the starting germanium wafer can be re-used and the recycling loop closed.**

I. Introduction

Germanium (Ge) is the major cost driver in lattice-matched multijunction solar cells [1]. It is also a scarce element, originating mostly from a single country, and is thus listed as a critical raw material [2]. Solutions to consume less, or none, are therefore of growing interest. Spalling and porous Ge are the two present solutions for thinner and kerfless Ge, both based on the lift-off of Ge films from a reusable wafer [1].

The present approach (Fig. 1) is a porous Ge approach where a regular array of macropores is formed by lithography and dry etching. With careful pattern engineering, these pores close and merge upon annealing, forming a suspended monocrystalline Ge membrane on top of one buried void, a so-called “Ge-on-nothing” (GeON) structure. This membrane can be thickened in-situ by homoepitaxy if required and, as the wafer miscut is preserved and no dislocations are induced, it can also be used as epitaxial template for III-V materials. This stack can then eventually be detached and transferred to another carrier for mechanical support. Afterwards, the Ge wafer is reconditioned and re-used to produce new foils. Contrarily to the electrochemical porous Ge route, this step results in a void- and hole-free membrane, on any wafer doping [3]. The morphology of the detachment layer can also be precisely controlled to tune the adhesion force between the wafer and the foil. All these properties have recently been demonstrated by detaching wafer-scale foils and small triple-junction solar cells [4]. Reaching a high detachment yield and a high device quality are in fact paramount to the added value of lift-off approaches. However, other factors are also essential but have not yet been addressed, namely the number of reuse cycles and the losses at wafer reconditioning.

In this contribution, we present updated technical highlights for this GeON approach and then focus on wafer reuse, demonstrating the completion of the recycling loop with a 19-cm wide foil detached from a reused substrate.

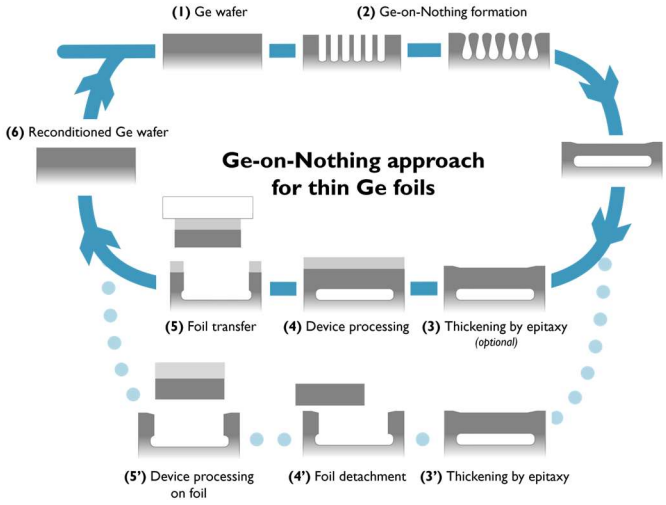

Fig. 1. GeON approach, whereby a thin Ge foil is detached from a porosified wafer that is reused multiple times. Depending on the thickness of the epitaxial Ge layer, the detached foil may require mechanical support or be processed as a wafer equivalent.

II. From a Blanket Ge Wafer to Triple-Junction Solar Cells on Tunable and Detachable Foils

In triple-junction solar cells, Ge wafers fulfill three functions, namely mechanical support, bottom junction, and heteroepitaxy seed. As recently reported and as highlighted below, GeON foils can replace Ge wafers [4].

In this approach, mechanical support is provided by the bulk Ge wafer and, after detachment, by another carrier such as the glass cover (Fig. 1 steps 3-5). Alternatively, if the foil is thickened enough via Ge epitaxy, it may be processed free-standing (steps 3’-5’). In both cases, finding the suitable foil adhesion to withstand the detachment step without cracks, and the solar cell processes without lift-off, is essential. This can be achieved by introducing irregularities in the pore pattern inducing the creation of pillars that connect the foil to its parent (Fig. 2). Their density can be defined in function of the process requirements. Fig. 2 illustrates how foils with different pillar pitches (in a range 1-400 times denser) and strengths (full or hollow) are transferred, or not, to a Gel-Pak® tape.

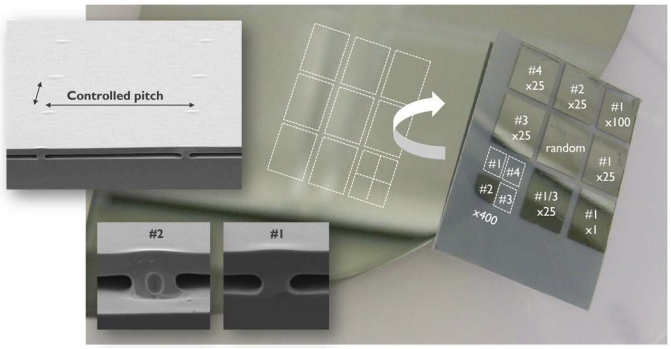

Fig. 2. Photograph of 12 GeON areas (9 mm × 9 mm) with 4 different pillar pitches and types (*e.g.*, SEM images of types #1 and #2 in lower insets), among which 9 were transferred to Gel-Pak®. The 3 areas with smallest pitch and largest pillar dimensions were too strongly attached.

The second function is that of bottom junction, which can be fulfilled by thickening and doping the membrane by homoepitaxy in-situ. By developing a dedicated atmospheric-pressure CVD process with $GeCl_4$ as precusor, growth rates up to ~190 nm/min have been achieved, with thicknesses from 1 up to 30 µm. Foils can currently be grown intrinsic (~ 1E14/cm^3) or doped with boron up to 3E19/cm^3.

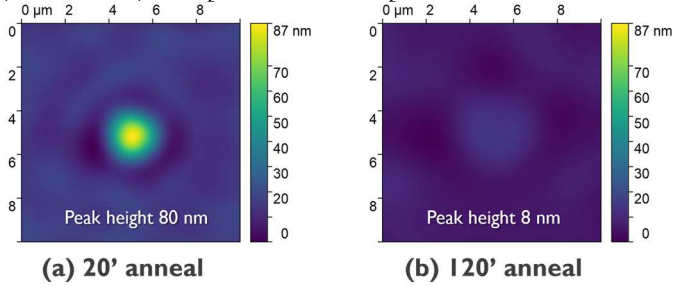

Fig. 3. 10 µm × 10 µm atomic force microscopy images plotted at the same scale in pairs, showing the reduction of (a, b) pillar bump height with increasing anneal time from 20 min to 2 h.

The last function of epitaxy seed for III-V materials is ensured by the smooth reflow of the porous surface, that preserves the crystalline quality of the parent wafer, including its miscut. This has been demonstrated by triple-junction InGaP/InGaAs/Ge solar cells grown by MOCVD on detachable 7-µm-thick GeON foils [4]. The GeON roughness is however about one order of magnitude larger than that of standard Cz Ge wafers, between 1 and 2 nm RMS. The foil surface presents a certain waviness and the additional pillars induce bumps or pits. By optimising the annealing conditions (temperature, time, atmosphere, ...), this topography may be reduced (Fig. 3). Owing to the etching properties of chlorine, epitaxial growth in $GeCl_4$ also results in significantly smoother layers (< 1 nm RMS beyond 2 µm epitaxy).

Under the surface, the foil quality was investigated by transmission electron microscopy and electron-channeling contrast imaging, by which no dislocation could be detected. Minority-carrier lifetimes confirmed the foil quality on a larger scale with 25 µs for intrinsic 16-µm-thick foils. Rutherford backscattering spectrometry channeling measurements are currently ongoing to further investigate the presence of crystal defects in the GeON seed and the epitaxial layer.

III. Parent Wafer Reconditioning

If the foil is proven to be a proper replacement for bulk wafers, it is not yet clear whether its economical and environmental added values will be sufficient. The overall Ge consumption of this approach has to be kept much lower than that of the standard bulk-wafer approach, and this directly depends on the efficiency of the reconditioning process. The GeON process steps impact the parent wafer by in-diffusing foreign species, by creating a recess at the border between GeON and bulk areas, and by roughening the surface with pillar debris. Reconditioning (step 6 in Fig. 1) hence consists in removing a thickness of Ge from the front and/or rear sides which trades-off the wafer quality and the Ge losses.

A. Contamination of the wafer rear side

The step during which contamination can take place is essentially the epitaxial deposition of the III-V layers, the only high-temperature step involving foreign elements. The front-side is not the only side at risk, since the rear side - unless capped with a protective dielectric - could also get in contact with the precursors. The steps from metallization onwards, especially if involving Au, are also a contamination source. It is yet unsure what negative impact such contaminations could have on the successive foil quality. However, beyond foil quality, the front-end-of-line semiconductor equipment required to etch the porous structure have strict restrictions on metallic elements. An investigation of their concentration and penetration depth was thus initiated.

The in-diffusion of elements involved in heteroepitaxy was monitored by secondary ion mass spectrometry (SIMS) with two different stacks, namely a nucleation stack (GaInP:Si and GaInAs grown for 35 minutes at 640°C) and a stack for forming triple-junction cells (GaInAs, GaInP, grown for 2 hours at 640°C). Profiles at the wafer rear side for the latter case with the longest thermal budget are shown in Fig. 4. As expected from theory, column-V elements, and particularly As, diffused the deepest. If all contamination was to be removed, about 2 µm Ge would have to be etched-off. A comparison with the front-side and for shorter thermal budgets will further be reported.

B. Recess from the porosified wafer rim

Essential wafer properties that must be recovered are in-plane flatness and roughness, on which the lithography quality depends. Alterations originate from pillar debris, that leave protrusions or pits of a few hundred nm in width, and from the recess at the edge between porosified and non-porosified areas. The recess of this exclusion edge is in the micron scale and depends on the pore dimension and, mostly, the Ge epitaxial layer thickness.

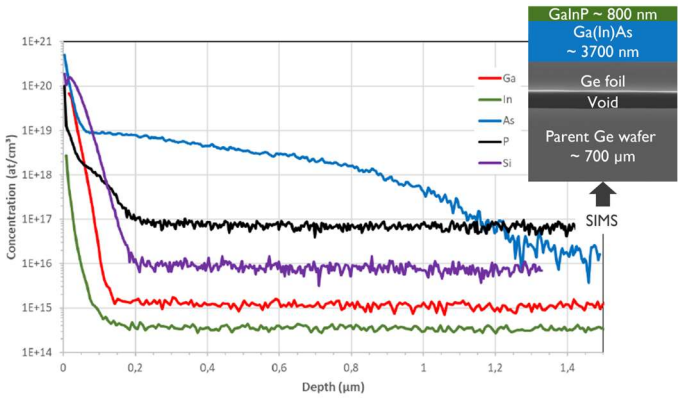

Fig. 4. SIMS profiles of Ga, In, As, P and Si measured at the rear side of the GeON parent wafer after 2 hours of MOCVD, probed until the detection limit of As was reached.

Preliminary tests were performed to identify the reconditiong route. Four 100-mm wafers on which the recess was created by masking and dry etching were used. A depth of 2.5-3 µm was targeted to mimick the depth left by a 1-µm-thickened Ge foil. The first conditioning sequence was (1) front-side grinding, (2) chemical etching for stress relief, (3) front-side polishing and (4) cleaning. The first 2 wafers followed this procedure. After grinding, the recess was successfully removed (Fig. 5). In total, this sub-optimal sequence consumed ~ 40 µm.

To minimise the losses, polishing without grinding was tested on the other 2 wafers. Despite the multiplication of passes and a total removal of ~40-50 µm, the recess could not be levelled (Fig. 5), showing that a polishing-only approach is not suitable to recover from this exclusion edge and that a dedicated approach will be needed to reduce the losses below 10 µm.

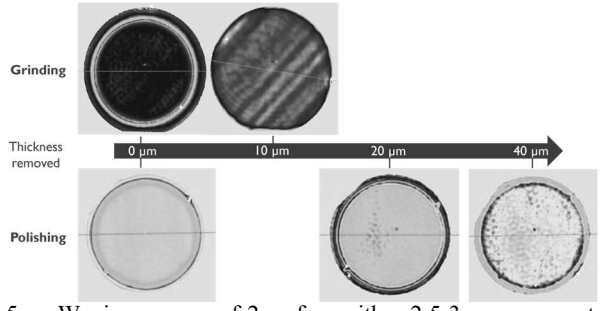

Fig. 5. Waviness maps of 2 wafers with a 2.5-3 µm recess at the edge, after grinding or polishing for different process times, with the corresponding amount of Ge removed from the front side.

C. Demonstration of wafer re-use

After these preliminary tests, four 200-mm GeON-processed wafers were reconditioned and re-processed, resulting in the first "second-generation" foils. Foils of the first generation were formed without Ge thickening or III-V growth (a limitation from wafer size), and transferred to a Gelpak® (Fig. 6a). Grinding/polishing was then applied at the front side, removing a total of 38 µm. Their contamination and roughness/flatness specifications being recovered, they were reprocessed without issue. The GeON area was printed over the full wafer, which allowed for the transfer to glass with adhesive bonding of a 12 cm × 12 cm foil and a 19-cm round foil, with a few holes at the edges caused by pattern defects (Fig. 6b) [4].

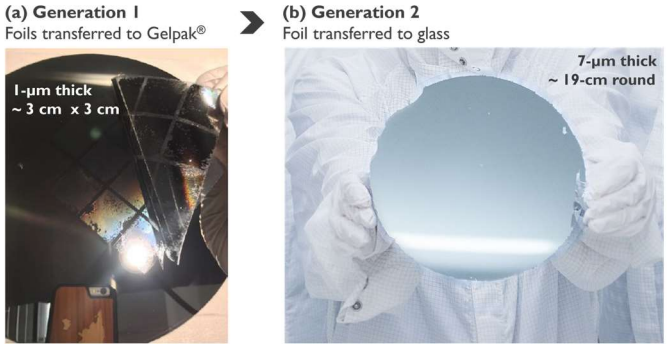

Fig. 6. (a) Twelve GeON foils being peeled off from the parent wafer and (b) one GeON foil, 19-cm in diameter, transferred from the same wafer to glass after reconditioning and reprocessing.

V. Conclusion

Ge-on-Nothing structures are proven as an efficient lift-off layer to fabricate thin Ge wafers as templates for lattice-matched III-V layer growth. With the detachment of wafer-scale foils from re-used wafers, the process loop is now closed. If the suitability of this material is demonstrated for the formation of triple junction cells, its potential for cost and Ge-consumption reductions is not yet clear. This potential will strongly depend on the number of re-use cycles that may eventually be achieved and the minimal losses of the reconditioning step.

Acknowlegments

I. García from Universidad Politécnica de Madrid is acknowledged for the III-V layer growths. This project was carried out under a program of and funded by the European Space Agency (ESA) with contract no. 4000129924/20/NL/FE. The view expressed herein can in no way be taken to reflect the official opinion of the European Space Agency.

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