PET-based perovskite solar cells to avoid potential-induced degradation

Robbe Breugelmans, Stijn Lammar, Aranzazu Aguirre, Tom Aernouts, Bart Vermang, and Michaël Daenen*

Interest in perovskite solar cells (PSCs) has grown, with advances in stability and scalability for commercialization. However, in real-world conditions, PSCs can encounter potential-induced degradation (PID), primarily due to sodium ion (Na^+) migration from conventional soda-lime glass (SLG) substrates. This study investigates whether PID can be completely avoided using Na^+-free substrates such as polyethylene terephthalate (PET). PET and SLG-based PSCs were subjected to –1000 V PID stress. The test was conducted in an inert environment to exclude other degradation factors. After 300 h, PET-based PSCs demonstrated only a 0.11% efficiency loss, staying well below the 5% stability threshold, compared to a 15% loss in SLG-based PSCs. The results confirm that using Na^+-free substrates effectively prevents PID, and that Na^+ migration is the primary cause of degradation during PID stress. These findings support further research to develop PID-resistant PSCs.

Impact statement

Potential-induced degradation (PID) is a critical challenge for perovskite solar cells (PSCs) in real-world conditions, significantly impacting their stability and posing a barrier to large-scale commercialization. This study provides evidence that PSCs can be engineered to resist PID. The findings pave the way for developing strategies to mitigate, prevent, and even eliminate PID in future PSC designs. Moreover, the study confirms that Na+ migration is the primary driver of degradation during PID stress under inert conditions, providing valuable insights that could accelerate the advancement of long-term stability solutions for PSCs, thereby expediting their commercialization.

Introduction

In recent years, interest in perovskite solar cells (PSCs) has been increasing. To commercialize this photovoltaic (PV) technology, both scalability and stability are crucial for achieving a levelized cost of electricity (LCOE) that is competitive with the current state-of-the-art PV systems.[1] Significant advancements have been made in scalability, including new records of 20.6% efficiency with an area of 215.33 cm^2, and 19.2% on an even larger area of 1027.1 cm^2.[2] However, stability remains a critical challenge as PSCs are inherently unstable and susceptible to external environmental factors such as moisture, oxygen, and heat, which can severely restrict their lifespan.[1,3–6]

Moreover, when PV modules are deployed in real-world conditions, studies have proven that they can be susceptible to additional degradation mechanisms beyond those observed in controlled laboratory environments. One such mechanism is potential-induced degradation (PID), which has been identified as a significant reliability threat and can deteriorate the power-conversion efficiency (PCE) of PSCs within a relatively short timeframe. This system-level degradation mechanism has already been extensively investigated within silicon

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photovoltaics.[7] In this context, sodium ion (Na^+) migration from the glass toward the silicon PV cell has been identified as the root cause of the degradation, and multiple mitigation, recovery, and prevention strategies have been developed.[7] However, due to the recent emergence of perovskite technology, PID has yet to be thoroughly investigated in perovskite PV.

Carolus et al.[8] conducted pioneering PID research on *n-i-p* perovskite solar cells, which degraded for 95% of their initial value after 18 h of 1000 V PID stress at 60°C, primarily due to a decrease in short-circuit current density (J_{SC}). This research clearly elucidates the severity of PID in perovskite PV systems.

Recent studies have demonstrated that elevated temperature and humidity significantly accelerate degradation during PID stress.[9,10] Analogous to PID in silicon solar cells, several characterization methods revealed that the migration of Na^+ from the glass toward the PV cell caused the degradation.[9,11–13]

Notably, these studies were conducted in ambient conditions on encapsulated devices.[8–12]

Given the sensitivity of perovskite, a new PID research method was proposed to isolate the PID mechanism by excluding influences of encapsulation and environmental stressors.[14] PID stress tests were performed on nonencapsulated devices at room temperature in an inert environment.[14]

Finally, Nakka et al.[11] introduced a first mitigation strategy by applying a nickel oxide (NiO_X) layer between the indium tin oxide (ITO) and the self-assembling monolayer (SAM). This approach significantly slows the migration of Na^+ toward the PV cell, thereby reducing degradation.

Nevertheless, significant degradation was still observed, highlighting the need for further research. The production of PSCs consists of low-temperature solution processing, which renders PSCs ideal candidates for deposition on various substrates, including poly(ethylene terephthalate) (PET) and poly(ethylene naphthalate) (PEN), which are sensitive to high processing temperatures.[15,16] Furthermore, it is hypothesized that no PID will occur when PSCs are fabricated on materials without Na^+, such as PET or PEN.

This study compares the PID susceptibility between PSCs processed on conventional soda-lime glass (SLG) and PET. Due to the absence of Na^+ in the PET, it is hypothesized that PID can be avoided. This premise is grounded in the established understanding that Na^+ migration from the substrate is the primary contributor to PID in conventional PSCs. The findings of this study have significant implications for the design and development of PID-resistant perovskite devices, addressing a critical barrier to their widespread deployment and commercialization.

Materials and methods

This study examines the differential susceptibility to PID between PET and SLG-based PSCs. All samples maintain a consistent PSC design with an identical material stack, varying only in the substrate material (i.e., SLG/ITO or PET/ITO). The devices incorporated a *p-i-n* (substrate/ITO/NiO_X/Me-4PACz/perovskite/LiF/C_{60}/BCP/Cu) architecture, using a 550-nm triple-cation perovskite absorber ($Cs_{0.05}FA_{0.85}MA_{0.10}PbI_{2.90}Br_{0.10}$). Both SLG and PET substrates were coated with a 150-nm-thick ITO layer. The SLG/ITO substrates were purchased from Colorado Concept (15 Ω/square sheet resistance), whereas the utilized PET/ITO films are Flexvue OC50 filaments sourced from Eastman Chemical Company (40–60 Ω/square sheet resistance).[17]

In order to correctly compare the results of the PID stress test, all PET and SLG devices underwent identical fabrication processes with lowered annealing temperatures compared to our previous study because PET was used.[14]

The manufacturing sequence involved radio-frequency sputtering of a 5-nm NiO_X layer instead of DC sputtering, as used in our previous work.[14] Hence, the necessity for post-sputtering annealing at 300°C was circumvented, which is required for DC sputtered NiO_X.

Afterward, a subnanometer SAM (i.e., Me-4PACz) and the perovskite solution were spin-coated using nitrogen (N_2) gas to quench the perovskite film. The electron-transport layer (ETL) was formed through subsequent evaporation of 0.8-nm lithium fluoride (LiF), 60-nm C_{60}, and a 5-nm bathocuproine bilayer (BCP). Finally, 100 nm of copper (Cu) was evaporated as rear contact.

The study encompasses 6 PET-based PSCs and 48 conventional SLG-based PSCs, each with an active area of 0.125 cm^2, all subjected to 300 h of PID stress. The entire PID stress setup was kept in an N_2 environment with oxygen and water vapor levels below 0.1 ppm and 0.5 ppm, respectively, using a custom-built setup presented in previous work.[14] PID stress was applied by connecting −1000 V to the short-circuited PSC, whereas a grounded Cu block contacted the front side, as illustrated in **Figure 1**.

Hence, all devices in this study remained unencapsulated, eliminating unwanted degradation mechanisms that could arise from suboptimal encapsulation material selection. Furthermore, given the known thermal sensitivity of PSCs, all devices were kept at ambient temperature during the experiment to isolate the effects of PID from any thermal-induced degradation processes. These experimental conditions were carefully controlled to ensure that the observed degradation could be attributed primarily to PID, enhancing the validity and specificity of this study's findings.

In order to elucidate the degradation mechanism, intermediate current density–voltage (JV) measurements were conducted within an N_2-filled glove box using a Keithley 2602A source measure unit and an Abet solar simulator. The measurements were performed on all devices under 1-sun illumination, employing a simulated 1000 W/m^2 AM 1.5 G illumination provided by a 450 W xenon lamp (Abet Sun 2000). During the JV measurements, temperature control of the devices was maintained at 30°C using a fan. The illumination intensity was calibrated using a

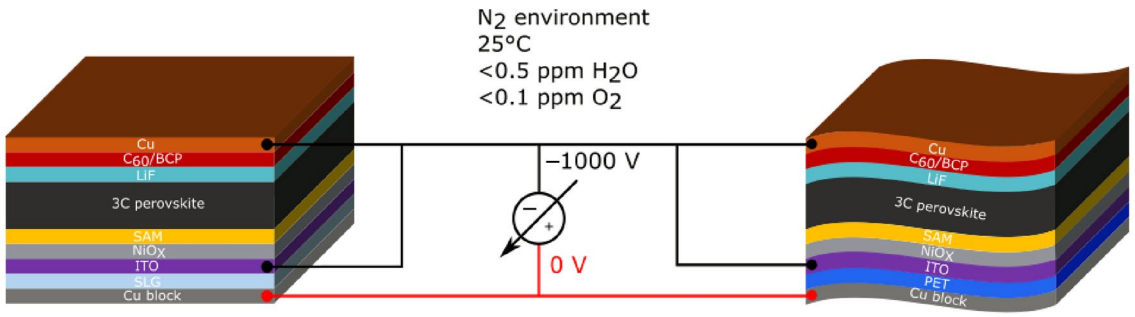

Figure 1. Schematical representation of the potential-induced degradation stress setup for a SLG and PET-based sample on the left and right sides, respectively. The Cu and ITO contacts are short-circuited and connected to −1000 V, whereas the Cu blocks contacting the SLG or PET are grounded.

WPVS reference solar cell (Type: RS-ID-4) from Fraunhofer ISE. JV weeps were executed over a voltage range of −0.2 V to 1.3 V, with a voltage step of 0.01 V and a delay time of 0.01 s (0.8 V/s).

Results and discussion

To assess the stability of PET-based PSCs under PID stress, intermediate JV measurements were performed. **Figure 2** illustrates the experimental results for PID-stressed PET and SLG-based PSCs, and presents the relative efficiency loss as a function of stress duration. The results are displayed as box plots, with SLG and PET-based samples represented in red and blue, respectively.

The SLG-based samples exhibited an average relative efficiency loss of 6.0% after 136 h of PID stress and 15% after 300 h. In contrast, the flexible PET-based PSCs demonstrated remarkable resilience, with an average efficiency loss of merely 0.05% and 0.11% after 136 h and 300 h, respectively, which is well below the 5% instability threshold.[18] Therefore, these findings highlight a substantial disparity in PID susceptibility between SLG-based and PET-based samples.

Figure 3 displays the JV curves during the stress test, allowing a closer inspection of the different JV parameters. The JV characteristics in Figure 3a reveal no significant differences over time for the PET devices as expected due to the previously presented stability. Conversely, Figure 3b, depicting the results of the SLG-based PSC, shows a more significant loss over time in J_{SC} compared to the fill factor (FF) and open-circuit voltage (V_{OC}), which is consistent with our previous study.[14]

The observable difference in FF (i.e., slope around V_{OC}) between the JV curves of the PET and SLG-based PSCs can be attributed to the higher sheet resistance of 40–60 Ω/square for the ITO layer deposited on a PET substrate, compared to the 15 Ω/square sheet resistance of the ITO on SLG substrates. However, this difference will not influence the PID stress test or the results.

Moreover, the graphs indicate that the overall efficiency of the PET-based devices is lower compared to the initial efficiency of their SLG-based counterparts. However, in potential future applications, modules will be employed that could be adapted by adjusting the P1–P1 scribe distance as a function of the conductivity of the transparent conductive oxide (TCO) to minimize resistive losses while enhancing overall device performance. Nevertheless, this optimization falls beyond the scope of the current study.

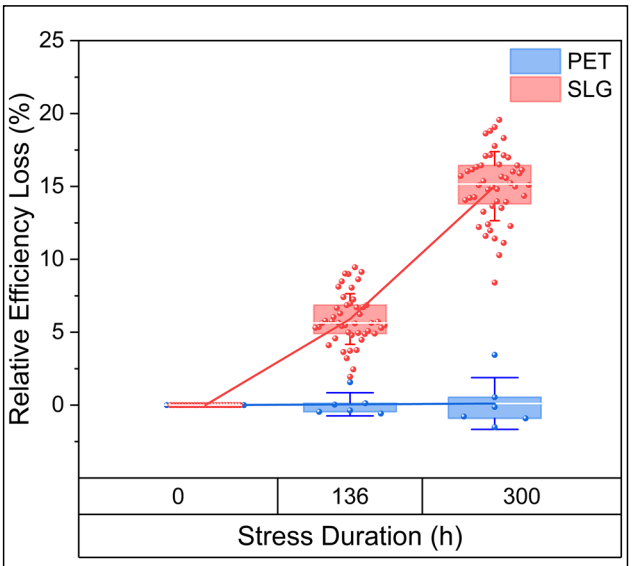

Figure 2. Red and blue box charts depicting the relative efficiency loss measured at three distinct time points (i.e., 0, 136, and 300 h) for the SLG and PET-based perovskite solar cells, respectively. The height of the charts represents the interquartile range (25% and 75% of the data), whereas the whiskers indicate one standard deviation. The means of each measurement are interconnected and additionally highlighted with a white horizontal line within each box.

Whereas Figure 3 shows the JV graphs of only one sample, **Table I** depicts the average relative losses of the entire stressed data set after 300 h of PID stress.

As was visualized by the JV graph, the J_{SC} showcased the most significant drop for SLG-based PSCs, followed by a drop in FF and V_{OC}, decreasing by 9.89%, 4.15%, and 1.63%, respectively.

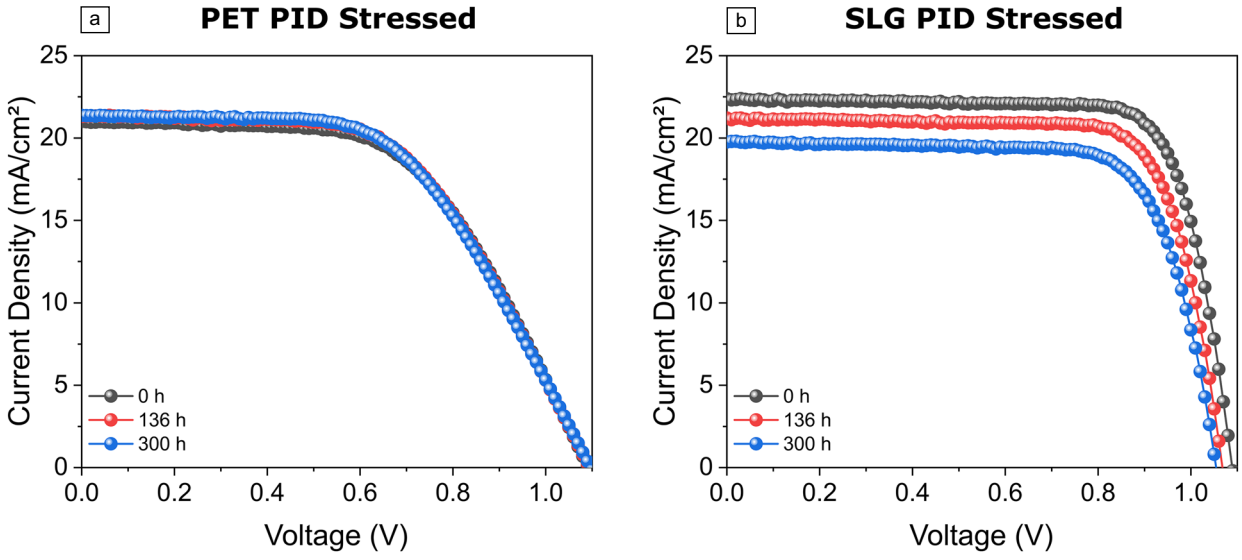

Figure 3. Light JV characteristics of (a) PET-based and (b) SLG-based perovskite solar cells measured after 0, 136, and 300 h of potential-induced degradation (PID) stress.

Table I. Summarizing table depicting the average relative losses for PCE, J_{SC}, V_{OC}, and FF after 300 h of PID stress for the PET and SLG-based substrates.

Sample Type	PCE (%)	J_{SC} (%)	V_{OC} (%)	FF (%)
PET	0.11	–0.11	–0.15	0.32
SLG	15.02	9.89	1.63	4.15

The absence of efficiency loss of the PET substrates in this study supports previous literature that suggested Na^+ migration as the main cause of PID.[9,11,12] Furthermore, due to the coherence present in the results of both groups, combined with the significant differences between PET and SLG over time, it is possible to conclude that the presented results are statistically relevant. A more detailed statistical power analysis can be found in the Supplementary information. Consequently, these results suggest that PID can be effectively avoided by accurately selecting the substrate material to minimize Na^+ content.

Conclusion and outlook

According to previous studies, PSCs are found to be susceptible to PID, even in inert conditions. It is observed that the Na^+ content in SLG substrates is the root cause of this degradation, migrating toward the solar cell under high-voltage stress. Therefore, this study investigated the use of an alternative substrate, PET, which contains no Na^+, hypothesizing that it would avoid PID.

To test this hypothesis, PET and SLG-based PSCs were subjected to PID stress for 300 h in an inert environment, minimizing the influence of additional degradation mechanisms due to environmental stressors. Intermediate JV measurements indicated an average relative efficiency loss of 15% for the SLG-based PSCs, primarily due to a decrease in J_{SC}, followed by reductions in V_{OC} and FF, confirming the results from an early PID study.[14] In contrast, the PET-based devices exhibited an average efficiency loss of only 0.11% after 300 h, well below the instability threshold of 5 percent.[18]

Consequently, it can be concluded that in the absence of Na^+ in the substrate material, PSCs do not degrade during PID stress. Moreover, this study confirms that in controlled environments where external stressors are minimized, the migration of Na^+ emerges as the primary driver of the PID mechanism in perovskite solar cells. These results provide evidence for the superior PID resistance of PET-based PSCs compared to their SLG counterparts, suggesting significant implications for the development of stable perovskite photovoltaic devices.

In addition, these results contribute to a deeper understanding of the physics underlying PID in perovskite devices, facilitating the development of effective mitigation and prevention strategies. Given that no PID was observed in perovskite devices using a Na^+-free substrate, future PID stress tests could focus on perovskite devices built on sodium-containing glass types with lower Na^+ concentrations compared to SLG, such as borosilicate glass (which contains 5 wt% Na compared to 15 wt% in SLG).[19]

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Author contributions

Conceptualization: all authors; Methodology: R.B., S.L., A.A.; Material preparation: R.B., S.L., A.A.; Data analysis: R.B., S.L.; Writing—original draft preparation: R.B.; Writing—review and editing: S.L., A.A., T.A., B.V., M.D.; Funding acquisition: R.B.; Resources: T.A., B.V., M.D.; Supervision: B.V., M.D.

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Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Conflict of interest

On behalf of all authors, the corresponding author states that there is no conflict of interest.

Supplementary information

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