Investigation of Recombination Mechanisms in Electronic Devices Using Bias-dependent Admittance Spectroscopy Applied to CIGS Solar Cells

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Investigation of recombination mechanisms in electronic devices using bias-dependent admittance spectroscopy applied to CIGS solar cells.

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- Admittance spectroscopy
- Defect characterization
- Interface recombination
- Capacitance measurements
- Thin-film photovoltaics
- CVf loss map

Abstract
The main cause for the power conversion efficiency limitations in $Cu(In,Ga)(S,Se)_2$ (CIGS) solar cells is still heavily debated in literature. Possible culprits for the limitation of the open circuit voltage of CIGS devices are conduction barriers, recombination in the bulk of the absorber, at grain boundaries, at the back contact or at the interface between the p-type absorber and the n-type buffer layer. In the present work we perform a large amount of bias-dependent admittance spectroscopy measurements on CIGS solar cells. We represent the data using CVf loss maps, comparing the measurement results to simulations, allowing us to draw conclusions about the recombination processes observed in the devices. Analysing a range of devices consisting of state-of-the-art absorber layers with varying buffer layers and power conversion efficiencies, we could draw conclusions on the presence of an interface defect at the absorber-buffer interface. In fact, all devices, independent of power conversion efficiency, showed the presence of an admittance trace

that could be related to a defect at the CIGS-buffer interface. A correlation could be found between the bias voltage position of the admittance trace with the open circuit voltage of the devices, indicating that the defect is limiting the photocurrent and open circuit voltage. A digital twin model involving only an interface defect at the CIGS-buffer interface was able to reproduce current voltage and admittance measurements of the best performing cell, proving the viability of the findings. We conclude that future improvements to the power conversion efficiency of these CIGS solar cells must come from interface engineering at the CIGS-buffer interface. Variations in doping of the absorber and buffer layer, the nature of the interface and buffer layer as well as the number of fixed charges at the interface all have the potential to drastically influence the significance and bias range of the interface recombination.

I. Introduction

Admittance (or impedance) spectroscopy is a technique that is extensively performed on all sorts of electronic systems to measure charge loss mechanisms that degrade the device performance. Notably in complementary metal-oxide-semiconductor (CMOS) transistors, admittance spectroscopy has helped identifying the major defects at the silicon oxide interface, which is at the heart of the devices. Successful measurement of the defect densities in these devices helped modifying the systems in such a way that performance could always be further improved to present standards [1-4]. Also, in other fields involving electron and hole currents, admittance or impedance spectroscopy can help identify charge loss phenomena. Other systems, where admittance measurements are routinely performed, are microelectronic sensor devices, photonic devices, capacitors, batteries, electrochemical cells, biosensors and solar cells, amongst others [5-10]. In this contribution, we will apply admittance spectroscopy to the case study of $Cu(In,Ga)(S,Se)_2$ (CIGS) solar cells.

CIGS solar cells have gathered significant attention as high efficiency thin film photovoltaic devices due to their excellent absorption characteristics and thin film nature which allow for extreme lightweight and also flexible applications[11,12]. Over the past decade, advancements in material quality, device architecture and fabrication processes have led to ever increasing record efficiencies [13-15]. Despite these achievements, further optimization of CIGS-based devices requires a deeper understanding of the underlying electronic properties and further insights into which recombination processes are limiting the open circuit voltage (V_{oc}) and power conversion efficiency. Possible culprits for the limitation of the open circuit voltage of CIGS devices are conduction barriers, recombination in the bulk of the absorber, at grain boundaries, at the back contact or at the interface between the p-type absorber and the n-type buffer layer. Admittance spectroscopy has already been widely used to identify recombination processes in CIGS solar cells with very convincing, but sometimes also controversial or opposing results[16-27]. In particular, the complex variation of admittance data with frequency, temperature and applied bias voltage is not trivial to interpret conclusively. In this contribution we use a novel method based on a graphical representation of the frequency and bias voltage dependent admittance data, in combination with advanced drift-diffusion simulations of the measured structures to gain insight into the main recombination processes in state of the-art CIGS devices.

II. Methods and Materials

a. Device structure and fabrication

The devices measured in this work have the general structure of state-of-the-art CIGS solar cells consisting of a substrate/back contact/p-type absorber/n^+-type buffer layer/transparent top contact stack[28-30]. Figure 1 shows a schematic representation of this stack together with a schematic representation of the measurement setup.

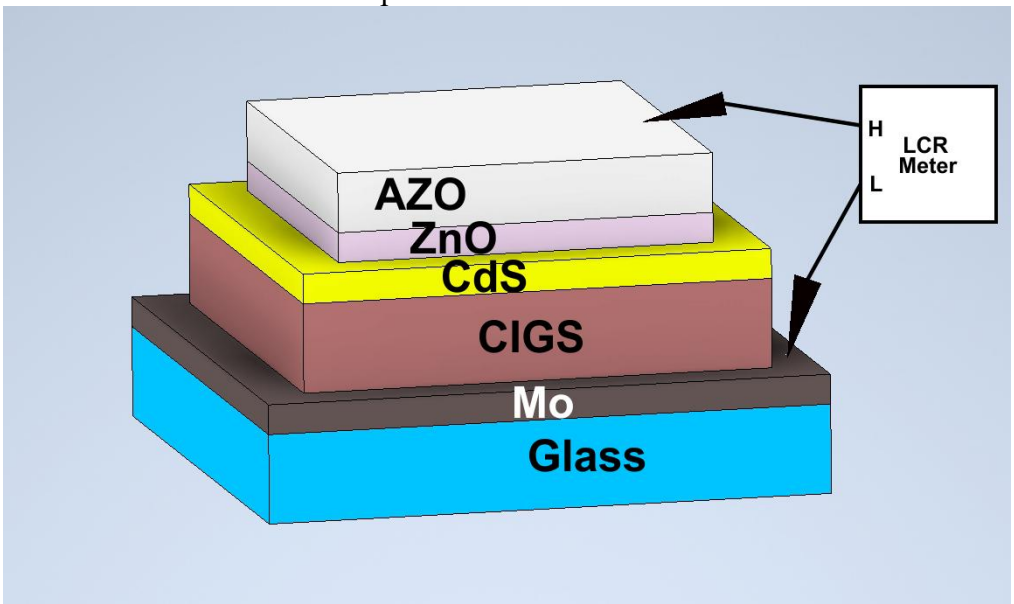

Figure 1. Schematic representation of the CIGS device structure and the measurement setup.

The substrate of our devices is a 3 mm thick soda lime glass substrate. The back contact is a sputtered Mo layer with a thickness of about 500 nm. In this work, two different types of CIGS absorber layers were used. The first type of CIGS absorber layer was fabricated in the labs of imec and TNO, whereas the second type of absorber layer was fabricated at Avancis. The fabrication procedure at Avancis can be found in reference 15. The fabrication procedure of the imec/TNO absorbers consists of sputtering an 800 nm thick, ten times multi-stack of $Cu_{0.75}Ga_{0.25}$/In metal layers, followed by the deposition of a two micrometer thick Se layer. This stack is then introduced in a rapid thermal anneal oven where it is annealed at a temperature of about 540°C in the presence of N_2 and H_2S for about 20 minutes to form the CIGS grains of the absorber. All absorbers in this work are state of the art CIGS absorbers which are Cu-poor, with a Cu/(Ga+In) value of about 0.9 and present an optimal amount of Gallium with a Ga/(Ga+In) value of around 0.2 to 0.3. This is the composition range where the CIGS devices with the highest power conversion efficiencies can be fabricated [31-33]. After absorber deposition, the n^+ buffer layer is deposited. Also here, different deposition methods have been utilized. In total, four different types of buffer layers have been used. The first type of buffer is a thin 50 nm thick CdS layer deposited by chemical bath deposition (CBD). A description of the deposition process can be found in references [34-36]. The second type of buffer layer is a thin 20 nm layer of ZnS deposited by ionic layer deposition [37,38]. The third type of buffer layer is a thin 20 nm SnO_2 layer deposited by atomic layer deposition [39,40]. The fourth type of buffer layer is a thin layer of ZnOS deposited by sputtering [15]. Finally, the transparent top contact consists of a 50 nm thick undoped ZnO layer followed by a highly n-type doped transparent

conductive oxide (TCO) such as aluminium-doped ZnO (AZO) or In-doped SnO_2 (ITO). The individual cells are laterally limited by mechanical scribing. The devices are measured by respectively contacting the back Mo contact and the top TCO contact with a needle.
In this work a total of ten different devices were measured, which came in three different groups. The first group of devices consists of six imec fabricated CIGS absorber layers with CdS CBD-deposited buffer layer (samples A1 to A5) and a ZnS buffer layer (sample A6). The second group of devices consists of three Avancis CIGS absorbers with a CdS buffer layer deposited by CBD (B1), a CBD CdS layer with an atomic layer deposition (ALD) SnO_2 layer deposited on top (B2) and with an ALD SnO_2 layer deposited directly on top of the CIGS absorber layer (B3). Finally, the third set of devices consists of one single device that was fully fabricated at Avancis and that consists of an Avancis CIGS absorber with an Avancis deposited Zn(O,S) buffer layer (C1).
Table 1 summarizes the properties of the ten devices which will be discussed in the following. For every device the electrical properties of the solar cells, such as device conversion efficiency η, open circuit voltage V_{oc}, short circuit current J_{sc} and fill factor FF are shown. The device conversion efficiencies span a wide range, from very low efficiencies to efficiencies as high as 17.6% for the Avancis device (C1), allowing for a broad analysis of possible mechanisms limiting the performance of the devices.

Sample name	Absorber	Buffer	η (%)	V_{oc} (mV)	J_{sc} (mA/cm2)	FF (%)
A1	Imec CIGS	CdS	12.7	641	27.5	71.7
A2	Imec CIGS	CdS	15.3	634	36.3	66.5
A3	Imec CIGS	CdS	14.1	609	34.4	67.5
A4	Imec CIGS	CdS	13	550	37.3	63.3
A5	Imec CIGS	CdS	9.9	603	30.5	53.8
A6	Imec CIGS	ZnS	0.3	151	8.9	25.4
B1	Avancis CIGS	CdS	11.5	618	33.6	55.5
B2	Avancis CIGS	CdS + SnO_2	12.8	608	32.2	65.5
B3	Avancis CIGS	SnO_2	4.8	305	31.4	50.7
C1	Avancis CIGS	ZnOS	17.6	677	37.2	69.9

Table 1. Device properties of the different samples analyzed for this work. Three large groups of devices have been processed. Samples A consist of imec-made CIGS absorbers with imec buffer layers. Samples B consist of Avancis made CIGS absorbers with imec- or UGent-made buffer layers and samples C consist of Avancis-made CIGS absorber layers and buffer layers.

b. Measurement and simulation methodology

The general principle behind admittance spectroscopy measurements is that the electronic device is put in a certain energetic state by applying a DC bias voltage, on top of which is then applied a small (infinitesimal) sinusoidal AC voltage with a frequency f. As a response to this DC bias and AC excitation, the resulting current through the device is then measured. The amplitude and the delay of the current response with respect to the AC voltage then allows the extraction of the complex admittance Y or impedance Z of the full device that is probed. The complex admittance Y just being the inverse of the impedance Z = 1/Y, so both terms are totally equivalent and can be derived from each other. In our measurements, the applied DC bias and the measurement frequency f are varied in small steps in wide ranges, to put the electronic device in a wide variety of energetic states, which allows to analyse the variation of the complex admittance response with bias voltage and with measurement frequency, giving as much information as possible about the response of the device.

The particularity of electronic defect states in the band gap of semiconductor devices is that they behave like small parallel RC circuits and respond mainly at a particular frequency $f_r = 1/2\pi RC$. Using Shockley-Read-Hall statistics, this response frequency f_r of electronic defect states in the band gap of a semiconductor can be calculated as [41-43]:

$$f_r = \frac{v_t \sigma N}{2\pi} \exp\left(-\frac{E_a}{kT}\right) = \frac{\gamma \sigma T^2}{2\pi} \exp\left(-\frac{E_a}{kT}\right), \quad (1)$$

Where E_a is the activation energy of the defect, k is the Boltzmann constant, T is the temperature, v_t is the average thermal velocity of the charge carrier, N is the effective density of states in the band, σ is the capture cross section of the defect and γ is a parameter comprising the temperature independent terms of the thermal velocity and the effective density of states, assuming that the thermal velocity has a $T^{1/2}$ temperature dependency and N has a $T^{3/2}$ temperature dependency. The activation energy of the defect E_a is related to the energy difference between the defect state energy in the band gap and the lowest possible band energy with which the defect exchanges charges.

As a consequence, varying the measurement frequency allows the separation of defects with different activation energies, as the system goes through a state difference when the frequency is respectively below or above the response frequency of the defect. Scanning the measurement frequency will therefore allow the separation of different defect responses and will yield information about the defect structure in the device. Only if the defect response frequency f_r is close to the measurement frequency f, an AC current will be measured in phase with the AC bias voltage, as the defect will then charge and discharge at the same frequency as the measured device. Very shallow defects with low activation energies below 100 meV will typically have very fast frequencies in excess of 1 MHz, making them difficult to impossible to measure at room temperature with standard inductance, capacitance and resistance (LCR) meters. Very deep defects with activation energies in excess of 0.6 eV will typically have very slow response frequencies of the order of several seconds or more, which make them also difficult to measure with standard equipment. They will generally show up in the measurements more like a hysteresis in the bias response. Changing the measurement temperature nevertheless allows deeper defects to be measured as well by raising the measurement temperature, or shallower defects to be measured by reducing the temperature [44].

Another pre-requisite for measuring a defect response is that the energy of the Fermi level, fixed by the DC bias voltage in the device, is within a few kT/q of the energy level of the defect, k being the Boltzmann constant and q the electron charge. Only if that is the case, the defect level will capture and emit a charge in phase with the AC measurement signal and yield an AC current, as

the Fermi level is then constantly filling and emptying the trap state. The value of the DC bias voltage is therefore also an important handle, as it defines the position of the Fermi level in the device. Only for very specific values of the DC bias voltage, the Fermi level in the device will be close to the defect level and will give rise to an AC current which is measurable. If none of the available bias voltages brings the Fermi level close to the defect energy, the defect will not be measurable.

Both frequency and bias voltage are therefore important handles to access all the different defect levels in the devices. In our measurements, we use an Agilent Precision LCR meter which is equipped with a DC bias option. We generally measure the CIGS solar cell devices with a 30 mV AC bias voltage and varying the DC bias voltage in 41 steps from -1 Volt to +1 Volt and by varying the measurement frequency logarithmically in 41 steps from 100 Hz to 1 MHz. This gives us a large continuous measurement space which allows us to derive the voltage- and frequency-dependencies of the measured responses of the device to the AC bias perturbation. All measurements were performed in the dark on devices that were only very shortly illuminated with an AM1.5G light spectrum. Metastable effects have not been considered in this work. We generally apply a potential on the Mo back electrode, keeping the top TCO contact grounded, such that the positive voltage range corresponds to the forward bias of the junction.

Because our p-n junction solar cell device in the dark below the threshold voltage is to first order a capacitance with shunt and series resistance, we generally express the output of the LCR meter in terms of conductance and capacitance. The complex admittance Y of a capacitor C in parallel with a conductance G, where G is 1/R, R being the resistance, is:

$$Y = G + j\omega C \ . \qquad (2)$$

The values G and C are then the outputs of the LCR meter and are being measured as a function of the 41 bias voltages and the 41 measurement frequencies that we use. It is important to understand that both G and C contain the defect information, as the defect charging and discharging gives both rise to a conductance response in phase with the AC excitation corresponding to the displacement of carriers and a capacitance response in quadrature with the AC sine wave corresponding to the varying level of fixed charge in the defect state. For metal-oxide-semiconductor (MOS) devices, where the DC current of the devices is strongly limited by the gate oxide, the conductance is used to analyse the defects [1,4]. In the case of the solar cell, which is mainly a p-n diode, the currents can be quite large, especially in the forward bias direction, such that the analysis of the capacitance is preferred, because there will be a large background of DC conductance in the conductance data which might hide any possible defect data. This DC response is omitted when analysing the capacitance. Walter et al. [45] analytically demonstrated that in a thin film p-n^+ type of solar cell, the trap density is to first order proportional to -fdC/df, which is why we predominantly use this figure of merit to analyse the cell properties in the following part of the work. In addition, to get an easy accessible understanding of the different bias voltage and frequency dependencies, we plot the measurement data as a two dimensional heat map of -fdC/df, where the vertical axis is the logarithm of the measurement frequency, related to the activation energy of the response, and the horizontal axis is the applied DC bias voltage, related to the variation of the Fermi level energy in the device. The heat map data is -fdC/df expressed in nF per cm^2 of cell area. This type of figure will be exclusively used in the following to analyse our measurement results and will be called a CVf loss map.

As the bias voltage and frequency dependencies of the figure of merit -fdC/df are usually complicated and non-intuitive, we have employed device simulation with a drift-diffusion simulator [46-48] to fabricate example cases for different type of possible non-idealities in CIGS solar cells. The exact procedure of how these simulations were performed and the detailed results can be

found in [49]. Figure 2 shows a summary of the main simulation results, showing from top to bottom simulations for a CIGS cell with (a) series resistance, (b) a bulk defect in the absorber, (c) a potential barrier in the CIGS-buffer conduction band energy, (d) a potential barrier in the CIGS/back contact valence band energy and (e) an interface defect located at the CIGS – buffer interface.

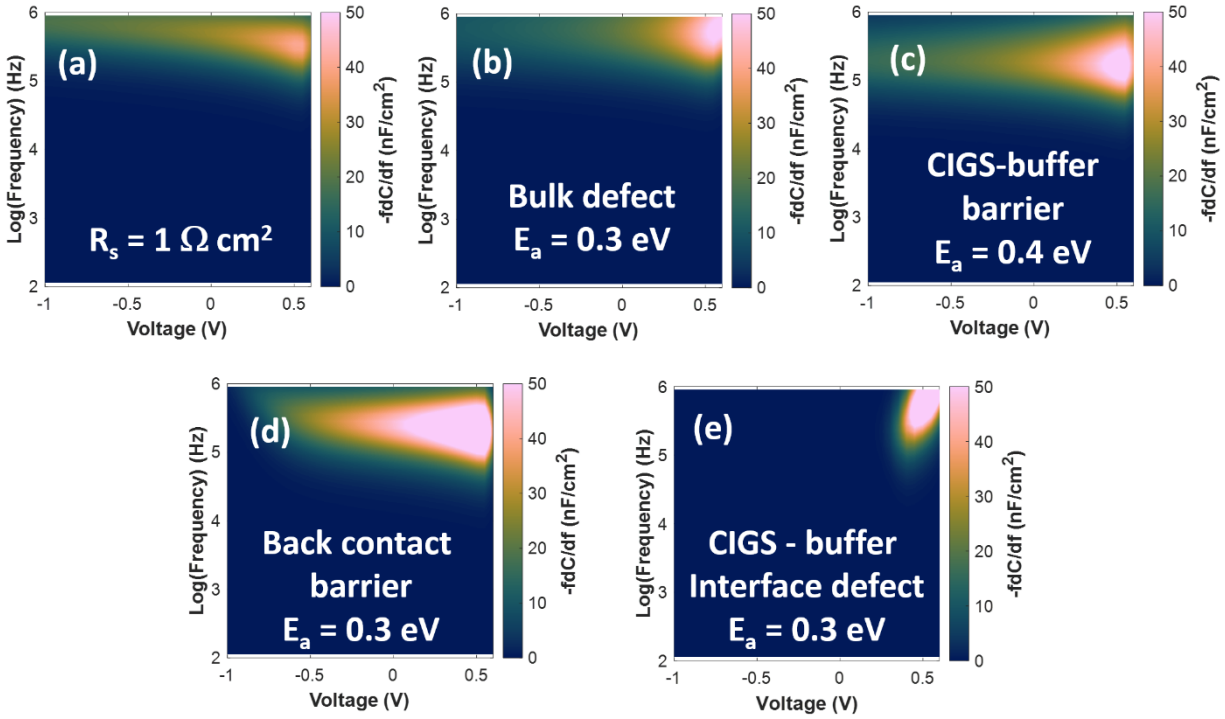

Figure 2. SCAPS simulation results of different defect types: **(a)** series resistance, **(b)** bulk defect in the CIGS, **(c)** potential barrier at the CIGS-buffer interface, **(d)** potential barrier at the back-contact CIGS interface, **(e)** interface defect at the CIGS-buffer interface.

At this point it is important to note that it is visible in figure 2 that series resistance, bulk defects and potential barriers have traces in the CVf loss map that are relatively similar, with a large tail of the response that extends all the way in to the negative bias range and depends a lot on the depletion layer width, therefore depends strongly on the doping in both the absorber and the buffer layer. The trace of interface defects is very different from the four previously mentioned cases though, as the bias extent of the trace for interface defects is much smaller. The reason for this being that the interface defects are on the one hand physically localized at a single location, the absorber-buffer interface, and on the other hand are usually also limited in the energy space in the band gap. Interface defects are generally distributed as gaussian distributions centred around a particular energy, that can be located either completely in the band gap of the semiconductor or also located in one of the bands, with only tails of the distribution extending into the band gap. This has for example been shown in much detail for Si, GaAs, InGaAs and InP interface defects [50-57] Therefore, when varying the DC bias voltage of the device, the Fermi level at the interface can move quite rapidly over the interface defect energy, leaving behind a very localized trace in the bias voltage range in the CVf loss map. This observation will have implications on the reasoning made in the results and discussion section. One notable exception to this rule is when the interface state density is so high that it leads to Fermi level pinning, in which case the movement of the

Fermi level is hindered at the defect energy location and the interface defect trace also extends into reverse bias. This particular case has not been observed though in the experimental studies done on CIGS devices that will be presented in the next section.
Even though these simulations were performed for CIGS-type solar cells, we can assume that they qualitatively are also valid for other type of p-n^+ solar cells. For studying devices that are not to first order p-n^+ junctions, simulations should be made which consider the device structure and possible defect types in those structures. In perovskite devices, for example, the intrinsic nature of the absorber and ion migration should also be taken into consideration. In photoelectrochemical (PEC) cells on the other hand, the charge transfer from the semiconductor to the electrolyte as well as the electrolyte diffusion will also need to be modelled to get the full functionality of the device. These other types of devices will not be covered in this work, but the general methodology of simulating CVf loss maps and comparing to experimental measurements could also be applied in those cases.

III. Results and discussion

On all ten devices admittance spectroscopy measurements were performed as a function of DC bias voltage and measurement frequency. As already mentioned in the previous section, we measure the admittance of the device for 41 different bias voltages ranging from -1 to +1 Volt and for 41 measurement frequencies ranging logarithmically from 100 Hz to 1 MHz. From the measured capacitance of the device, we then calculate -fdC/df and plot the result on a 2-dimensional heat map where the vertical axis is the logarithm of the measurement frequency, and the horizontal axis is the bias voltage. We call this heat map the CVf loss map, as a response in this map generally is related to an energy loss event and can be related to some sort of non-ideality in the device. An ideal device would show a perfectly blue shape, corresponding to no-signal, i.e. no capacitance variation with frequency. The brighter coloured areas are areas where we can measure a capacitance variation and therefore a response in the -fdC/df value, corresponding to different non-idealities. Figure 3 shows the room temperature measurement results of the six different type A devices.

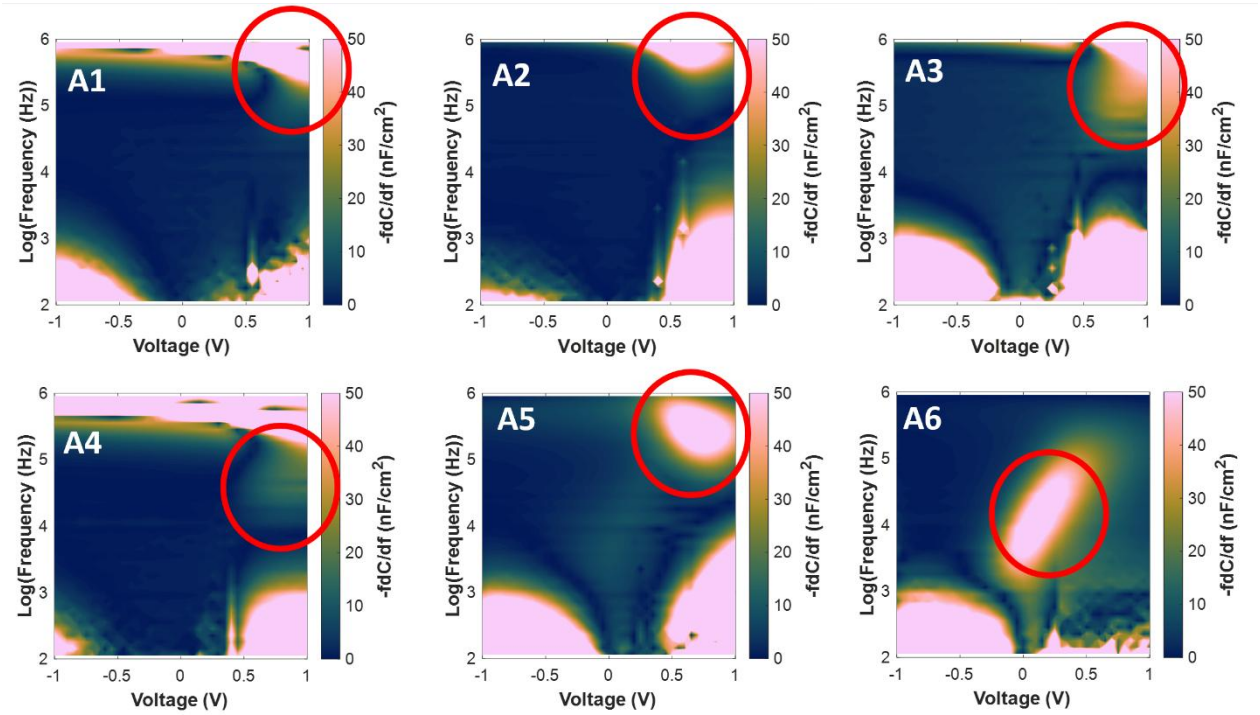

Figure 3. Room temperature CVf-loss maps of the Sample A devices. The red circles highlight a defect response in forward bias that is strongly limited in the bias voltage range and therefore is likely related to an interface defect.

Firstly, we can identify several common bright features in the CVf loss maps, which are often present in these p-n$^+$ type of devices. The bright feature in the bottom right hand side corner is caused by the forward DC current of the diode. In that area the dissipation factor $D = G/(2\pi fC)$ is larger than 10 and the value of the capacitance cannot be correctly measured by the LCR meter. This is also the case in the bottom left hand side corner, where the reverse shunt conductance of the device causes a large DC current, hindering the correct measurement of the capacitance. Also, at high frequencies around 1 MHz, in most devices, a large signal can be seen over the full bias range, which is the trace of the series resistance (see figure 2a). These three different signals are usually always present. As generally known, it is advantageous for the device efficiency to minimize these signals as much as possible, by maximizing the shunt resistance and by minimizing the series resistance. Nevertheless, in good devices, these signals are not the cause of very serious efficiency limitations, so we will not discuss them further in the next sections. For more extensive analysis and information about these features please refer to reference [49].

In addition, and most importantly for this work, in all the measured devices, another response is visible in the room temperature CVf loss maps. This response is highlighted by the red circles in figure 3. It consists of a response that is only present in forward bias and is quite limited in the bias voltage and frequency range. Comparing the response to the simulations of figure 2, this response can arise because of an interface defect at the CIGS-buffer interface, which is the hypothesis we will adopt in the following analysis. In fact, from all the simulated CVf-loss map responses in Reference [1] and in Figure 2, only the interface defect response does not have a tail going to reverse bias voltages. As the experimental data of the defect response highlighted with the red circles in Figure 3 does not present a tail towards negative bias voltage, we conclude that it can only arise from the interface region between the CIGS and the CdS buffer layer. One must be particularly

careful here in the analysis, as it is known that in forward bias, diffusion capacitance effects become important [21,58]. The diffusion capacitance arises due to the injection of large amounts of minority carriers into the layers, which take some time to recombine and therefore add to the capacitance response at frequencies below the characteristic frequency of the carrier recombination which is typically in the 1MHz to 1GHz range, depending on minority carrier lifetime and carrier velocity. Because our measurements go in most cases beyond the V_{oc} of the diode, certain diffusion capacitance effects are to be expected. The cutoff frequency of the diffusion capacitance is nevertheless in most cases quite high, well above 1 MHz, such that a strong frequency dependence in the absence of other frequency dependent interface defects is not expected in our measurement range. Previous analysis by Weiss et al. has also shown the diffusion capacitance effects to be small all the way to the V_{OC} [21].
In some cases, the interface trap response in forward bias merges with the series resistance response or lies at too high frequency and cannot be clearly identified at room temperature. Example cases for this are samples A1, A2 and to some extent A3. In such case it is possible to reduce the measurement temperature, which will consequently slow down the defect response through the action of the temperature in equation (1) and which will effectively separate it from the series resistance response at high frequency, or which will reduce it to lower frequencies such that it will fit in the measurement window. To visualize this, we have done these measurements for the example case of device A2. Figure 4 shows the CVf loss maps acquired at different temperatures. Whereas the trap response in the room temperature measurement cannot be clearly identified, as it slows down with decreasing temperature, it can be clearly identified as an interface response similar to the response in figure 2(e).

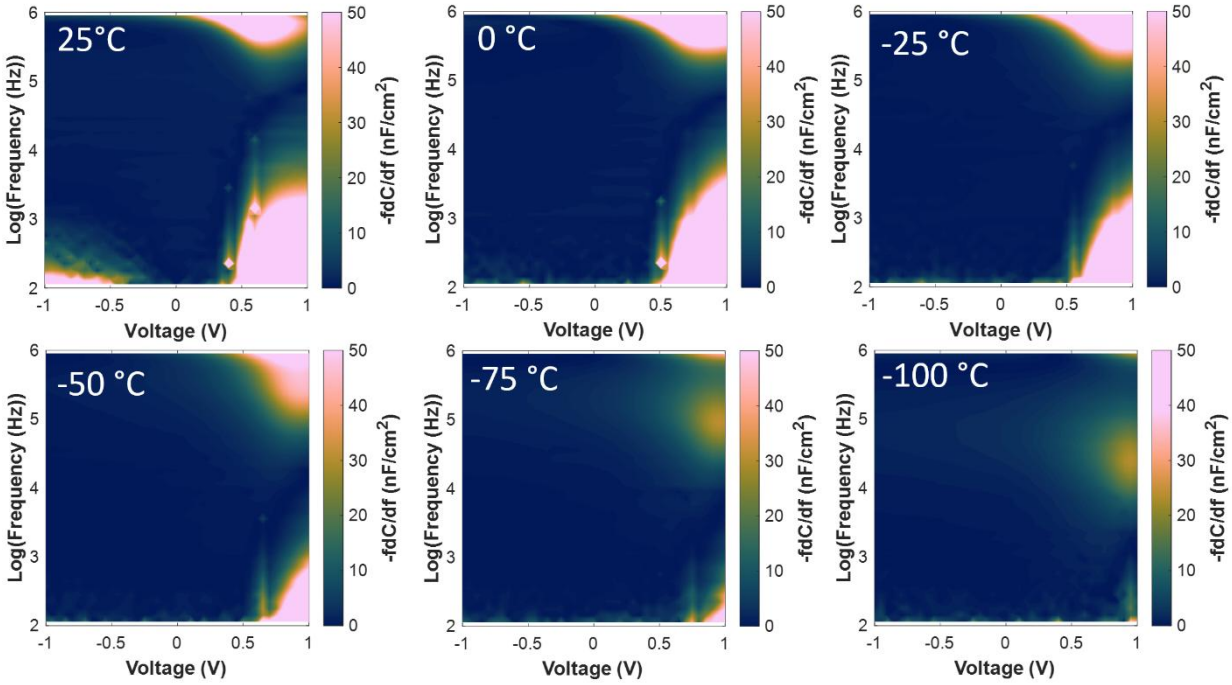

Figure 4. Low temperature CVf loss maps of sample A2. The response in forward bias can be clearly identified at lower temperatures.

Assuming that the capture cross section is independent of temperature in equation (1), we can also make an Arrhenius plot [43], plotting ωT^{-2} ($\omega = 2\pi f$) of the maximum of the admittance response

versus the inverse of the measurement temperature (1000/T). The exponential fit yields an activation energy E_a of 117 meV and a capture cross section σ of 1.4 10^{-17} cm^2, as shown in figure 5.

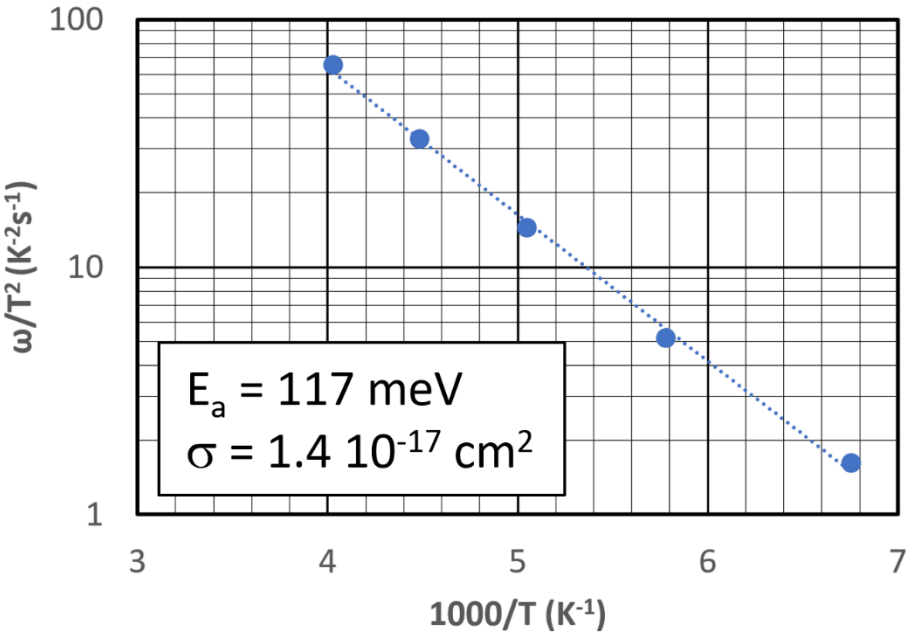

Figure 5. Arrhenius plot of the response in forward bias for sample A2.

These are very typical values for the widely reported N1 defect measured in CIGS devices before light soaking [16,59,60]. In the framework of this work, it is therefore proposed that the N1 defect is related to a defect at the CIGS-buffer interface, even though this is still heavily debated in literature [9,18,20,26,61-68]. As the main goal of this work is the analysis of the room temperature data, we did not do low temperature measurements on all the devices presented in this work, such that a very solid conclusion on the activation energy of all the presented devices will not be achievable at this point. We note also that no light-soaking study has been performed on the devices measured here, such that meta-stable effects have not yet been addressed. All admittance measurements on these devices have been performed in the dark on devices that had been only submitted to very short illumination times with an AM1.5G light spectrum.

On the other hand, so far, no very clear correlation between the intensity or position of the admittance response and the performance metrics of the different solar cell devices could be determined from the measurements. To investigate this correlation more in detail, we have produced a series of devices with a high-quality absorber layer, namely a state-of-the-art absorber fabricated by Avancis, on which we have deposited a series of different buffer layers. These are the B-type devices in this work. For device B1 a CdS buffer layer was deposited on the CIGS absorber. For device B2 a CdS buffer layer was also deposited, followed by the ALD deposition of a thin SnO_2 layer. Device B3 on the other hand only has a thin SnO_2 buffer layer deposited directly on top of the CIGS absorber. The CVf loss maps of these three devices are shown in figure 6.

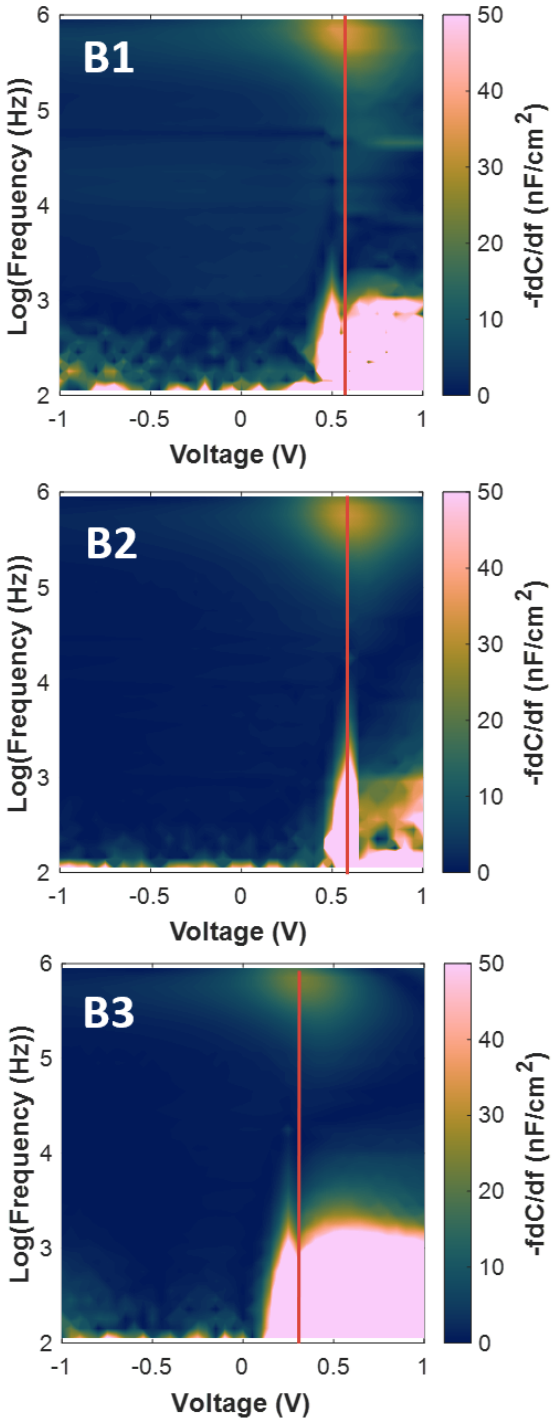

Figure 6. Room temperature CVf-loss maps of the Sample B devices. The vertical red line highlights the bias position of the defect response in forward bias, which is correlated to the V_{oc} values of the devices.

All three devices show a clear trace in forward bias, similar to the simulation of the interface defect response. Whereas devices B1 and B2 show a power conversion efficiency of about 12 % and a V_{oc} of about 600 mV, device B3 only shows a power conversion efficiency of about 5% and a V_{oc}

of about 300 mV, very drastic differences, considering that the CIGS absorber is the same. Assuming that the degradation for device B3 is caused by a worse interface quality between the CIGS and the buffer layer, one would assume a larger -fdC/df intensity in the admittance signal, as the intensity of the signal is to first order correlated to the defect density [45]. The contrary is the case though, the intensity for device B3 is marginally lower as compared to the devices B1 and B2, so it seems that the overall defect density at the interface did not vary much for the ALD SnO_2 interface as compared to the CBD CdS interface. What has changed drastically though for device B3 is the bias position of the response, which was reduced by about 300 mV to about 0.3 V instead of 0.6 V for devices B1 and B2. It seems therefore that the V_{oc} reduction was mainly caused by a difference in the DC bias voltage at which the Fermi level is crossing the interface defect in the device. Such a DC bias voltage variation at which the Fermi level is crossing the defect energy level can be caused either by a variation of the Fermi level energy at the interface, or by the variation of the energy position of the defect in the band gap of the CIGS. Considering that interface defects are often caused by intrinsic defects of the semiconductor material in question, generated by the sudden disruption of the crystal lattice at the interface [50], we consider it less likely that the energy position of the defect changed drastically between devices B1, B2 and B3, as all three CIGS absorbers are the same. The Fermi energy position at the interface on the other hand is a complex function of the doping in the p-type CIGS, the doping in the n^+-type buffer layer, the band alignment between the two layers and eventual fixed charges in the vicinity of the interface. It is very likely that SnO_2 has a very different level of n-type doping as compared to CdS, a different level of band alignment with the CIGS and possibly also a different level of fixed charges, causing this shift of the Fermi energy at the interface. This shift of Fermi energy moves the Fermi level into the defect energy now already at 300 mV lower bias voltages, charging up the defect and increasing carrier recombination at the interface, thereby reducing the photocurrent and the V_{oc} accordingly. It will also be noted that in the extreme case, when the interface response in the CVf loss map occurs already at negative bias values, such as in the case of sample A6 in Figure 3, the efficiency is almost completely reduced to zero, even though the absorber layer is of good quality.
Finally, the CVf loss map of the highest efficiency device C1 is shown in Figure 7.

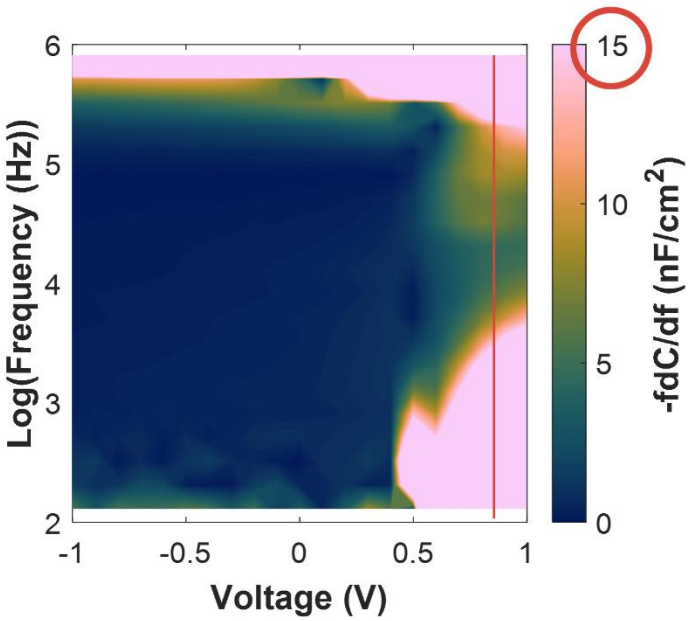

Figure 7. Room temperature CVf-loss map of sample C1. The vertical red line highlights the bias position of the defect response in forward bias. The red circle highlights the different -fdC/df scale as compared to Figures 2, 3, 4 and 6.

The interface defect can still be identified in this sample, albeit having a lower intensity as compared to the type A and type B samples. In fact, the -fdC/df axis was reduced in this figure to a maximum value of 15 nF/cm^2 instead of 50 nF/cm^2 previously, highlighted by the red circle, to clearly see the response. The intensity of the -fdC/df signal depends on the defect density on one hand, but on the other hand also on other properties like the CIGS and the buffer doping and band alignment, such that universal conclusions are difficult. Nevertheless, because very large variations in absorber and buffer doping are not expected, to first order, it seems that the efficiency of the C1 device is highest, because the number of defects at the CIGS-buffer interface was successfully decreased. Also, the bias voltage at which the response goes to a maximum in forward bias is now almost 0.8 V, also explaining the high V_{OC} values of that device as compared to the other devices. To conclude the admittance analysis, we would like to show the plausibility of the findings that the interface defect at the CIGS-buffer interface is limiting the power conversion efficiency of the solar cell. For this aim we have performed simulations with the one dimensional drift-diffusion simulation software SCAPS [48,69], where we simulate a CIGS device in which only one major type of defect is added, namely an acceptor-type defect at the CIGS-buffer interface. We have positioned this defect at the interface between the CIGS and the buffer layer at an energy of 250 meV above the valence band edge energy of the CIGS with a gaussian energy distribution and a total defect density of 2 10^{12} cm^{-2}. For our simulation, we have chosen to model the interface defect as a thin, highly defective interfacial layer with a thickness of 10 nm and a bulk defect density of 2 10^{18} cm^{-3} as this gives numerically more stable results for the simulation and also a slightly better fit to the experimental data. It is also possible to choose the interface defect option integrated in SCAPS and results will be similar. In addition to that defect, only a series resistance of 0.5 Ohm cm^2 and a shunt resistance of 2000 Ohm cm^2 were added to the device as well as carrier recombination at the front and back contacts with a low surface recombination velocity of 100 cm/s. The values of band gap, doping and electron affinity in the CIGS were 1.2 eV, 10^{16} cm^{-3} and 4.1 eV, whereas the values of band gap, doping and electron affinity in the buffer were chosen to be 2.4 eV, 1.3 10^{18} cm^{-3} and

3.9 eV. The complete device structure and all parameter settings can be found as screenshots of the various input fields of the SCAPS software input fields in the supplementary information, Figures S3 to S13, such that the interested reader can repeat the simulations.
Simulating this structure without the interface defect yields a power conversion efficiency of 29%, a Jsc of 41.9 mA/cm^2, a V_{oc} of 850 mV and a fill factor of 83.6 %, close to the intrinsic Shockley-Queisser limit [70] and mainly limited by the series and shunt resistance values, the small band offsets in the conduction and valence band edge energies between the absorber and the buffer layers and the small front and back contact recombination. Including the interface defect as described above in the simulation, yields the data as shown in figure 8, where the interface defect reduces the fill factor and V_{oc}, and accordingly reducing the power conversion efficiency to 19.3%.

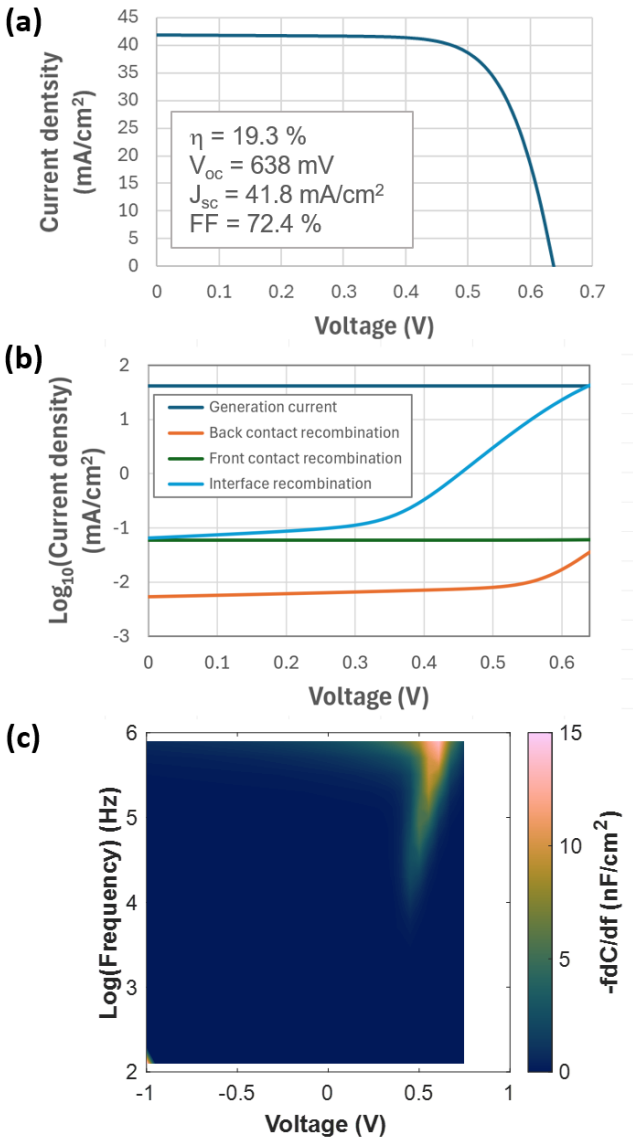

Figure 8. Simulation results of a CIGS solar cell with only an interface defect at the CIGS-CdS interface added. Current density versus voltage curve under AM1.5G illumination (a), Logarithm of the generation-recombination currents versus voltage under AM1.5G illumination (b) and room temperature CVf loss map simulated in the dark (c).

In the figure, the current density versus bias voltage under an AM1.5G illumination (a), the logarithm of the generation-recombination currents versus bias voltage under AM1.5G illumination (b) as well as the simulated CVf loss map in the dark (c) are shown. It is visible that the power conversion efficiency, V_{oc} and fill factor were reduced to about the same values as our highest performing device C1. The recombination currents show that without applied bias, the recombination via the interface defect is small, whereas it gradually increases as the bias voltage is increased, reducing fill factor gradually. When the recombination current due to the interface recombination equals the generation current, the V_{oc} of the device is obtained. Figure 8c on the other hand shows the simulated dark and room temperature CVf loss map of the cell, also resembling the interface response of the CVf loss map of the highest performing device C1 (figure 7).

Figure 9 schematically shows the band diagram of the simulated CIGS cell with the configuration of the interface defect in reverse bias and in forward bias. In reverse bias the acceptor-type interface defect is fully charged and does not contribute much to carrier recombination in the device. In forward bias on the other hand the interface defect gets partially discharged and contributes stronger to the recombination current, limiting V_{oc} and fill factor of the device.

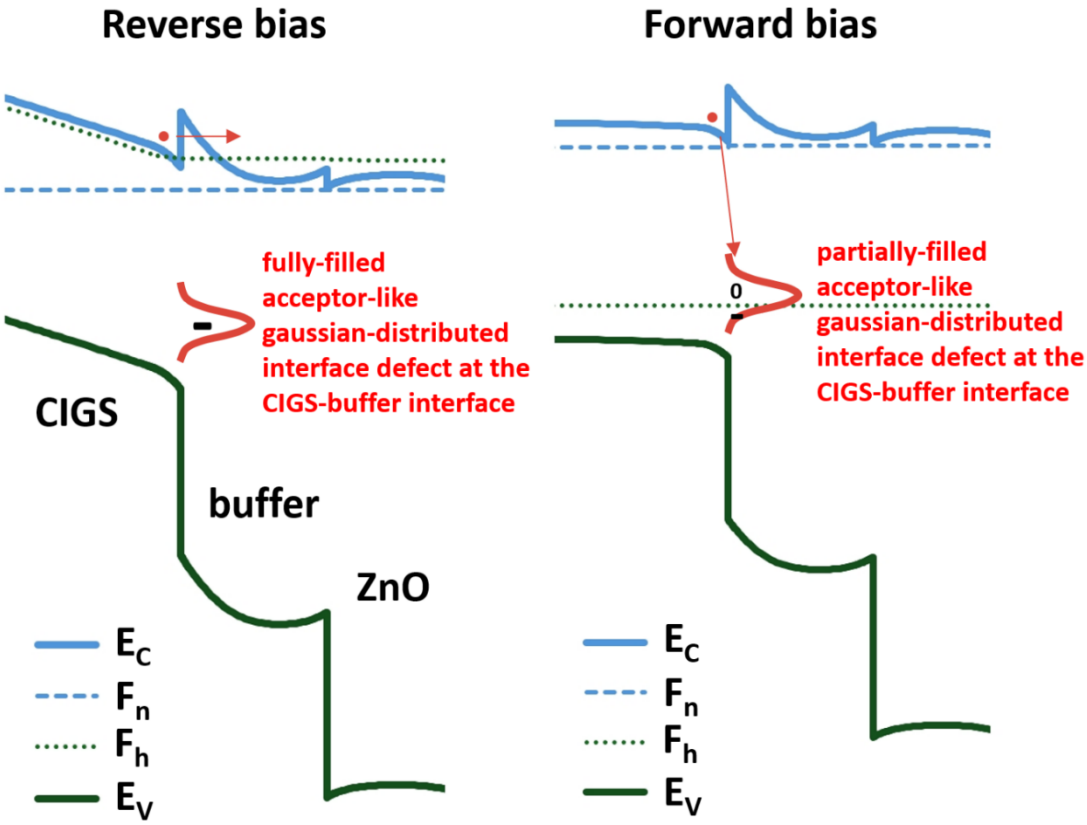

Figure 9. Schematic representation of the simulated CIGS cell and the interface defect configuration in reverse bias, where the interface defect is fully charged and not much contributing to recombination currents (left). In forward bias, the defect becomes partly discharged, contributing strongly to recombination currents and limiting V_{oc} and fill factor of the device (right). E_c is the conduction band minimum energy, E_v is the valence band maximum energy, F_n is the Fermi level for electrons and F_h is the Fermi energy for holes.

Whether the measured defect is indeed an acceptor-like defect positioned above the valence band edge energy of the CIGS cannot be said for certain, this is just one of the possible configurations, but the simulations clearly demonstrate that this is a viable hypothesis. Combining these simulation results with the observed admittance measurements, it is quite likely that the defect limiting the power conversion efficiency in the highest performing device C1 is indeed an interface defect at the CIGS-buffer interface, even though back contact recombination, bulk recombination and conduction barriers in the device likely also play a role, which might be larger or smaller, depending on the exact configuration of the cell.

IV. Conclusions

We have performed extensive bias-dependent admittance spectroscopy measurements on state-of-the-art CIGS solar cells, studying the recombination processes that are responsible for the V_{OC} and efficiency limitations of the devices. The measurement results show that in all devices a response is present which is limited to the forward bias range, which we attribute to an interface defect at the CIGS-buffer interface, because of the specific bias voltage and frequency dependence that we derived from device simulation. The clearest correlation that was found of the admittance response with the device parameters was a correlation of the bias position of the response with the open circuit voltage and the fill factor of the devices. If the response appeared at lower forward bias voltages, the fill factor and open circuit voltage were strongly reduced. The devices with the highest V_{oc} and highest power conversion efficiency values showed the response at the highest forward bias. In the highest efficiency devices, the intensity of the signal was also reduced. It therefore seems that even the highest efficiency CIGS solar cells are still limited by the effect of the interface defect. We therefore assume that further improvements to the power conversion efficiency of state-of-the-art CIGS devices must come from interface engineering at the CIGS-buffer interface, as this can influence both the density of interface defects as well as the bias voltage at which the Fermi level at the interface runs into the defect energy level. A digital twin model of the highest performing solar cell was shown, demonstrating the viability of the hypothesis that the interface defect is limiting the power conversion efficiency of the device.

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Author Contributions

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript. GuBr, RS, SH, JoPa, JdW, GiBi, TO, MM, JePo and BV conceptualized the work. GuBr, RS, SH, JoPa, JdW, GiBi, TO, MvdV, MS, DG, RB and NP did experimental investigations. MM, AN, JD, DF, TA, JePo and BV supervised the work. BV was responsible for the acquisition of funds. GB wrote the initial manuscript, and all authors reviewed and edited it.

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SUPPORTING INFORMATION

Figure S1 shows the simulation of the low-temperature behavior of an interface defect, and Figure S2 illustrates how the voltage position of the interface defect in the CVf loss map can influence the open-circuit voltage and fill factor in JV curves. Figures S3–S13 contain screenshots of all SCAPS input fields used for the simulations presented in Figure 8 of the main text. This material is available free of charge via the Internet at http://pubs.acs.org.

REFERENCES

(1) Nicollian, E. H.; Brews, J. R. *MOS (Metal Oxide Semiconductor) Physics and Technology*, Wiley classics library ed.; Wiley classics library; Wiley-Interscience: Hoboken, NJ, 2003.
(2) Truong, L.; Fedorenko, Y. G.; Afanaśev, V. V.; Stesmans, A. Admittance Spectroscopy of Traps at the Interfaces of (100)Si with Al2O3, ZrO2, and HfO2. *Microelectron. Reliab.* **2005**, *45* (5–6), 823–826. https://doi.org/10.1016/j.microrel.2004.11.039.
(3) Preier, H. CONTRIBUTIONS OF SURFACE STATES TO MOS IMPEDANCE. *Appl. Phys. Lett.* **1967**, *10* (12), 361–363. https://doi.org/10.1063/1.1728213.
(4) Nicollian, E. H.; Goetzberger, A. MOS CONDUCTANCE TECHNIQUE FOR MEASURING SURFACE STATE PARAMETERS. In *Semiconductor Devices: Pioneering Papers*; WORLD SCIENTIFIC, 1991; pp 558–561. https://doi.org/10.1142/9789814503464_0072.
(5) Leon, C.; Le Gall, S.; Gueunier-Farret, M.-E.; Kleider, J.-P. How to Perform Admittance Spectroscopy and DLTS in Multijunction Solar Cells. *Sol. Energy Mater. Sol. Cells* **2022**, *240*, 111699. https://doi.org/10.1016/j.solmat.2022.111699.
(6) Itagaki, M.; Suzuki, S.; Shitanda, I.; Watanabe, K. Electrochemical Impedance and Complex Capacitance to Interpret Electrochemical Capacitor. *Electrochemistry* **2007**, *75* (8), 649–655. https://doi.org/10.5796/electrochemistry.75.649.
(7) Gaberšček, M. Impedance Spectroscopy of Battery Cells: Theory versus Experiment. *Curr. Opin. Electrochem.* **2022**, *32*, 100917. https://doi.org/10.1016/j.coelec.2021.100917.
(8) Li, H.; Liu, X.; Li, L.; Mu, X.; Genov, R.; Mason, A. CMOS Electrochemical Instrumentation for Biosensor Microsystems: A Review. *Sensors* **2016**, *17* (1), 74. https://doi.org/10.3390/s17010074.

(9) Werner, F.; Siebentritt, S. Buffer Layers, Defects, and the Capacitance Step in the Admittance Spectrum of a Thin-Film Solar Cell. *Phys. Rev. Appl.* **2018**, *9* (5), 054047. https://doi.org/10.1103/PhysRevApplied.9.054047.
(10) Gomeniuk, Y. V.; Lytvyn, P. M.; Gomeniuk, Y. Y.; Rudenko, T. E.; Vasin, A. V.; Rusavsky, A. V.; Lysenko, V. S.; Kilchytska, V.; Flandre, D.; Nazarov, A. N. Charge Transport and Charge Trapping in Polycrystalline ZnO Thin Films Doped by Methane: Local and Integrated Analysis. *Phys. Scr.* **2025**, *100* (2), 025905. https://doi.org/10.1088/1402-4896/ada4ea.
(11) Arya, S.; Mahajan, P. CIGS-Based Solar Cells. In *Solar Cells*; Springer Nature Singapore: Singapore, 2023; pp 77–100. https://doi.org/10.1007/978-981-99-7333-0_3.
(12) Hamtaei, S.; Debot, A.; Scaffidi, R.; Brammertz, G.; Cariou, E.; Garner, S. M.; Aguirre, A.; Poortmans, J.; Dale, P. J.; Vermang, B. Fabrication of Bendable and Narrow Bandgap Cu(In,Ga)(S,Se)2 for Tandem Photovoltaics. *Commun. Mater.* **2025**, *6* (1), 2. https://doi.org/10.1038/s43246-024-00706-x.
(13) Feurer, T.; Reinhard, P.; Avancini, E.; Bissig, B.; Löckinger, J.; Fuchs, P.; Carron, R.; Weiss, T. P.; Perrenoud, J.; Stutterheim, S.; Buecheler, S.; Tiwari, A. N. Progress in Thin Film CIGS Photovoltaics – Research and Development, Manufacturing, and Applications. *Prog. Photovolt. Res. Appl.* **2017**, *25* (7), 645–667. https://doi.org/10.1002/pip.2811.
(14) Keller, J.; Kiselman, K.; Donzel-Gargand, O.; Martin, N. M.; Babucci, M.; Lundberg, O.; Wallin, E.; Stolt, L.; Edoff, M. High-Concentration Silver Alloying and Steep Back-Contact Gallium Grading Enabling Copper Indium Gallium Selenide Solar Cell with 23.6% Efficiency. *Nat. Energy* **2024**. https://doi.org/10.1038/s41560-024-01472-3.
(15) Elanzeery, H.; Stölzel, M.; Eraerds, P.; Borowski, P.; Aboulfadl, H.; Lomuscio, A.; Helmecke, D.; Schubbert, C.; Oueslati, S.; Hála, M.; Röder, J.; Giesl, F.; Dalibor, T. Beyond 20% World Record Efficiency for Thin-Film Solar Modules. *IEEE J. Photovolt.* **2024**, *14* (1), 107–115. https://doi.org/10.1109/JPHOTOV.2023.3326559.
(16) Herberholz, R.; Igalson, M.; Schock, H. W. Distinction between Bulk and Interface States in CuInSe2/CdS/ZnO by Space Charge Spectroscopy. *J. Appl. Phys.* **1998**, *83* (1), 318–325. https://doi.org/10.1063/1.366686.
(17) Werner, F.; Babbe, F.; Elanzeery, H.; Siebentritt, S. Can We See Defects in Capacitance Measurements of Thin-film Solar Cells? *Prog. Photovolt. Res. Appl.* **2019**, *27* (11), 1045–1058. https://doi.org/10.1002/pip.3196.
(18) Hölscher, T.; Walter, T.; Schneider, T.; Maiberg, M.; Scheer, R. Device Simulation of Cu(In,Ga)Se2 Solar Cells by Means of Voltage Dependent Admittance Spectroscopy. *Thin Solid Films* **2019**, *669*, 345–350. https://doi.org/10.1016/j.tsf.2018.11.022.
(19) Cunha, J. M. V.; Rocha, C.; Vinhais, C.; Fernandes, P. A.; Salome, P. M. P. Understanding the AC Equivalent Circuit Response of Ultrathin Cu(In,Ga)Se_2 Solar Cells. *IEEE J. Photovolt.* **2019**, *9* (5), 1442–1448. https://doi.org/10.1109/JPHOTOV.2019.2927918.
(20) Werner, F.; Wolter, M. H.; Siebentritt, S.; Sozzi, G.; Di Napoli, S.; Menozzi, R.; Jackson, P.; Witte, W.; Carron, R.; Avancini, E.; Weiss, T. P.; Buecheler, S. Alkali Treatments of Cu(In,Ga)Se_2 Thin-film Absorbers and Their Impact on Transport Barriers. *Prog. Photovolt. Res. Appl.* **2018**, *26* (11), 911–923. https://doi.org/10.1002/pip.3032.
(21) Weiss, T. P.; Nishiwaki, S.; Bissig, B.; Buecheler, S.; Tiwari, A. N. Voltage Dependent Admittance Spectroscopy for the Detection of near Interface Defect States for Thin Film Solar Cells. *Phys. Chem. Chem. Phys.* **2017**, *19* (45), 30410–30417. https://doi.org/10.1039/C7CP05236G.
(22) Bailey, J.; Zapalac, G.; Poplavskyy, D. Metastable Defect Measurement from Capacitance-Voltage and Admittance Measurements in Cu(In, Ga)Se2 Solar Cells. In *2016 IEEE 43rd Photovoltaic Specialists Conference (PVSC)*; IEEE: Portland, OR, USA, 2016; pp 2135–2140. https://doi.org/10.1109/PVSC.2016.7750011.

(23) Marin, A. T.; Musselman, K. P.; MacManus-Driscoll, J. L. Accurate Determination of Interface Trap State Parameters by Admittance Spectroscopy in the Presence of a Schottky Barrier Contact: Application to ZnO-Based Solar Cells. *J. Appl. Phys.* **2013**, *113* (14), 144502. https://doi.org/10.1063/1.4799633.
(24) Decock, K.; Khelifi, S.; Buecheler, S.; Pianezzi, F.; Tiwari, A. N.; Burgelman, M. Defect Distributions in Thin Film Solar Cells Deduced from Admittance Measurements under Different Bias Voltages. *J. Appl. Phys.* **2011**, *110* (6), 063722. https://doi.org/10.1063/1.3641987.
(25) Lauwaert, J.; Decock, K.; Khelifi, S.; Burgelman, M. A Simple Correction Method for Series Resistance and Inductance on Solar Cell Admittance Spectroscopy. *Sol. Energy Mater. Sol. Cells* **2010**, *94* (6), 966–970. https://doi.org/10.1016/j.solmat.2010.01.025.
(26) Eisenbarth, T.; Unold, T.; Caballero, R.; Kaufmann, C. A.; Schock, H.-W. Interpretation of Admittance, Capacitance-Voltage, and Current-Voltage Signatures in Cu(In,Ga)Se2 Thin Film Solar Cells. *J. Appl. Phys.* **2010**, *107* (3), 034509. https://doi.org/10.1063/1.3277043.
(27) Burgelman, M.; Nollet, P. Admittance Spectroscopy of Thin Film Solar Cells. *Solid State Ion.* **2005**, *176* (25–28), 2171–2175. https://doi.org/10.1016/j.ssi.2004.08.048.
(28) Repins, I.; Contreras, M. A.; Egaas, B.; DeHart, C.; Scharf, J.; Perkins, C. L.; To, B.; Noufi, R. 19·9%-efficient ZnO/CdS/CuInGaSe ^{2} Solar Cell with 81·2% Fill Factor. *Prog. Photovolt. Res. Appl.* **2008**, *16* (3), 235–239. https://doi.org/10.1002/pip.822.
(29) Kato, T. Cu(In,Ga)(Se,S)$_2$ Solar Cell Research in Solar Frontier: Progress and Current Status. *Jpn. J. Appl. Phys.* **2017**, *56* (4S), 04CA02. https://doi.org/10.7567/JJAP.56.04CA02.
(30) Powalla, M.; Paetel, S.; Ahlswede, E.; Wuerz, R.; Wessendorf, C. D.; Magorian Friedlmeier, T. Thin-Film Solar Cells Exceeding 22% Solar Cell Efficiency: An Overview on CdTe-, Cu(In,Ga)Se2-, and Perovskite-Based Materials. *Appl. Phys. Rev.* **2018**, *5* (4), 041602. https://doi.org/10.1063/1.5061809.
(31) Jung, S.; Ahn, S.; Yun, J. H.; Gwak, J.; Kim, D.; Yoon, K. Effects of Ga Contents on Properties of CIGS Thin Films and Solar Cells Fabricated by Co-Evaporation Technique. *Curr. Appl. Phys.* **2010**, *10* (4), 990–996. https://doi.org/10.1016/j.cap.2009.11.082.
(32) Lee, D.; Yang, J.; Kim, Y.-S.; Mo, C. B.; Park, S.; Kim, B.; Kim, D.; Nam, J.; Kang, Y. Effects of the Cu/(Ga+In) Ratio on the Bulk and Interface Properties of Cu(InGa)(SSe)2 Solar Cells. *Sol. Energy Mater. Sol. Cells* **2016**, *149*, 195–203. https://doi.org/10.1016/j.solmat.2016.01.023.
(33) Zhu, C.; Liu, W.; Li, Y.; Huo, X.; Li, H.; Guo, K.; Qiao, B.; Zhao, S.; Xu, Z.; Zhao, H.; Song, D. Key Factors Governing the Device Performance of CIGS Solar Cells: Insights from Machine Learning. *Sol. Energy* **2021**, *228*, 45–52. https://doi.org/10.1016/j.solener.2021.09.031.
(34) Hashimoto, Y.; Kohara, N.; Negami, T.; Nishitani, N.; Wada, T. Chemical Bath Deposition of Cds Buffer Layer for GIGS Solar Cells. *Sol. Energy Mater. Sol. Cells* **1998**, *50* (1–4), 71–77. https://doi.org/10.1016/S0927-0248(97)00124-4.
(35) Dhere, N. G.; Waterhouse, D. L.; Sundaram, K. B.; Melendez, O.; Parikh, N. R.; Patnaik, B. Studies on Chemical Bath Deposited Cadmium Sulphide Films by Buffer Solution Technique. *J. Mater. Sci. Mater. Electron.* **1995**, *6* (1). https://doi.org/10.1007/BF00208134.
(36) Buffière, M.; Mel, A. E.; Lenaers, N.; Brammertz, G.; Zaghi, A. E.; Meuris, M.; Poortmans, J. Surface Cleaning and Passivation Using (NH_4)$_2$ S Treatment for Cu(In,Ga)Se$_2$ Solar Cells: A Safe Alternative to KCN. *Adv. Energy Mater.* **2015**, *5* (6), 1401689. https://doi.org/10.1002/aenm.201401689.
(37) Soonmin, H. Recent Advances in the Growth and Characterizations of SILAR-Deposited Thin Films. *Appl. Sci.* **2022**, *12* (16), 8184. https://doi.org/10.3390/app12168184.
(38) Lindroos, S.; Kanniainen, T.; Leskelä, M. Growth of ZnS Thin Films by Liquid-Phase Atomic Layer Epitaxy (LPALE). *Appl. Surf. Sci.* **1994**, *75* (1–4), 70–74. https://doi.org/10.1016/0169-4332(94)90138-4.

(39) Mullings, M. N.; Hägglund, C.; Bent, S. F. Tin Oxide Atomic Layer Deposition from Tetrakis(Dimethylamino)Tin and Water. *J. Vac. Sci. Technol. Vac. Surf. Films* **2013**, *31* (6), 061503. https://doi.org/10.1116/1.4812717.
(40) Ramachandran, R. K.; Filez, M.; Dendooven, J.; Galvita, V. V.; Poelman, H.; Solano, E.; Fonda, E.; Marin, G. B.; Detavernier, C. Size- and Composition-Controlled Pt–Sn Bimetallic Nanoparticles Prepared by Atomic Layer Deposition. *RSC Adv.* **2017**, *7* (33), 20201–20205. https://doi.org/10.1039/C7RA01463E.
(41) Shockley, W.; Read, W. T. Statistics of the Recombinations of Holes and Electrons. *Phys. Rev.* **1952**, *87* (5), 835–842. https://doi.org/10.1103/PhysRev.87.835.
(42) Hall, R. N. Electron-Hole Recombination in Germanium. *Phys. Rev.* **1952**, *87* (2), 387–387. https://doi.org/10.1103/PhysRev.87.387.
(43) Heath, J.; Zabierowski, P. Capacitance Spectroscopy of Thin-Film Solar Cells. In *Advanced Characterization Techniques for Thin Film Solar Cells*; Abou-Ras, D., Kirchartz, T., Rau, U., Eds.; Wiley, 2011; pp 81–105. https://doi.org/10.1002/9783527636280.ch4.
(44) Martens, K.; Chui, C. O.; Brammertz, G.; De Jaeger, B.; Kuzum, D.; Meuris, M.; Heyns, M.; Krishnamohan, T.; Saraswat, K.; Maes, H. E.; Groeseneken, G. On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates. *IEEE Trans. Electron Devices* **2008**, *55* (2), 547–556. https://doi.org/10.1109/TED.2007.912365.
(45) Walter, T.; Herberholz, R.; Müller, C.; Schock, H. W. Determination of Defect Distributions from Admittance Measurements and Application to Cu(In,Ga)Se2 Based Heterojunctions. *J. Appl. Phys.* **1996**, *80* (8), 4411–4420. https://doi.org/10.1063/1.363401.
(46) Burgelman, M.; Nollet, P.; Degrave, S. Modelling Polycrystalline Semiconductor Solar Cells. *Thin Solid Films* **2000**, *361–362*, 527–532. https://doi.org/10.1016/S0040-6090(99)00825-1.
(47) Decock, K.; Khelifi, S.; Burgelman, M. Modelling Multivalent Defects in Thin Film Solar Cells. *Thin Solid Films* **2011**, *519* (21), 7481–7484. https://doi.org/10.1016/j.tsf.2010.12.039.
(48) Decock, K.; Zabierowski, P.; Burgelman, M. Modeling Metastabilities in Chalcopyrite-Based Thin Film Solar Cells. *J. Appl. Phys.* **2012**, *111* (4), 043703. https://doi.org/10.1063/1.3686651.
(49) Brammertz, G.; Kohl, T.; De Wild, J.; Buldu, D. G.; Birant, G.; Meuris, M.; Poortmans, J.; Vermang, B. Bias-Dependent Admittance Spectroscopy of Thin-Film Solar Cells: Experiment and Simulation. *IEEE J. Photovolt.* **2020**, *10* (4), 1102–1111. https://doi.org/10.1109/JPHOTOV.2020.2992350.
(50) Lüth, H. *Solid Surfaces, Interfaces and Thin Films*; Graduate Texts in Physics; Springer International Publishing: Cham, 2015. https://doi.org/10.1007/978-3-319-10756-1.
(51) Schulz, M. Interface States at the SiO2-Si Interface. *Surf. Sci.* **1983**, *132* (1–3), 422–455. https://doi.org/10.1016/0039-6028(83)90551-4.
(52) Castagné, R.; Vapaille, A. Description of the SiO2□Si Interface Properties by Means of Very Low Frequency MOS Capacitance Measurements. *Surf. Sci.* **1971**, *28* (1), 157–193. https://doi.org/10.1016/0039-6028(71)90092-6.
(53) Brammertz, G.; Buffière, M.; Oueslati, S.; ElAnzeery, H.; Ben Messaoud, K.; Sahayaraj, S.; Köble, C.; Meuris, M.; Poortmans, J. Characterization of Defects in 9.7% Efficient Cu2ZnSnSe4-CdS-ZnO Solar Cells. *Appl. Phys. Lett.* **2013**, *103* (16), 163904. https://doi.org/10.1063/1.4826448.
(54) Brammertz, G.; Martens, K.; Sioncke, S.; Delabie, A.; Caymax, M.; Meuris, M.; Heyns, M. Characteristic Trapping Lifetime and Capacitance-Voltage Measurements of GaAs Metal-Oxide-Semiconductor Structures. *Appl. Phys. Lett.* **2007**, *91* (13), 133510. https://doi.org/10.1063/1.2790787.
(55) Brammertz, G.; Lin, H.-C.; Martens, K.; Mercier, D.; Sioncke, S.; Delabie, A.; Wang, W. E.; Caymax, M.; Meuris, M.; Heyns, M. Capacitance-Voltage Characterization of GaAs–Al2O3 Interfaces. *Appl. Phys. Lett.* **2008**, *93* (18), 183504. https://doi.org/10.1063/1.3005172.

(56) Brammertz, G.; Lin, H.-C.; Caymax, M.; Meuris, M.; Heyns, M.; Passlack, M. On the Interface State Density at In0.53Ga0.47As/Oxide Interfaces. *Appl. Phys. Lett.* **2009**, *95* (20), 202109. https://doi.org/10.1063/1.3267104.
(57) Brammertz, G.; Alian, A.; Lin, D. H.-C.; Meuris, M.; Caymax, M.; Wang, W.-E. A Combined Interface and Border Trap Model for High-Mobility Substrate Metal–Oxide–Semiconductor Devices Applied to $\hbox{In}_{0.53} \hbox{Ga}_{0.47}\hbox{As}$ and InP Capacitors. *IEEE Trans. Electron Devices* **2011**, *58* (11), 3890–3897. https://doi.org/10.1109/TED.2011.2165725.
(58) Sze, S. M.; Ng, K. K. *Physics of Semiconductor Devices*, 1st ed.; Wiley, 2006. https://doi.org/10.1002/0470068329.
(59) Zabierowski, P.; Rau, U.; Igalson, M. Classification of Metastabilities in the Electrical Characteristics of ZnO/CdS/Cu(In,Ga)Se2 Solar Cells. *Thin Solid Films* **2001**, *387* (1–2), 147–150. https://doi.org/10.1016/S0040-6090(00)01850-2.
(60) Heise, S. J.; Hirwa, H.; Stölzel, M.; Dalibor, T.; Ohland, J. Investigating the Origin of the N1 Signature in Admittance Spectroscopy of Cu(In,Ga)(S,Se) 2 Thin-Film Solar Cells by a Variation of Individual Cell Layers. *Thin Solid Films* **2022**, *759*, 139463. https://doi.org/10.1016/j.tsf.2022.139463.
(61) Heath, J. T.; Cohen, J. D.; Shafarman, W. N. Bulk and Metastable Defects in CuIn1−xGaxSe2 Thin Films Using Drive-Level Capacitance Profiling. *J. Appl. Phys.* **2004**, *95* (3), 1000–1010. https://doi.org/10.1063/1.1633982.
(62) Heise, S. J.; Gerliz, V.; Hammer, M. S.; Ohland, J.; Keller, J.; Hammer-Riedel, I. Light-Induced Changes in the Minority Carrier Diffusion Length of Cu(In,Ga)Se2 Absorber Material. *Sol. Energy Mater. Sol. Cells* **2017**, *163*, 270–276. https://doi.org/10.1016/j.solmat.2017.01.045.
(63) Djebbour, Z.; Darga, A.; Migan Dubois, A.; Mencaraglia, D.; Naghavi, N.; Guillemoles, J.-F.; Lincot, D. Admittance Spectroscopy of Cadmium Free CIGS Solar Cells Heterointerfaces. *Thin Solid Films* **2006**, *511–512*, 320–324. https://doi.org/10.1016/j.tsf.2005.11.087.
(64) Eisenbarth, T.; Unold, T.; Caballero, R.; Kaufmann, C. A.; Abou-Ras, D.; Schock, H.-W. Origin of Defects in CuIn1−xGaxSe2 Solar Cells with Varied Ga Content. *Thin Solid Films* **2009**, *517* (7), 2244–2247. https://doi.org/10.1016/j.tsf.2008.10.142.
(65) Reislöhner, U.; Metzner, H.; Ronning, C. Hopping Conduction Observed in Thermal Admittance Spectroscopy. *Phys. Rev. Lett.* **2010**, *104* (22), 226403. https://doi.org/10.1103/PhysRevLett.104.226403.
(66) Lauwaert, J.; Van Puyvelde, L.; Lauwaert, J.; Thybaut, J. W.; Khelifi, S.; Burgelman, M.; Pianezzi, F.; Tiwari, A. N.; Vrielinck, H. Assignment of Capacitance Spectroscopy Signals of CIGS Solar Cells to Effects of Non-Ohmic Contacts. *Sol. Energy Mater. Sol. Cells* **2013**, *112*, 78–83. https://doi.org/10.1016/j.solmat.2013.01.014.
(67) Schoneberg, J.; Ohland, J.; Eraerds, P.; Dalibor, T.; Parisi, J.; Richter, M. Accessing the Band Alignment in High Efficiency Cu(In,Ga)(Se,S)2 (CIGSSe) Solar Cells with an InxSy:Na Buffer Based on Temperature Dependent Measurements and Simulations. *J. Appl. Phys.* **2018**, *123* (15), 155701. https://doi.org/10.1063/1.5017087.
(68) Schneider, T.; Dethloff, C.; Hölscher, T.; Kempa, H.; Scheer, R. Comparison of Mo and ITO Back Contacts in CIGSe Solar Cells: Vanishing of the Main Capacitance Step. *Prog. Photovolt. Res. Appl.* **2022**, *30* (2), 191–202. https://doi.org/10.1002/pip.3476.
(69) Burgelman, M.; Decock, K.; Khelifi, S.; Abass, A. Advanced Electrical Simulation of Thin Film Solar Cells. *Thin Solid Films* **2013**, *535*, 296–301. https://doi.org/10.1016/j.tsf.2012.10.032.
(70) Shockley, W.; Queisser, H. J. Detailed Balance Limit of Efficiency of *p-n* Junction Solar Cells. *J. Appl. Phys.* **1961**, *32* (3), 510–519. https://doi.org/10.1063/1.1736034.