Faculteit Industriële Ingenieurswetenschappen

master in de industriële wetenschappen: elektronica-ICT

Masterthesis

Development of a Measuring System for a Textile-Based Organic Electrochemical Transistor

Laurence Jorissen

Scriptie ingediend tot het behalen van de graad van master in de industriële wetenschappen: elektronica-ICT

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Preface

This thesis was carried out as part of an Erasmus traineeship at Hochschule Niederrhein in Mönchengladbach, Germany, within the Faculty of Textile and Clothing Technology. The subject of the thesis was aligned with my personal interests, which led to an introduction to a textile-based organic electrochemical transistor that had been previously developed at the faculty.

Initially, the goal was to design a demonstration device to highlight the sensor's wearability. However, as the project evolved, the scope expanded. The focus shifted toward developing a custom measurement system, not only to demonstrate the sensor but also to support its further development.

I would like to express my gratitude to my external supervisor, Prof. Dr. Ir. Anne Schwarz-Pfeiffer, and my internal supervisor, Prof. Dr. Ir. Wim Deferme, for their guidance, feedback and support throughout the course of this thesis.

I am also thankful to the research group at Hochschule Niederrhein, including Rsc. Rike Brendgen, Joel Schüßler, and Theresa Junge, for their guidance and insightful discussions.

Furthermore, I am grateful to Rsc. Thijs Vandenryt, Lambert-Paul Jorissen, and Johannes Chopov for their technical support, input, and encouragement during my stay.

Finally, I would like to thank my family for their continuous support and motivation throughout this experience.

Looking back, I am truly grateful for the opportunity to work in such a supportive and inspiring environment, which allowed me to grow both technically and personally throughout the course of this thesis.

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Abstract

Modern healthcare increasingly demands non-invasive, comfortable and accurate monitoring solutions. Textile-based Organic Electrochemical Transistors (OECTs) are promising candidates due to their biocompatibility, low operating voltage and high sensitivity. However, their effective development and integration into wearable devices require precise electrical characterization and reliable measurement systems.

This master's thesis presents the design and implementation of a compact, user-friendly measurement platform capable of accurately controlling gate and drain voltages and detecting low drain and gate currents in the microampere range. The system features a digital-to-analog converter for voltage control, a transimpedance amplifier for current-to-voltage conversion, and a high-resolution analog-to-digital converter for data acquisition. All components were designed, simulated and integrated on a microcontroller-based platform with wireless data transmission and a custom-built user interface.

Experimental results demonstrate reliable voltage regulation in the millivolt range and accurate current measurement, making the system suitable for real-time OECT monitoring and for supporting material scientists in evaluating and optimizing the electrical properties of OECT-based sensors. This platform represents a significant step toward practical and efficient OECT characterization and deployment in future healthcare applications.

Abstract in Dutch

De moderne gezondheidszorg vraagt steeds meer om niet-invasieve, comfortabele en nauwkeurige monitoringoplossingen. Textielgebaseerde organische elektrochemische transistoren (OECT's) zijn veelbelovende kandidaten vanwege hun biocompatibiliteit, lage werkspanning en hoge gevoeligheid. Hun effectieve ontwikkeling en integratie in draagbare apparaten vereisen echter een nauwkeurige elektrische karakterisering en betrouwbare meetsystemen.

Deze masterscriptie presenteert het ontwerp en de implementatie van een compact, gebruiksvriendelijk meetplatform dat gate- en drainspanningen nauwkeurig kan regelen en lage drain- en gatestromen in het microampèrebereik kan detecteren. Het systeem beschikt over een digitaal-naar-analoogconverter voor spanningsregeling, een transimpedantieversterker voor stroom-naar-spanningsconversie en een analoog-naar-digitaalconverter met hoge resolutie voor data-acquisitie. Alle componenten zijn ontworpen, gesimuleerd en geïntegreerd op een microcontrollergebaseerd platform met draadloze datatransmissie en een speciaal ontwikkelde gebruikersinterface.

Experimentele resultaten tonen een betrouwbare spanningsregeling in het millivoltbereik en nauwkeurige stroommeting aan, waardoor het systeem geschikt is voor realtime OECT-monitoring en voor het ondersteunen van materiaalwetenschappers bij het evalueren en optimaliseren van de elektrische eigenschappen van OECT-gebaseerde sensoren. Dit platform vormt een belangrijke stap in de richting van praktische en efficiënte OECT-karakterisering en implementatie in toekomstige toepassingen in de gezondheidszorg.

Chapter 1

Introduction

1.1 Context

Improving patient comfort and disease management are key goals in modern health monitoring systems. Therefore, textile-based sensors such as modified Organic Electrochemical Transistors (OECTs) are gaining significant attention due to their low operating voltage, high sensitivity, and biocompatibility. These attributes make them ideal for developing non-invasive, wearable sensors that monitor physiological processes such as glucose and ion levels with minimal discomfort [1]–[3].

The technology behind OECTs is similar to traditional transistors, as they can amplify and switch electrical signals. However, a unique feature of OECTs is the use of the organic conductive polymer PEDOT:PSS as the channel, which can absorb and release ions, making it ideal for biomedical applications. As seen in Figure 1.1, OECTs utilize a unique gating mechanism with an electrolyte layer placed between the gate (G) and the organic source-drain channel, where the current is primarily controlled by ion movement and chemical processes within the electrolyte. In its default doped state, PEDOT:PSS is highly conductive, enabling efficient current flow between the source (S) and drain (D) electrodes. Applying a voltage to the drain (Vds) maintains this conductive state. However, when a positive voltage is applied to the gate (V_{gs}), ions from the electrolyte are driven into the PEDOT:PSS channel. This process causes de-doping of the material, resulting in a decrease in the channel's conductivity [1]–[5].

This ion-driven modulation allows OECTs to function as highly sensitive sensors. A prime example is glucose detection, where the electrolyte is functionalized with enzymes that react specifically with glucose molecules. This reaction triggers ion movement in the electrolyte, changing the conductivity of the channel and results in measurable changes of the source-drain current. Therefore, OECTs can sensitively measure analyte concentrations, such as glucose levels in sweat, through electrical signals. Furthermore, integrating OECT technology with textiles opens promising possibilities for wearable devices capable of real-time physiological monitoring during physical activity. Systems that combine textile and non-textile components to actively interact with the user or environment, or so-called "smart textiles", provide an ideal platform for these innovations [1], [2].

At Hochschule Niederrhein, Faculty of Textile and Clothing Technology in Mönchengladbach (Germany), expertise in textile materials and functional integration enabled the successful de-

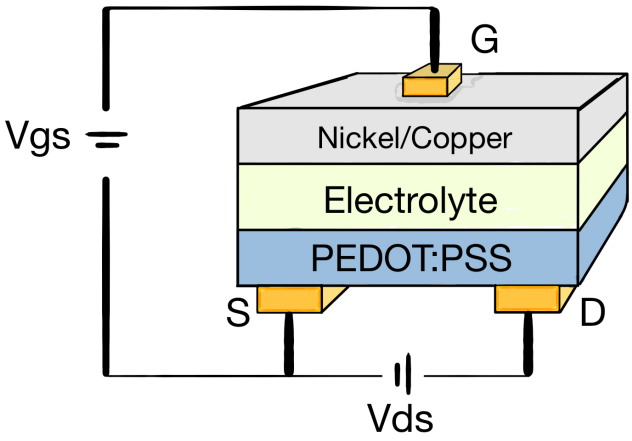


Figure 1.1: *Schematic diagram of the OECT device structure, illustrating its key components: the gate electrode, electrolyte layer, PEDOT:PSS channel, and the source-drain electrodes. Voltage sources are connected to the gate, source, and drain to control the operation of the device.*

velopment of a textile-based OECT. This device incorporates a conductive nickel/copper-coated ripstop fabric as the gate electrode, an electrolyte layer, and a cellulose-based porous nonwoven substrate spray coated with PEDOT:PSS. This innovation is a significant advancement in the field of smart textiles, demonstrating the potential of combining electronics with everyday fabrics for wearable sensing applications [1], [2]. However, before transitioning from a textile-based OECT to a fully integrated smart textile device, it is crucial to distinguish the sensor from its measurement system. A stable and reliable measurement system is not only essential for obtaining accurate and consistent results from the OECT sensor but also for streamlining the process of improving sensor design.

1.2 Problem Statement

Despite the successful development of textile-based OECTs, reliable measurement systems for these devices face several challenges.

First of all, these devices are still in the early stages of development, and variations in material properties and fabrication processes lead to inconsistent electrical characteristics between individual sensors, as these processes are not yet fully optimized [1], [2]. Secondly, OECTs inherently operate at low voltages, resulting in source-drain currents in the microampere range [1]–[5]. This makes accurate and stable current measurements more difficult, as even minor noise can significantly affect signal interpretation. Additionally, switching from a flexible textile material, such as a nonwoven substrate with PEDOT:PSS to a rigid, metal probe can introduce issues such as contact resistance, also reducing the accuracy and stability of the measurements [6]. Together, these challenges limit the advancement of textile-based OECTs towards future biomedical applications.

The development of a robust measurement system to extract the electrical characteristics of the OECT plays a crucial role in addressing the challenges described above. If the measurements are not reliable, it will limit the depth and quality of the results, potentially overlooking important and detailed electrical properties of the OECT. This makes it challenging for material scientists to identify areas for improvement in the sensor development process.

At Hochschule Niederrhein, the current measurement setup lacks the flexibility to adapt to the operator's needs, forcing the operator to work around its limitations. Ideally, the system should adapt to the specific demands of the operator and the device under test, not the other way around. This idea leads to the central question of this thesis:

How can a measurement system for a textile-based OECT be developed that is accurate, reliable and efficient to operate? To answer this research question, it is broken down into the following sub-questions:

- What are the typical electrical characteristics of textile-based OECTs?
- What types of electrodes are suitable for connecting the measurement system to the textile-based OECT?
- What are the hardware requirements to accurately control and measure the source-drain current in the OECT?
- What are the software requirements to ensure the system is both compatible with the OECT and user-friendly for the operator?
- How does the performance of the developed measurement system compare to standard high-quality Source Measuring Units (SMUs)?

To streamline the process of answering these questions, clear objectives need to be defined first.

1.3 Objectives

The primary objective of this thesis is to develop a measurement system capable of accurately characterizing the electrical properties of OECTs, with a focus on reliability and user-friendliness. To support this goal, the following sub-objectives are defined:

Obtain a baseline understanding of the electrical characteristics of the textile-based OECT. This will be done by reviewing previous results. These insights will help set the requirements and performance benchmarks for the new measurement system.

After the sub-objective has been addressed, the realization of the software and hardware design for the new measurement system takes place.

With a focus on user-friendliness and adaptability, the hardware system will be based on a microcontroller solution. To control input parameters and display outputs, a dedicated software program must be developed that allows the user to set drain and gate voltages, view real-time current measurements, and save data in a .csv file for further analysis.

The OECT measurement system must first provide reliable electrical interfacing incorporating three electrodes to connect to the gate, drain, and source terminals of the device. To control the operation of the OECT, the system should be able to supply precise voltages in the range of -1V to 1V, with a resolution of at least 0.01V.

Equally important is the ability to accurately measure the current from the drain source. The measuring system needs a high sensitivity in the -20 to 20 mA range. To ensure detection of small signal variations, the system should achieve a current measurement accuracy of at least 90 percent, with an ideal target of 95 percent. In addition, sufficient data collection is necessary to

capture dynamic changes in the OECT behavior. Therefore, a minimum data acquisition rate of 40 Hz is required.

After establishing core functionality, the performance of the system will be validated by comparing its results with those of a high-precision SMU. The target is a maximum measurement deviation of 10 percent, ensuring the accuracy and reliability of the developed system.

1.4 Materials and Methods

To illustrate how the various materials and methods were practically combined, the approach is structured into work packages, each focusing on a specific aspect of the process.

Work Package 1: Understanding and Reproducing the Textile OECT The process began by establishing foundational knowledge on PEDOT:PSS-based OECTs and reconstructing the textile-based OECT described by Brendgen et al [1], [2]. This provided a baseline for subsequent hardware and software development.

Work Package 2: Hardware System Design A dedicated measurement setup was developed with a microcontroller (MCU) at its core. To ensure stable voltage supplies for the DAC and ADC, a low dropout voltage regulator and a switched-capacitor voltage converter were implemented. The analog circuit surrounding the DAC and ADC included a differential amplifier to shift the DAC's output to the OECT's desired range, and a transimpedance amplifier to apply the bias voltage and measure the OECT current. The resulting voltage was adjusted to the ADC's range for accurate digitization. This architecture was mirrored for both channels (Gate and Drain), with data processed on the MCU using Circuitpython.

Work Package 3: Simulation and Validation Component constraints were modeled in LTSpice, allowing the simulated circuit behavior to be compared against theoretical predictions. Once verified, the design was translated into a PCB layout using KiCad 8.0, and manufactured by JLCPCB.

Work Package 4: Firmware and Data Acquisition Collected measurement data was transmitted via Bluetooth to a custom Windows application developed using Flutter. This application provided real-time visualization, parameter adjustment, and data storage capabilities.

Work Package 5: Calibration and Testing The system was calibrated by measuring the differential amplifier output with a multimeter (Peaktech4000) and recording the corresponding DAC input codes, constructing a lookup table implemented in the MCU. The current sensing side was validated by sourcing known currents from an SMU (Keysight B9xxBL) and replacing the OECT with known resistors to compare measured and theoretical values. Finally, system behavior was cross-validated using a J201 N-channel transistor and compared to results from a reference setup.

1.5 Outlook

The upcoming chapters begin with a detailed review of the literature on Organic Electrochemical Transistors. The focus then shifts to the design and implementation of the custom measurement system, starting with an overview of existing approaches used to characterize OECTs, from which a conceptual design is developed.

This design includes a detailed breakdown of the hardware, covering both analog and digital components, as well as the software used to control the system and visualize the collected data. Afterwards, various testing procedures and calibration methods are presented alongside the results, demonstrating the system's accuracy.

The thesis concludes with a reflection on the current design and future outlook, exploring potential improvements and the broader usage of custom-built measurement systems for OECT research.

Chapter 2

The Organic Electrochemical Transistor

This chapter introduces organic electrochemical transistors (OECTs), focusing on their fundamental principles, how they differ from other types of organic transistors, and how they are measured. At a basic level, OECTs control charge flow through an organic semiconductor channel by injecting ions from an electrolyte, with PEDOT:PSS being the most commonly used organic semiconductor[7]–[10].

To fully understand how OECTs function, the following key questions will be addressed:

- What are conductive polymers?
- What are OECTs?
- Why are specific materials chosen for each layer of the device?
- What is the difference between the OECT built at Hochschule Niederrhein (HSNR) and traditional OECTs?
- What electrical characteristics can be measured?

These questions will be explored in the following sections, which examine the device architecture, the function of each layer, and the physical mechanisms that describe the OECT behavior.

2.1 Electrical transport in organic conductive polymers

Before diving into the principles of OECTs, it's essential to first understand organic conductive polymers. Polymers are large molecules composed of repeating units called monomers, as illustrated in Figure 2.1. These monomers are held together by strong covalent bonds formed by the sharing of electrons. In organic polymers, the monomers typically contain carbon atoms, which can bond to each other to form long chains or ring-like structures [7]–[10].

On their own, most organic polymers don't conduct electricity very well, they behave more like insulators or semiconductors. To make them conductive, charge carriers that can move through the material, need to be added. This is done through a process called doping, which introduces extra electrons or creates holes where electrons are missing[11]. The more doping is applied, the more conductive the polymer becomes, ranging from nearly insulating in its natural state to behaving like a metal when heavily doped[8]–[10], [12], [13].

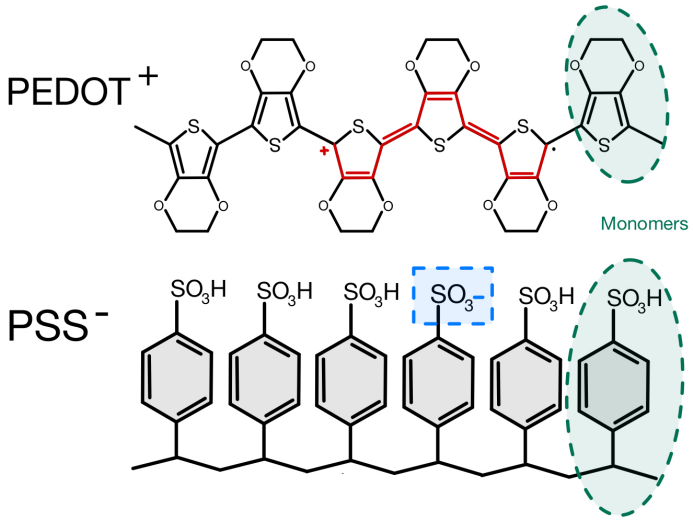


Figure 2.1: *Chemical structure of the two polymers PEDOT and PSS. The red indication represents the positive electrical charge (polaron) on the PEDOT backbone. The blue mark shows the compensating sulfonate ion on the PSS chain, and the green highlight represents an example of a single monomer unit.*

Doping is usually performed through a chemical process known as a redox (reduction-oxidation) reaction [11]. In simple terms, chemical reduction adds electrons to the polymer, while oxidation takes electrons away. This changes the electrical charge distribution along the polymer chain and allows it to conduct electricity. These doping processes can be reversed, so the material can switch between conductive and non-conductive states depending on how the polymer is treated [8]–[10].

A well-known example of a conductive polymer is PEDOT:PSS, illustrated in Figure 2.1. PEDOT:PSS stands for poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) and consists of two components. PEDOT serves as the conductive polymer for charge transport, while PSS functions both as a stabilizer and a dopant. The chemical reaction between both components is described below:

$$\mathrm{PEDOT}^0 + \mathrm{PSS}^- \rightarrow \mathrm{PEDOT}^+ : \mathrm{PSS}^- + e^- \tag{2.1}$$

The PSS component introduces negatively charged sulfonate groups, which dope the PEDOT and therefore enhances its conductivity[11]. As a result of this interaction, PEDOT:PSS can achieve conductivities of up to 1000 S/cm, making it one of the most conductive organic materials known [8]–[10], [12], [13].

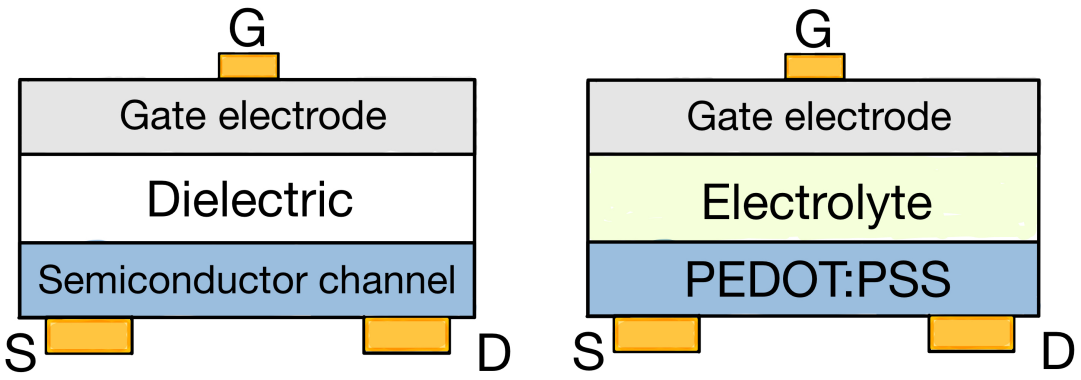
Besides the tunable electrical properties, the polymer structure also provides mechanical flexibility, which is why PEDOT:PSS is used in a wide range of applications. These include biomedical devices, such as bioelectronics and organic electrochemical transistors, as well as flexible and wearable electronics, organic light-emitting diodes (OLEDs), and more [8]–[10], [13]–[15].

2.2 OECT principles

With a basic understanding of how the organic conductive polymer PEDOT:PSS functions and how its conductivity can be tuned, it is possible to further explore its role in the operation of organic electrochemical transistors (OECTs).

2.2.1 General OECT functionality

As previously mentioned in the introduction, OECTs function similarly to traditional transistors in that they can switch and amplify signals. More specifically, OECTs belong to the broader class of electrolyte-gated transistors (EGTs), which also includes devices such as electrolyte-gated organic field-effect transistors (EGOFETs) [10]. As shown in Figure 2.2, the basic structure of an OECT resembles that of a traditional field-effect transistor (FET), or more specifically an organic field-effect transistor (OFET), sharing the same source, drain, and gate configuration. What differentiates EGTs is their use of an electrolyte, rather than a solid dielectric, between the gate and the channel [9]. Depending on the design and application, the electrolyte can be a polymer electrolyte film, an ion gel, or a liquid ionic conductor [2], [16].



(a) Field-Effect Transistor (FET) (b) Organic Electrochemical Transistor (OECT)

Figure 2.2: *Side-by-side layer comparison between a conventional field-effect transistor and an organic electrochemical transistor. (a) shows the layout of a traditional field-effect transistor, where the semiconductor channel can also be organic, resulting in an organic field-effect transistor (OFET). (b) illustrates the basic structure of an organic electrochemical transistor (OECT).*

To understand the behavior of OECTs, it is helpful to compare them to traditional FETs. Both OFETs and OECTs can operate in either enhancement or depletion mode and can be designed with p-type or n-type channels. However, n-type OECTs are less common and generally less stable compared to their p-type counterparts [17]. OECTs most closely resemble depletion-mode p-type OFETs, where a conductive channel exists even at zero gate voltage ($V_g = 0$). When a drain-source voltage (V_{ds}) is applied, a corresponding drain current (I_{ds}) flows. Applying a positive gate voltage ($V_g > 0$) creates a negative space-charge region, depleting the channel of electron holes and reducing I_{ds}. In contrast, a negative gate voltage ($V_g < 0$) enhances conduction by forming a hole-rich layer, thereby increasing I_{ds} [2], [9], [10].

In OECTs however, the gating mechanism differs significantly from that of OFETs and EGOFETs. OECTs benefit from the ability of ions to penetrate the organic semiconductor, altering its doping level and therefore its bulk conductivity [2], [8], [9], [17]. The resulting gate-channel capacitances can be over three orders of magnitude higher than those achieved with advanced high-k dielectrics. This unique property of OECTs enables low-voltage operation ($\pm 1V$) and strong signal amplification[10], [18].

Figure 2.3 shows how OECTs work in both enhancement and depletion modes through three different operating states. In the first state ($V_g = 0$), no ion movement occurs. As a result, the conductive polymer remains in its original state as fabricated (discussed in Chapter 2.1). In enhancement mode, a negative V_g is applied, triggering ion movement within the electrolyte.

Anions are driven into the organic polymer channel, while cations migrate toward the gate electrode. As anions enter the polymer, they further dope the PEDOT, increasing its conductivity (I_{ds}). In depletion mode, a positive V_g is applied, attracting anions toward the gate and driving cations into the conductive polymer channel. This ion movement causes a reduction of the PEDOT, effectively dedoping the channel. As a result, the channel's conductivity decreases, leading to a reduction in I_{ds} [1], [2], [8]–[10].

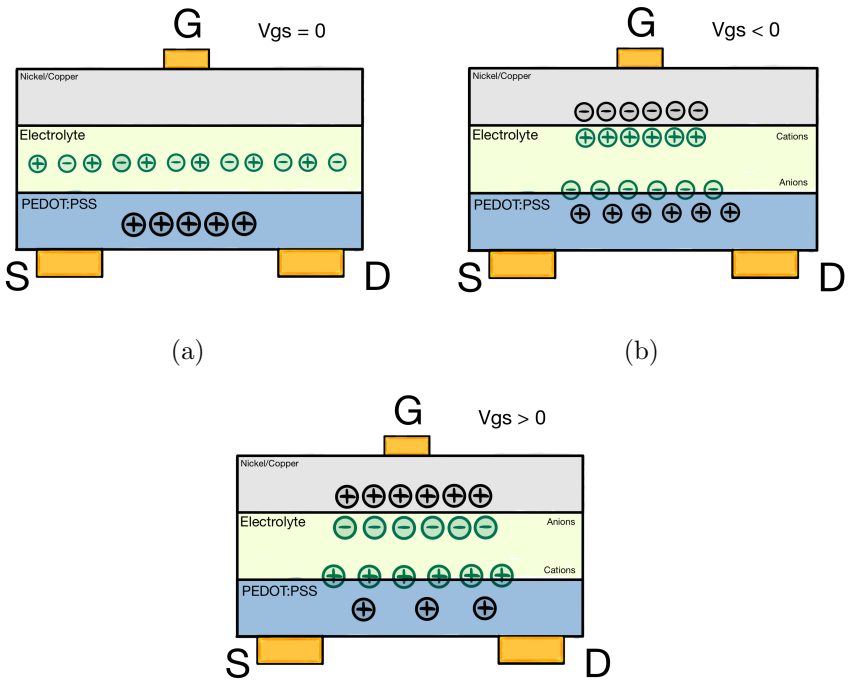


Figure 2.3: *Illustration of the three operating modes of an OECT with a static positive V_{ds}. The electrolyte contains both anions and cations. (a) The pristine state, where no gate voltage (V_g) is applied, resulting in no ion movement. (b) Enhancement mode, where a negative V_g pulls cations toward the gate electrode and pushes anions into the PEDOT:PSS, increasing channel conductivity. (c) Depletion mode, where a positive V_g attracts anions to the gate and drives cations into the PEDOT:PSS, reducing channel conductivity.*

2.2.2 Organic conductive polymer inside a OECT

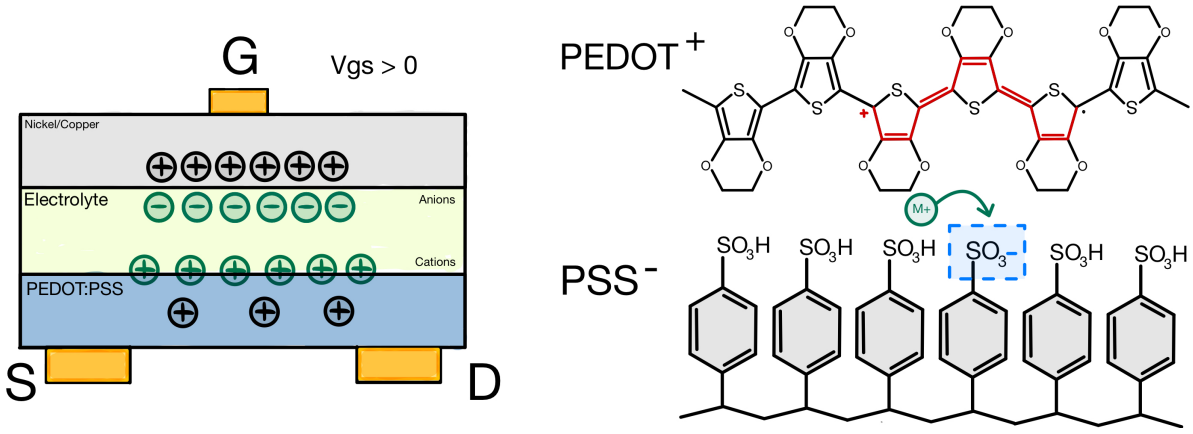
This section provides additional information on the behavior of the conductive polymer within an OECT.

Starting with depletion mode, when a positive V_g is applied, cations (e.g., M^+) from the electrolyte are pushed into the organic polymer. As illustrated in Figure 2.4(b), these cations move towards negatively charged sulfonate groups (SO_3^-) of PSS [2], [10], [19].

This ionic interaction introduces an electrochemical reduction reaction that leads to the dedoping of the PEDOT polymer. In its doped (oxidized) state, PEDOT exists as $PEDOT^+$ to maintain charge balance with the negatively charged PSS^-. When a cation and an electron are introduced, PEDOT is reduced to its neutral (non-conductive) form, as described by the redox reaction:

$$PEDOT^+ : PSS^- + M^+ + e^- \xrightarrow{\text{reduction}} PEDOT^0 : PSS^- : M^+ \tag{2.2}$$

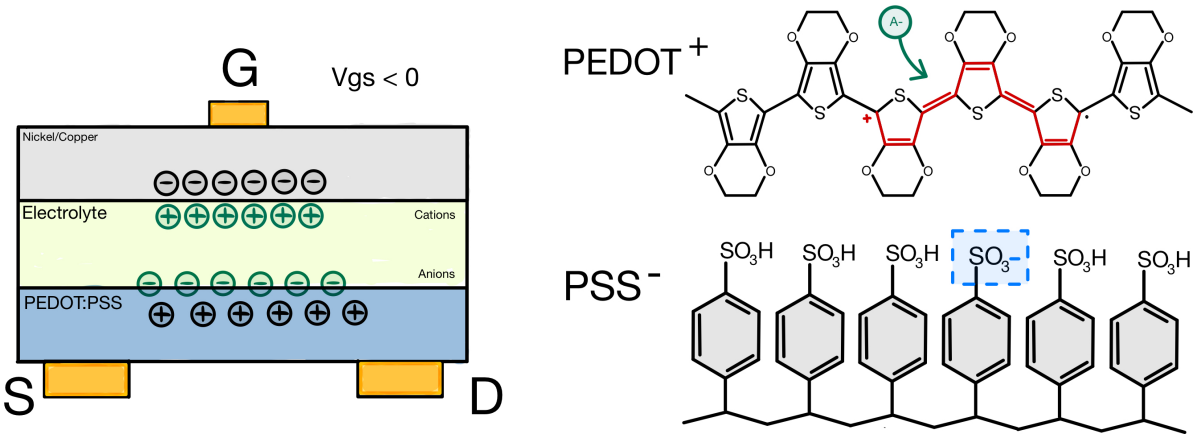
This process decreases the density of positive charge carriers (polarons) in the polymer backbone, thereby reducing the channel's conductivity and decreasing the I_{ds} [2], [10], [19].



(a) (b)

Figure 2.4: *(a) Representation of an OECT device in depletion mode. (b) Chemical structure of the polymers PEDOT and PSS, showing a cation (M^+) moving in to neutralize the negatively charged sulfonate group (SO_3^-) on the PSS chain.*

In enhancement mode, the opposite process occurs. When a negative V_g is applied, anions (e.g., A^-) from the electrolyte are driven into the conducting polymer channel. As shown in Figure 2.5(b), these anions enter the PEDOT:PSS substrate and behave similarly to the PSS^- counterions already present in the polymer.



(a) (b)

Figure 2.5: *(a) Representation of an OECT device in enhancement mode. (b) Chemical structure of the polymers PEDOT and PSS, showing an anion (A^-) entering the polymer, doping the PEDOT in the same way the SO_3^- ion can dope the PEDOT.*

The entry of anions introduces an oxidation reaction that converts neutral PEDOT ($PEDOT^0$) back to its doped positively charged form ($PEDOT^+$), increasing the density of the charge carriers and enhancing the conductivity of the polymer. This can be described by the following redox equation:

$$PEDOT^0 + A^- \xrightarrow{\text{oxidation}} PEDOT^+ : A^- + e^- \tag{2.3}$$

This doping of the polymer effectively opens the channel, resulting in an increased drain-source current (I_{ds}).

2.2.3 Biosensing with OECTs

OECTs are widely used in biosensing applications due to their unique structure and operation. With an electrolyte layer containing mobile ions and a channel material that responds electrochemically to these ions, OECTs are highly sensitive to changes in their environment. This sensitivity makes them well-suited for detecting biological signals. OECTs have been employed in a variety of biosensing applications, including glucose sensing [1], [2], [10], [14], nucleic acid detection [20], sweat analysis with ion-selective detection [21], and the monitoring of redox-active molecules such as adrenaline, dopamine, and ascorbic acid [22].

In redox-based sensing, added analytes undergo electrochemical oxidation at the channel–electrolyte interface when a gate voltage is applied, releasing electrons and protons into the surrounding medium. The generated protons (H^+ ions) interact with the PEDOT:PSS channel, leading to dedoping of the polymer and a measurable decrease in drain current (I_{ds}). This sensing strategy typically requires no additional modifications to the OECT architecture, as redox-active molecules can directly participate in electron transfer processes at the channel interface. Gualandi et al. [22] demonstrated this principle using a textile-based OECT for the real-time detection of adrenaline. Upon oxidation, adrenaline produced protons that modulated the channel conductivity, resulting in a current response proportional to the analyte concentration and enabling sensitive detection on a textile substrate.

To achieve glucose sensing, modifications are made to the electrolyte layer of the transistor. As mentioned earlier, the electrolyte is an ionic medium, meaning both the concentration and the types of ions present can be controlled and modified. For glucose detection, the electrolyte is modified by incorporating a specific enzyme, glucose oxidase (GO_x) [2], [19].

As shown in the reaction below, the enzyme catalyzes the reaction between glucose and oxygen, producing gluconic acid and hydrogen peroxide. During this process, protons are also released into the electrolyte, thereby changing the local ionic environment near the gate electrode and/or the channel [2], [19].

$$\text{Glucose} + \text{O}_2 + \text{H}_2\text{O} \rightarrow \text{Gluconic acid} + \text{H}_2\text{O}_2 + 2\text{H}^+ \tag{2.4}$$

The increase in proton concentration affects the electrochemical potential at the electrolyte interface. This local change leads to the dedoping of the PEDOT:PSS channel, resulting in a measurable decrease in the drain current (I_{ds}) [2], [19].

OECTs can be modified for detection of other biological targets, including deoxyribonucleic acids (DNA) [20], analytes in sweat, with a focus on ion-selective detection [21], and redox-active molecules like adrenaline, dopamine, and ascorbic acid [22]. OECT architectures can be modified in ways that go beyond adding enzymes to the electrolyte interface. One of such example is the ion-selective organic electrochemical transistor (IS-OECT), which incorporates an ion-selective membrane (ISM) to control which ions from the electrolyte can reach the OECT channel. This enhances the device's selectivity in complex biological fluids such as sweat, where multiple ionic species are present. The ISM allows only the target ion (e.g., K^+ or Na^+) to pass through and

interact with the PEDOT:PSS channel, resulting in a selective and specific electrical response [23].

For instance, Coppedé et al. [21] demonstrated a textile-based IS-OECT for sweat monitoring by integrating an ion-selective membrane directly over the PEDOT:PSS channel. The membrane was composed of polymeric ion-selective materials, such as polyvinyl chloride (PVC) combined with small molecules designed to selectively bind specific ions (ionophores). In this configuration, the electrolyte itself contains the ions to be detected (analyte).

To further enhance performance, IS-OECTs can be modified by introducing an additional inner electrolyte layer between the ISM and the PEDOT:PSS channel. This internal layer facilitates uniform ion transport across the entire channel surface. In this layered architecture, the gate electrode interacts with the analyte (sweat), driving ions toward the ISM. The ISM selectively permits only the target ions to pass through into the inner electrolyte, which then delivers them to the channel for detection [23]. However, modifying OECTs to detect specific ions or biomolecules presents significant challenges. For accurate and selective detection, the device must be carefully engineered to stabilize the ionic environment surrounding the electrolyte interface and the PEDOT:PSS channel. This ensures that any signal change is solely the result of controlled ion movement [1], [2], [10], [14], [20], [22]. In enzyme-modified OECTs, more complexity arises due to the need to maintain enzyme activity and structural integrity, which can be affected by pH, temperature, and the composition of the surrounding medium. Similarly, in ion-selective sensing, the integration of ion-selective membranes must be precisely tuned to avoid interference from non-target ions, maintain long-term stability, and ensure compatibility with the biological fluids of interest. When transitioning to real-world applications involving complex fluids such as sweat, saliva, or interstitial fluid, factors such as variable ionic composition, hydration state, and biofouling further complicate sensor reliability. These considerations highlight the critical importance of interface engineering and material optimization when adapting OECTs for diverse biosensing applications [21], [23].

2.2.4 Electrode materials

In addition to the channel and electrolyte, which have already been discussed, the architecture of an OECT also includes electrodes. These electrodes can be specifically selected or modified to suit the requirements of the device [6], [24], [25].

An OECT consists of three electrodes: the gate, drain, and source. For the source and drain electrodes, highly conductive metals such as gold (Au), silver (Ag), and platinum (Pt) are commonly used. These materials are chosen for their excellent electrical conductivity, which ensures efficient transport of electrical signals between the external circuitry and the transistor channel [24], [25]. Gold is often preferred due to its chemical stability and resistance to oxidation, making it well-suited for long-term use in aqueous environments. Silver offers a cost-effective alternative with high conductivity, although it is more fragile to oxidation. Platinum is typically used when long-term chemical stability and durability are required in reactive conditions [24], [25]. The gate electrode, however, serves a different role. Instead of just conducting electrons, the gate modulates the ionic environment around the channel material. Therefore, materials like silver/silver chloride (Ag/AgCl) are frequently used for the gate. Ag/AgCl electrodes offer a stable and well-defined electrochemical potential [24], [25].

While the electrode materials discussed above dominate OECT research [24], [25], ongoing research has explored alternatives that go into the direction to meet the demands of flexibility, biocompatibility, and scalable fabrication [21]. Particularly in the context of wearable and flexible electronics, researchers have investigated the use of conducting polymers and metal-coated textiles [1], [2]. For instance, in fully textile-based OECTs, conductive threads or printed inks have been employed as functional electrodes, enabling direct integration into textile [22]. These developments highlight how electrode selection can be adapted to suit the mechanical and environmental requirements of specific applications.

2.2.5 HSNR textile-based OECT

This section presents the textile-based OECT developed at HSNR, focusing on the materials used, the fabrication process, and the resulting device performance. Various textile-based OECTs have been fabricated at HSNR by testing different materials for both the electrodes and the channel. Brendgen et al. [11] explored multiple textile substrates as the foundation for the PEDOT:PSS channel, including variations in the number and configuration of PEDOT:PSS layers. Additionally, Brendgen also investigated alternative electrolyte layers and gate materials, such as nickel/copper and tin-copper ripstop fabrics [1], [2].

The following subsection explains the materials and fabrication methods used to produce the textile-based OECTs developed at HSNR.

Materials and methods

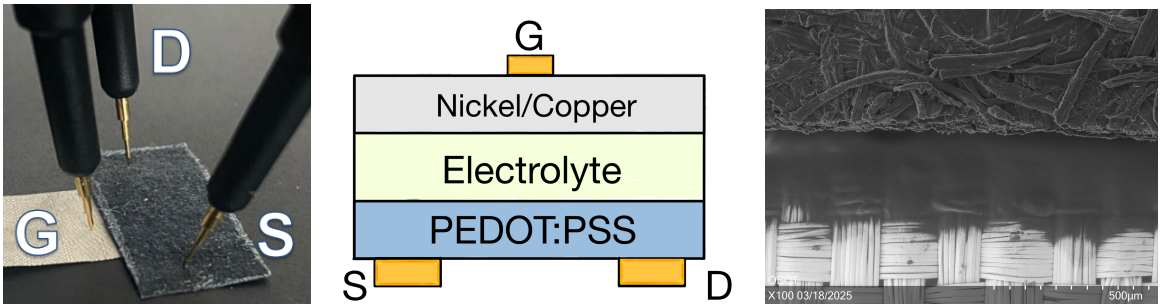
The fabrication process starts with the preparation of a PEDOT:PSS solution, which includes dimethyl sulfoxide (DMSO) as a secondary dopant and glycerol to enhance water retention and conductivity. This solution is spray-coated in multiple layers onto a biodegradable, cellulose-based filter paper, which serves as the porous substrate. After each layer is applied, the substrate is dried at 60°C to ensure proper absorption and adhesion of the conductive polymer [1], [2], [11]. For the gate electrode, a nickel/copper-coated ripstop fabric is used. This textile is lightweight, flexible and conductive, making it well-suited for integration into a flexible device [1], [2]. The electrolyte layer is prepared by first dissolving hydroxyethyl cellulose (tylose) in distilled water, then blending it with ECG contact gel in a 1:1 ratio. Glycerol and lithium chloride are added to enhance moisture retention and ionic conductivity. The resulting gel mixture is homogenized and defoamed prior to application [1], [2].

Device assembly is carried out by applying the electrolyte onto the gate fabric using a hand squeegee. While the electrolyte is still wet, the PEDOT:PSS-coated nonwoven substrate is placed on top. The assembled layers are then dried at 60°C to solidify the electrolyte and bond all components together. After drying, individual OECTs are cut to a final size of 3cm x 1cm [1], [2]. This method results in the fabrication of a textile-based OECT, as shown in Figure 2.6(a). Here, gold-plated probes are placed on the device to establish electrical contact with the gate, source, and drain terminals.

Previous Results

The functionality of the textile-based OECT was successfully demonstrated by Brendgen et al., who tested the device under varying V_{ds} and V_{gs} conditions [1], [2]. The resulting I_{ds} measure-

ments confirm the behavior of a p-type OECT and with I_{ds} values within the milliampere to microampere range. It is also noteworthy that I_{ds} values vary between measurements and/or across devices, reflecting inherent variability in measurement conditions and/or device performance. This highlights the importance of a robust measurement platform to ensure consistent data collection and to accurately capture the variability among differently fabricated devices. The development of such a measurement system will be described in Chapter 3: Measuring System Design and Implementation.



(a) (b) (c)

Figure 2.6: *Textile-based OECT developed at Hochschule Niederrhein. (a) Photograph of the fabricated device. (b) Schematic cross-section showing the layer configuration, with the gate (G) electrode placed on top of the ripstop fabric and the drain (D) and source (S) electrodes on the PEDOT:PSS substrate. (c) Scanning electron microscope (SEM) image showing the structure of the textile-based device.*

2.3 Physical-based model theories

To better understand the operation and performance of OECTs, it is important to explore the physical principles and models that describe their behavior. By using the following model, expected results can be simulated and analyzed, providing insight into the typical behavior of an OECT [9], [10], [26]–[29].

A widely recognized model describing OECT operation was proposed by D. A. Bernards and G. G. Malliaras (B-M) [26]. As illustrated in Figure 2.7, this model is made of two main components: an electronic model and an ionic model. The electronic model describes hole transport within the semiconducting channel, while the ionic model accounts for the migration of charged ions in the electrolyte [9], [27]–[29].

The electronic behavior of the channel is described by the generalized Ohm's law:

$$J(x) = q\,\mu\,\rho(x)\,\frac{dV(x)}{dx} \tag{2.5}$$

where:

- $J(x)$ is the current density at position x,
- q is the elementary charge,
- μ is the hole mobility,
- $\rho(x)$ is the local hole concentration,
- $\frac{dV(x)}{dx}$ represents the electric field along the channel.

The coordinate x lies along the longitudinal axis of the channel, as shown in Figure 2.7.

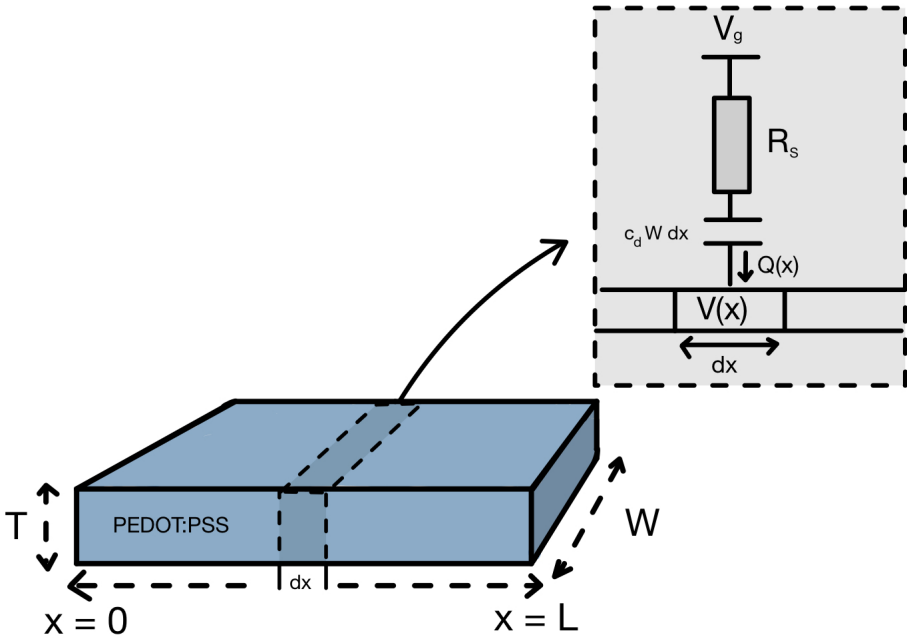


Figure 2.7: *Schematic representation of the B-M model for OECTs, highlighting the electronic and ionic components in the striped region. The geometry of the semiconducting channel is defined by its thickness (T), length (L), and width (W).*

Each cation neutralizes the charge of a hole in the polymer, effectively reducing the doping level of the semiconductor [9], [26]–[29]. This process alters the hole concentration and can be described by the following expression:

$$\rho = \rho_0 \left(1 - \frac{Q}{qV\rho_0}\right) \tag{2.6}$$

where:

- ρ_0 is the initial hole concentration in the absence of a gate voltage ($V_G = 0$),
- V is the volume of the semiconducting film,
- Q is the total charge of the injected cations.

The ionic part of the model describes the transport of cations within the electrolyte toward the channel and can be represented by a resistor and a capacitor connected in series. The resistor accounts for the ionic conductivity of the electrolyte, which reflects its ionic strength, while the capacitor represents the polarization occurring at the channel–electrolyte and gate–electrolyte interfaces [9], [26]–[29].

The transient response of this ionic component to an applied gate voltage resembles the behavior of a charging capacitor, described by the equation:

$$Q(t) = Q_{ss}\left[1 - \exp\left(-\frac{t}{\tau_i}\right)\right] \tag{2.7}$$

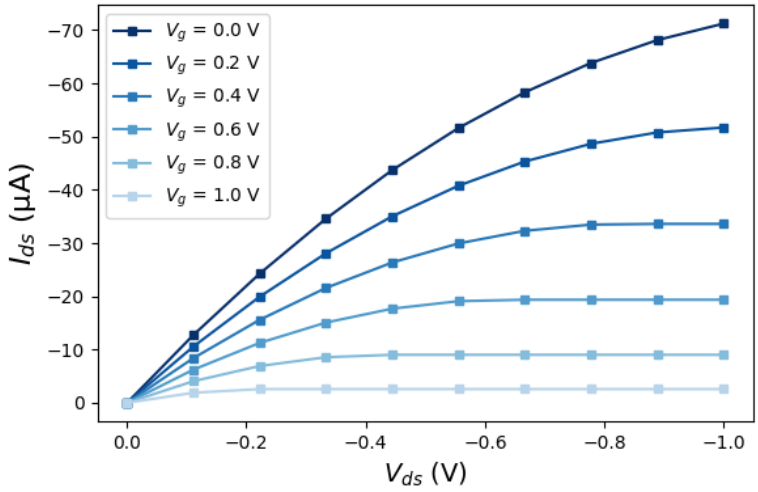


Figure 2.8: *Transfer characteristic curve obtained from equation 2.9 with a biased V_G while V_{ds} being varied.*

where:

- $Q(t)$ is the time-dependent charge,
- $Q_{ss} = C_d \Delta V$ is the steady-state charge,
- ΔV is the voltage across the electrolyte,
- $\tau_i = R_s C_d$ is the ionic transit time constant.

Since the capacitance C_d depends on the area of the device, it is often expressed as:

$$C_d = c_d A \tag{2.8}$$

where c_d is the specific capacitance per unit area, and A is the device area. For simplicity, the B-M model neglects the potential and concentration dependence of the double-layer capacitance and a constant value for c_d is assumed in the model [26].

An OECT can be characterized by studying its two main operating regimes: steady-state and transient behavior. This section first focuses on the steady-state response, which reflects the de-doping process occurring throughout the polymer [9], [26]. The behavior can be seen in Figure 2.8 and is described by the following equation:

$$J(x) = q\mu\rho \left(1 - \frac{V_G - V}{V_{DS}}\right) \frac{dV(x)}{dx} \tag{2.9}$$

The interpretation of this equation depends on the applied drain-source voltage V_{DS} in relation to the gate voltage V_G:

- When $V_{DS} > 0$ and $V_{DS} < V_G$, de-doping occurs uniformly throughout the entire polymer film. In this regime, the local potential remains above the gate voltage along the channel [26].
- As V_{DS} increases beyond V_G, the system enters the so-called emptying condition. De-doping now occurs only in regions where the local potential $V(x)$ falls below the gate voltage. This

leads to spatially selective modulation of the doping profile [26].

- When V_{DS} reaches the saturation voltage V_{DSsat}, a critical condition is met. At this point, the polymer becomes fully de-doped at the drain end, meaning the local density of injected cations equals the intrinsic doping concentration of the semiconductor. Beyond this point, further increases in V_{DS} do not affect the current, resulting in current saturation [26].

To analyze the transient behavior of the OECT model the following equation is used:

$$I(t, V_g) = I_{ss}(V_g) + \Delta I_{ss} \left(1 - f\frac{\tau_e}{\tau_i}\right) \exp\left(-\frac{t}{\tau_i}\right) \tag{2.10}$$

where:

- $I_{ss}(V_g)$ is the steady-state drain current at a gate voltage V_g,
- $\Delta I_{ss} = I_{ss}(V_g = 0) - I_{ss}(V_g)$ is the change in steady-state current,
- τ_i is the ionic time constant,
- τ_e is the electronic time constant,
- f is a scaling factor.

This equation leads to two types of transient responses, illustrated in Figure 2.9:

- Monotonic decay ($\tau_i > f\tau_e$): The current gradually approaches the steady-state value. This indicates that the electronic response is fast enough to be considered instantaneous [26].
- Spike-and-recovery ($\tau_i < f\tau_e$): The current initially spikes before settling, revealing that the ionic response dominates the transient behavior [26].

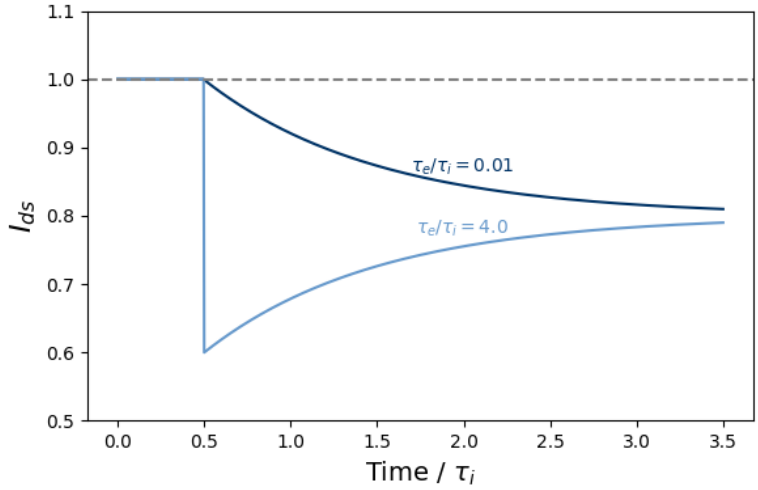


Figure 2.9: *Transient response types of an OECT based on the relative values of τ_i and τ_e with I_{ds} normalized. Where $\frac{\tau_e}{\tau_i} = 0.01$ is the monotonic transient response and $\frac{\tau_e}{\tau_i} = 4.0$ is the spike-and-recovery transient response.*

To further illustrate the modeled transient behavior, a pulse response simulation is shown in Figure 2.10. In this example, a gate voltage V_G is applied at 20 s and removed at 40 s. The first graph shows a monotonic response, while the second graph shows a spike-and-recovery response.

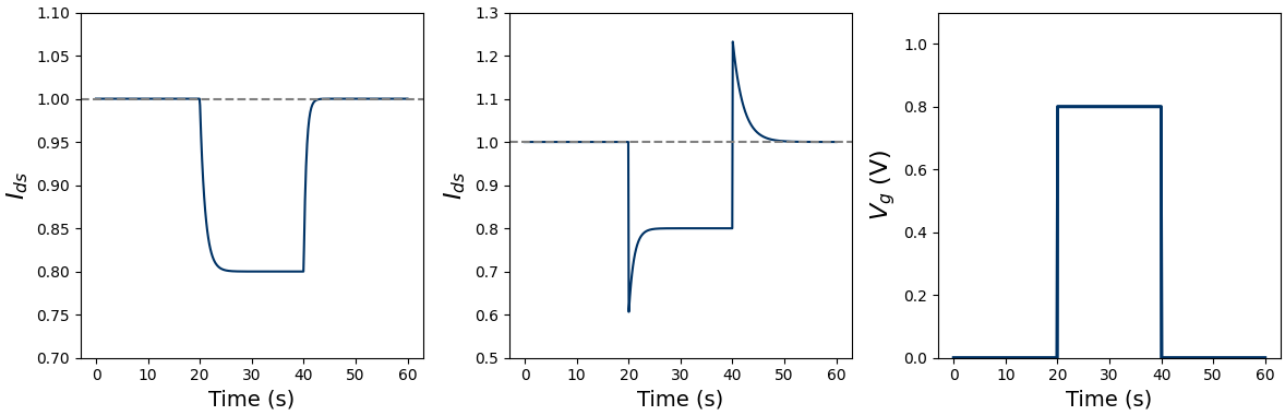


Figure 2.10: *Pulse response of the B-M OECT model with I_{ds} normalized: (left) monotonic response; (middle) spike-and-recovery response; (right) block pulse V_G which is applied between 20 s and 40 s.*

Another interesting model is presented by Gentile et al. (2020) [27], where the behavior of the gate-source current (I_{gs}) is described. When a positive gate voltage is applied, a current flows through the electrolyte from the gate to the channel. The behavior of I_{gs} may provide insights into the wettability of the electrolyte, offering additional information beyond what I_{ds} alone reveals. This current, I_{gs}, behaves opposite to the drain-source current (I_{ds}) and is typically 10 to 50 times smaller than I_{ds} [9], [27], [29]. Taking this into account in the context of the previously discussed B-M model, the expected transient pulse responses I_{gs} and I_{ds} can be observed in Figure 2.11.

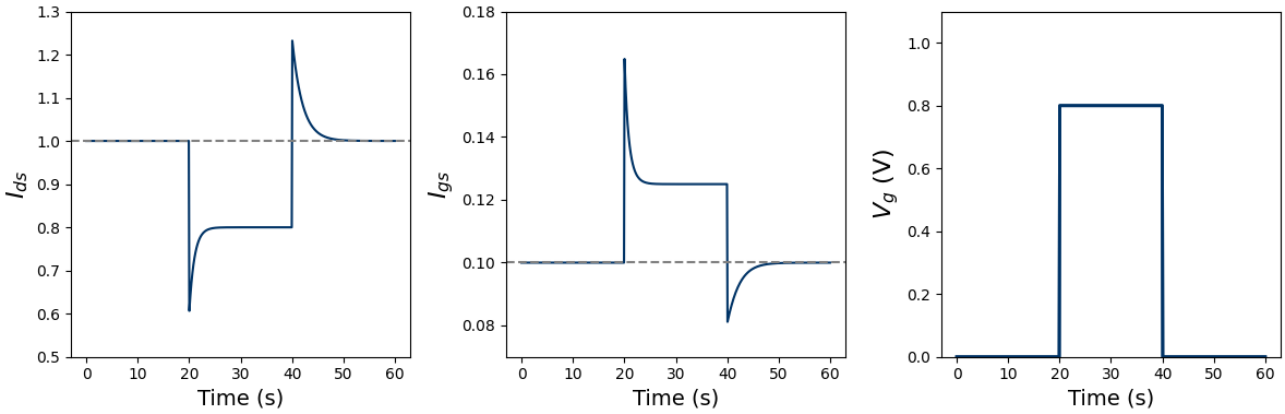


Figure 2.11: *Pulse response of the B-M OECT model with a look at I_{gs} and I_{ds} normalized: (left) spike-and-recovery response of I_{ds}; (middle) spike-and-recovery response of I_{gs}; (right) block pulse V_G which is applied between 20 s and 40 s.*

2.4 Conclusion

This chapter has outlined the fundamental principles of OECTs, including their operation, characteristics, and potential applications. Although the current device at Hochschule Niederrhein proofs stable p-type OECT behavior, challenges remain, particularly the lack of reproducibility in I_{ds} values across sensors. To address this, the described models such as the Bernards-Malliaras (B-M) model are valuable for predicting general device behavior, even if precise numerical comparisons are not possible. These models support both device development and interpretation of measurements. Although the main goal of this thesis is to develop a system to measure I_{ds},

this chapter also highlighted the importance of monitoring I_{gs}, which could reveal additional information about ionic interactions. These insights are especially relevant for biosensing and electrolyte performance.

With this foundational understanding in place, the next chapter introduces the design and implementation of a custom measurement system for the electrical characterization of OECTs.

Chapter 3

Measuring System Design and Implementation

3.1 Introduction

The textile-based OECT currently under development at Hochschule Niederrhein remains in an early stage of research. At this point, existing measurement methods lack the reliability and control needed to properly characterize the device, limiting a deeper understanding of its behavior. To address this challenge, this thesis focuses on the development of a dedicated measurement system engineered to the specific requirements of textile-based OECTs. The system must be capable of accurately measuring the drain-source current (I_{ds}) while reliably applying the necessary drain and gate voltages. Additionally, it should be efficient and user-friendly, allowing material scientists to interact with the sensor effectively.

Building on the previous chapter, which introduced OECTs and their measurable electrical outputs, this chapter presents the complete measurement system developed as part of this thesis. It begins with a review of conventional methodologies for characterizing OECTs, followed by an overview of customized measurement setups implemented by other research groups. Next, the conceptual design of the system developed in this work is introduced, highlighting its functional building blocks. Each block is then discussed in detail, including the specific components selected for implementation and their roles within the system.

3.1.1 General lab equipment

The conventional setup for powering and measuring the OECT is shown in Figure 3.1. In this configuration, both the gate and drain are supplied with voltage, and the drain current (I_{ds}) is measured using a multimeter.

At Hochschule Niederrhein (HSNR), two DC power supplies (Siglent SP85081X) were used to manually apply the required drain and gate voltages. A PeakTech 4000 multimeter was placed in series with the drain power supply to measure I_{ds}. Data was then collected via serial communication using the multimeter's software, with a sampling rate of 5 Hz [1], [2].

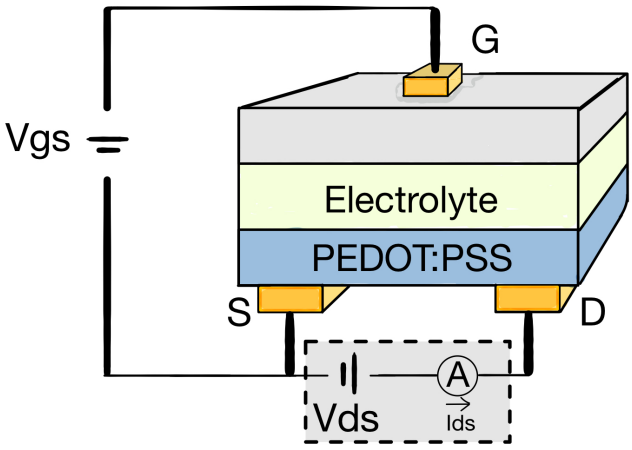


Figure 3.1: *General OECT measuring setup. V_{gs} is the gate-source voltage supply, V_{ds} the drain-source voltage supply, and A represents the ammeter (or multimeter) used to measure current.*

Source-Measuring Unit

The key difference between a typical OECT characterization setup and the one used at HSNR lies in the instrumentation. High-end setups use Source-Measure Units (SMUs) controlled via a customized or factory program. These SMUs can simultaneously source voltage and measure current, providing more accurate and automated control [5], [19], [26].

Most SMUs apply a voltage and measure current using an internal precision shunt resistor [30], [31]. This resistor is placed in series with the device under test (DUT), in this case an OECT, and the current is calculated by measuring the voltage drop across it, as shown in Figure 3.2, and applying Ohm's law:

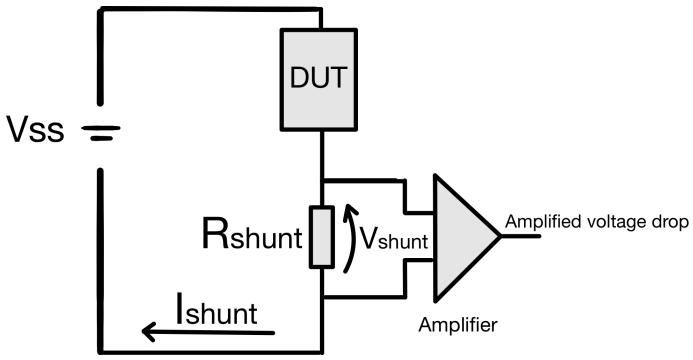


Figure 3.2: *Basic principle of current measurement using a shunt resistor inside an SMU. V_{ss} is the supply voltage, DUT is the device under test, R_{shunt} is the shunt resistor, V_{shunt} is the voltage drop across the resistor, and I_{shunt} is the current flowing through the resistor and the DUT.*

$$I = \frac{V}{R} \tag{3.1}$$

This voltage drop is often amplified to improve measurement accuracy [30], [31]. Modern SMUs, such as those from Keysight and Ossila, include multiple internal shunt resistors to cover a wide range of current levels. For instance, the Ossila SMU supports currents from ±200mA down to ±20µA, with measurement resolutions as low as 100pA. These devices often use auto-ranging to switch between shunt resistors, ensuring optimal accuracy across different current ranges [30], [31]. This approach is standard in precision measurement setups and is particularly useful for

characterizing low-current devices such as OECTs [5], [19], [26], [30], [31].

3.1.2 Customized OECT measuring systems

This section provides a brief overview of the key components used in existing custom-built OECT measurement setups, which serves as the basis for developing a dedicated measuring system in this thesis.

Previously, custom-built measurement setups such as the Universal Wireless Electrochemical Detector (UWED) have demonstrated the possibility of compact, wireless measurement units. The UWED combines a microcontroller with Bluetooth Low Energy (BLE), and integrates a 16-bit digital-to-analog converter (DAC), a transimpedance amplifier (TIA) for current measurement, and a 16-bit analog-to-digital converter (ADC). It also incorporates multiple amplifiers for noise filtering. The system is powered by a LiPo battery connected to a low-dropout voltage regulator (LDO) [32].

Another custom device, specifically developed for OECT measurements, features wireless communication with a smartphone. In this setup, a shunt resistor is used for current sensing. The voltage drop across the resistor is amplified and then read by an analog-to-digital converter [33].

A wearable device was developed by Tian et al. (2022), named the Personalized Electronic Reader for Electrochemical Transistors (PERfECT). This setup is capable of measuring both the transfer and transient behavior of OECTs with a resolution and sampling rate comparable to conventional laboratory equipment [3]. The system features a microcontroller with BLE support and a triple DAC to control the drain, gate, and source voltages. To measure I_{ds}, a transimpedance amplifier is used, with its output digitized by an ADC. In a later version (2024), the device was further improved with the integration of a multiplexer, enabling sequential measurements of multiple OECTs [34].

Lastly, the behavior of an OECT was simulated along with two readout circuits, which were later tested experimentally as part of a master's thesis. The gate and drain were powered using standard laboratory equipment, while the drain current was measured using two different approaches: one using a transimpedance amplifier and the other a gyrator [8].

The literature review of existing measurement setups has provided valuable insights into the design of custom-built systems for OECT characterization. While it is likely that additional solutions exist beyond those examined, the reviewed systems offer a foundation for the development of a dedicated measurement platform. Many of these microcontroller-based setups primarily focus on measuring the drain current using a transimpedance amplifier (TIA). However, none were found to simultaneously measure the gate current (I_{gs}) using a second TIA. Although this thesis aims to develop a system for accurately measuring I_{ds}, the previous chapter also highlighted the importance of capturing I_{gs}. Monitoring I_{gs} provides insight into ionic interactions at the gate electrode, which is particularly relevant for applications such as biosensing and assessing the electrolyte's wettability [27].

3.1.3 Conceptual design of the measuring system

Based on the existing OECT measurement systems discussed in the previous sections, a conceptual design was developed that incorporates the essential components required for accurate and

reliable measurements. This design is illustrated in Figure 3.3. At the core of the system is a microcontroller unit (MCU), which serves as the central hub for control and communication. Since both the gate and drain voltages ($-1\,\mathrm{V}$ to $1\,\mathrm{V}$) need to be controlled independently, two DACs are incorporated into the system. The currents flowing through the drain-source and gate-source terminals also need to be measured. To achieve this, two TIAs are used to convert the positive and negative milliampere currents into measurable voltages. These voltages are then digitized using an ADC. As both signals must be captured simultaneously, a multi-channel ADC is preferred. For wireless communication with the user interface application, Bluetooth Low Energy is integrated into the system. This allows real-time data transmission to a computer or mobile device.

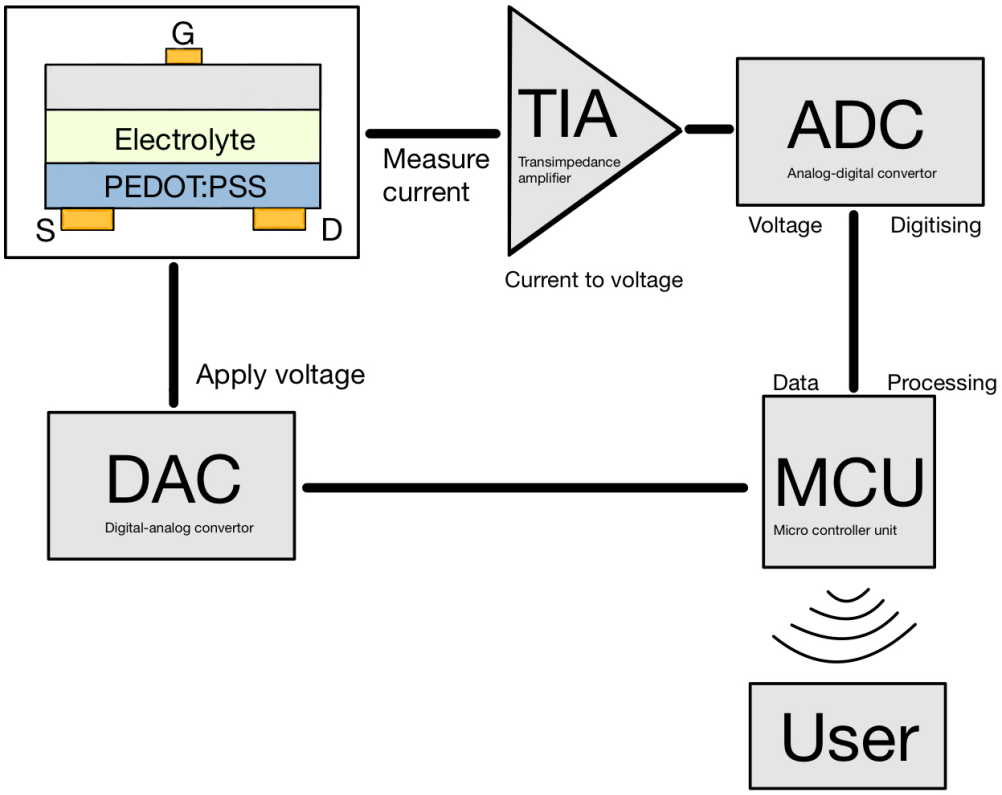


Figure 3.3: *Conceptual design of the OECT measuring system.*

These components can be categorized into digital and analog hardware domains. The DACs, ADC, and MCU form the digital subsystem, while the TIAs belong to the analog domain. The following sections discuss these subsystems and their corresponding components in greater detail.

3.2 Hardware design

3.2.1 Digital hardware

The digital hardware forms the backbone of the control and data processing system. It is responsible for generating voltage signals, collecting measured data and managing communication with the user interface. This section covers the three key digital components of the measuring system: the microcontroller, the digital-to-analog converter, and the analog-to-digital converter.

Microcontroller

The microcontroller unit acts as the central processing and coordination element of the system. It is responsible for configuring and controlling the DACs and ADC and for handling wireless communication via Bluetooth. Furthermore, it runs the firmware that defines the measurement protocol and ensures synchronization between signal generation and data collection. The MCU can also supply voltages to components, two typically options are 3.3 V or 5 V, depending on its specifications. MCUs can be selected based on criteria such as processing capability, number of I/O pins, communication interfaces, and power efficiency [35], [36]. Microcontrollers are available in various packages and sizes, allowing one to choose the one that best matches the specific requirements of a given application.

Digital-to-Analog Converter

The digital-to-analog converter generates the voltage signals required to control the gate and drain terminals of the OECT. The MCU sends digital control values to the DAC, which then outputs the corresponding analog voltages.

One of the most important specifications of a DAC is its resolution, expressed in bits. The resolution determines how finely the output voltage can be adjusted. For example, a 12-bit DAC can represent $2^{12} = 4096$ discrete voltage levels, while a 16-bit DAC provides $2^{16} = 65,536$ levels. Higher resolution allows for finer voltage control [35], [36].

Most DACs are designed to produce only positive output voltages, typically ranging from 0 V up to the supply voltage (such as 3.3 V or 5 V). Because of this, generating negative voltages often requires additional circuitry. Other important factors when choosing a DAC include its output voltage range, how accurately it can follow the desired signal (linearity), how stable the output remains over time, and the communication protocol it uses to connect with the MCU, such as I^2C [35], [36].

Analog-to-Digital Converter

The analog-to-digital converter converts the analog voltage signals into digital values. The MCU then reads these digitized values from the ADC.

As with the DAC, one of the most important specifications of an ADC is its resolution, expressed in bits. The resolution determines how accurately the ADC can represent the input voltage. For example, a 12-bit ADC can distinguish $2^{12} = 4096$ discrete levels, while a 16-bit ADC provides $2^{16} = 65,536$ levels. Higher resolution enables the detection of smaller changes in the measured signals [35], [36].

Most ADCs are designed to operate with unipolar input ranges, typically between 0 V and the supply voltage (e.g., 3.3 V or 5 V). As such, any signal from the analog front-end, which might include negative voltages due to the OECT's demands, must be level-shifted or otherwise conditioned to remain within the ADC's acceptable input range. Other key considerations for ADC selection include the number of input channels, input voltage range, sampling rate, and the communication protocol used to interface with the MCU, such as I^2C [35], [36].

I²C Communication Protocol

Inter-Integrated Circuit (I^2C) is a widely used serial communication protocol that enables multiple digital devices to communicate over the same two wires: a data line (SDA) and a clock line (SCL). It supports multiple devices on the same bus by assigning each one a unique address. I^2C is especially suitable for short-distance, low-speed communication between components on the same board [35], [36].

The SDA and SCL lines must have external pull-up resistors (typically 1–10 kΩ) because I^2C is an open-drain bus: devices can only pull the line low and cannot drive it high. The resistors ensure that the lines return to a high logic level when not actively driven low, enabling proper logic transitions [35], [36].

In the context of this measuring system, I^2C is used to send configuration commands from the microcontroller to the DAC and ADC, specifying the desired output voltage levels and recieving the digitized data [35], [36].

3.2.2 Analog hardware

The analog hardware in this measurement system is required to shift the DAC output voltages into the desired range of -1 V to 1 V, to measure the current flowing through the OECT, and to remove the previously applied voltage shift so that the ADC can correctly interpret the signals.

The analog subsystem consists of three key building blocks: a differential amplifier to shift the DAC output, a transimpedance amplifier to convert current into voltage and a summing amplifier to remove the voltage offset prior to ADC conversion.

Differential Amplifier

The differential amplifier, illustrated in Figure 3.4, is a voltage subtraction circuit that produces an output voltage proportional to the difference between two input signals applied to the inverting (−) and non-inverting (+) terminals of an operational amplifier. This configuration provides a linear transfer function, making it well-suited for shifting voltage levels [37].

For the conceptual design, this amplifier is used to shift the DAC output voltage into the required range of $-1\,V$ to $1\,V$, using a reference voltage.

The general transfer (output) function is given by the following equation:

$$V_{out} = V_{REF} \cdot \frac{R_2}{R_1 + R_2} \cdot \left(1 + \frac{R_4}{R_3}\right) - V_{DAC} \cdot \frac{R_4}{R_3} \tag{3.2}$$

When the resistor ratios are equal:

$$\frac{R_2}{R_1} = \frac{R_4}{R_3} \tag{3.3}$$

the output function simplifies to:

$$V_{out} = \frac{R_4}{R_3} \cdot (V_{REF} - V_{DAC}) \tag{3.4}$$

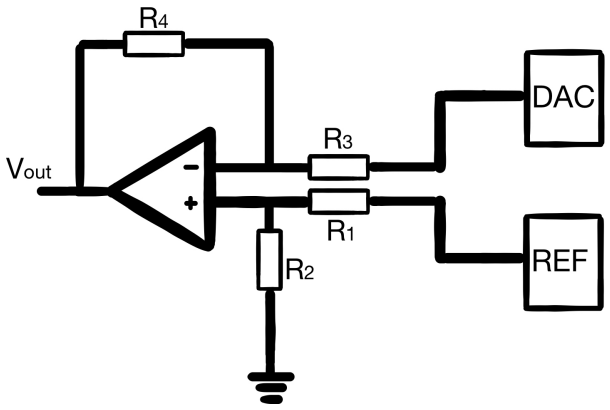


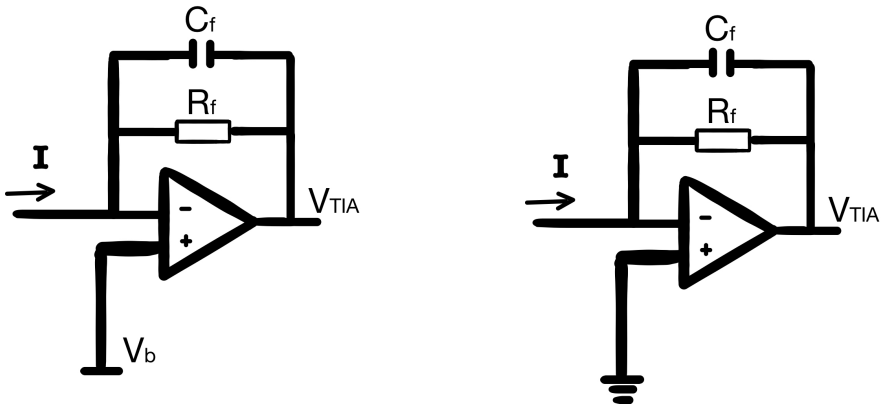
Figure 3.4: *Schematic design of an amplifier with a resistor configuration resulting in a differential amplifier. The DAC provides the voltage V_{DAC}, and the REF component provides the reference voltage V_{REF}. The output of the amplifier is labeled as V_{out}.*

To achieve a voltage output range of $-1\,V$ to $1\,V$, it is best that the reference voltage V_{REF} is approximately:

$$V_{REF} \approx \frac{V_{DAC,max}}{2} \tag{3.5}$$

Transimpedance Amplifier

The transimpedance amplifier (TIA) is a critical analog component in the measurement system. Its primary function is to convert the current generated by the OECT into a corresponding voltage. Although TIAs are commonly used with photodiodes [36, Chapter 4, pp. 537-539], the previously mentioned measurement systems demonstrate that the same principle can be used for OECT-based sensing. Two common TIA configurations are shown in Figure 3.5.



(a) With biasing voltage applied to the input.

(b) Without input biasing.

Figure 3.5: *Two common transimpedance amplifier configurations.*

In these configurations, the resistor R_f sets the gain of the amplifier. A capacitor C_f is typically placed in parallel with R_f to enhance stability and suppress oscillations caused by the sensor. This feedback capacitor reduces the bandwidth but improves the amplifier's robustness against high-frequency noise and instability [36, Chapter 4, pp. 537-539].

The way a transimpedance amplifier works is that it receives a current at the inverting input. However, due to the high input impedance of the op-amp, this input current cannot flow into the op-amp itself. Instead, the current flows through the feedback resistor R_f, generating a voltage drop across it. This voltage drop influences the op-amp's output voltage [36, Chapter 4, pp. 537-539].

The op-amp's reaction is to adjust its output in such a way that the inverting input voltage remains equal to the non-inverting input voltage (which sets the reference potential). This behavior keeps the voltage at the inverting input at a stable potential. As a result, the op-amp converts the input current into an output voltage proportional to the current and the value of R_f, effectively performing a current-to-voltage conversion without influencing the biased voltage on the non-inverting input [36, Chapter 4, pp. 537-539]. This stable, biased voltage is essential to ensure the OECT is supplied with a low voltage that doesn't change during measurements, as every small influence could lead to falls characterizations. The value of R_f in this design will be of most importance because it is chosen based on the expected input current range, as it directly determines how much voltage is produced per unit of current. Given that the output voltage range is limited by the amplifier's supply voltage, the gain must be carefully selected to avoid saturation while maximizing resolution [36, Chapter 4, pp. 537-539]. The output voltage of the TIA without an input biasing voltage is described by the following equation:

$$V_{\text{TIA}} = -I \cdot R_f \tag{3.6}$$

where I is the input current. The negative sign indicates that the amplifier is configured in an inverting mode.

The output voltage of the TIA with an input biasing voltage is described by the following equation:

$$V_{\text{TIA}} = V_b - I \cdot R_f \tag{3.7}$$

As discussed in Sections 2.2 and 2.3, the OECT channel exhibits variable conductivity due to doping and dedoping processes, which can be described using the generalized Ohm's law. Assuming a stable applied voltage, and considering that both the current and the channel's resistivity may vary, the channel can be effectively modeled as a variable resistor, represented by R_X. Section 2.3 also notes that the behavior of the current flowing from gate to source is the opposite from that of I_{ds}. It flows in the opposite direction and is typically 10 to 50 times smaller in magnitude. For design purposes, the gate-source path is likewise represented by a varying resistor R_X.

This resistive behavior is incorporated into the TIA design, which is configured with a biasing voltage V_b to control the drain or gate voltage of the OECT, as illustrated in Figure 3.6. In this configuration, positive current flows from the drain or gate toward the source, which is located away from the inverting input of the amplifier. As a result, the direction of current flow is opposite to that shown in Figure 3.5, leading to the following expression for the TIA output voltage:

$$V_{\text{TIA}} = V_b + I \cdot R_f \tag{3.8}$$

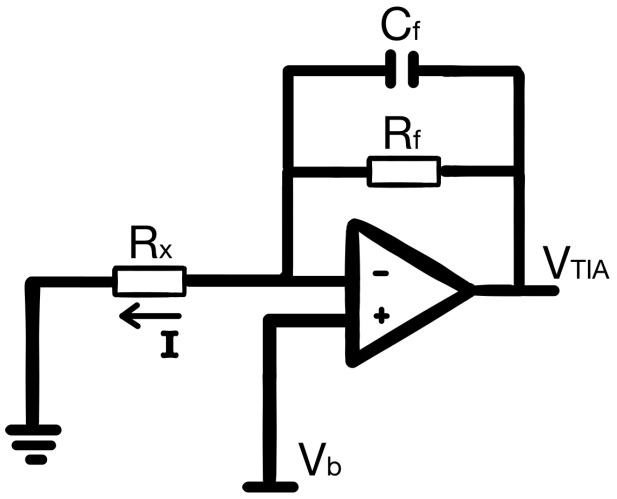


Figure 3.6: *Conceptual TIA configuration: R_X represents the OECT channel resistance, R_f the feedback resistor, C_f the feedback capacitor, I the drain current through the channel, V_{TIA} the output of the amplifier, and V_b the bias voltage applied to the non-inverting input.*

In the previously mentioned custom measurement setups, no feedback capacitor was included in the amplifier design. However, according to the B-M model, there is a capacitance present at the interface between the OECT channel and the gate electrode. Although the exact input capacitance of the textile-based OECT is unknown, their relatively large physical dimensions could suggest a significant parasitic capacitance between the conductive layers [38]. This unknown but likely high input capacitance could affect the stability of the amplifier [36, Chapter 4, pp. 537-539]. Including a feedback capacitor C_f in the design could mitigate this issue by reducing high-frequency noise and improving the stability of the amplifier. The C_f value is chosen so that the amplifier's $-3\,dB$ bandwidth (frequency f_{3dB} at which the output begins to attenuate) remains below the point where instability might occur. This helps prevent oscillations and ensures that the amplifier provides reliable and accurate current measurements across the desired frequency range [36, Chapter 4, pp. 537-539].

Because the appropriate value for C_f depends on several variables, its selection is typically an iterative process. Practical tuning often involves simulation or experimental adjustment to optimize both stability and performance [36, Chapter 4, pp. 537-539]. To implement this approach in the design, the following formula is used to calculate an initial estimate of C_f:

$$C_f \geq \frac{1}{2\pi R_f f_{3dB}} \tag{3.9}$$

Summing Amplifier

The summing amplifier is placed after the TIA to shift, scale, or simultaneously shift and scale the output voltage of the TIA, thereby adapting it to the input range required by the ADC configuration. In this design, a 3-input summing amplifier is implemented, with the three inputs being V_{TIA}, V_{cc}, and ground (connected via resistor R_5). This configuration is based on the work

of Adrian S. Nastase [39], who describes a method to convert a bipolar voltage range of −5 V to +5 V into a unipolar range of 0 V to 2.5 V.

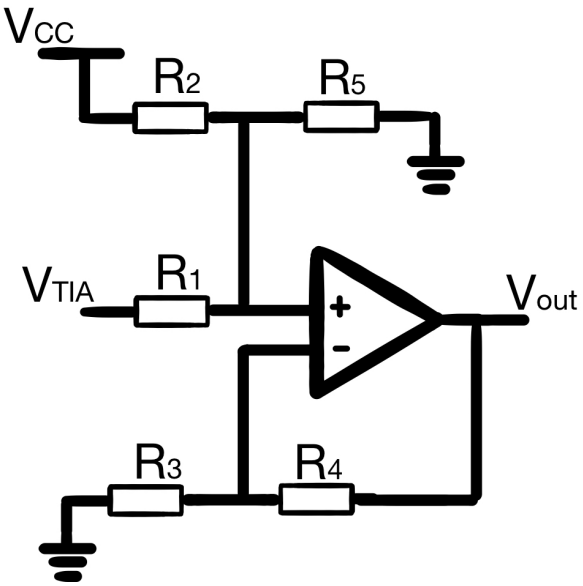


Figure 3.7: *Three-input summing amplifier used to convert the bipolar TIA output to a unipolar voltage suitable for the ADC. V_{cc} is a fixed reference voltage, V_{TIA} is both the output of the transimpedance amplifier and the input to the summing amplifier, and V_{out} is the resulting output voltage of the summing amplifier.*

The output voltage of this summing amplifier is given by:

$$V_{\text{out}} = \left(1 + \frac{R_4}{R_3}\right)\left[V_{\text{TIA}} \cdot \frac{(R_2^{-1} + R_5^{-1})^{-1}}{R_1 + (R_2^{-1} + R_5^{-1})^{-1}} + V_{\text{cc}} \cdot \frac{(R_1^{-1} + R_5^{-1})^{-1}}{R_2 + (R_1^{-1} + R_5^{-1})^{-1}}\right] \tag{3.10}$$

R_1, R_3, and R_5 are chosen with standard resistor values of 10 kΩ, 10 kΩ, and 4.99 kΩ, respectively. This leaves two unknown resistor values: R_3 and R_4. These can be determined by solving the two equations below. The equations incorporate the known lower and upper bounds of the TIA output voltage V_{TIA}, and the corresponding desired lower and upper bounds of the output voltage of the summing amplifier. By solving the corresponding equation, Adrian S. Nastase found that resistor R5 reduces both the weight of V_{cc} and V_{TIA}, attenuating both signals [39].

$$\begin{cases} V_{\text{out,lower}} = \left(1 + \dfrac{R_4}{R_3}\right)\left[\begin{array}{l} V_{\text{TIA,lower}} \cdot \dfrac{(R_2^{-1} + R_5^{-1})^{-1}}{R_1 + \left(R_2^{-1} + R_5^{-1}\right)^{-1}} \\ + V_{\text{cc}} \cdot \dfrac{(R_1^{-1} + R_5^{-1})^{-1}}{R_2 + \left(R_1^{-1} + R_5^{-1}\right)^{-1}} \end{array}\right] \\ V_{\text{out,upper}} = \left(1 + \dfrac{R_4}{R_3}\right)\left[\begin{array}{l} V_{\text{TIA,upper}} \cdot \dfrac{(R_2^{-1} + R_5^{-1})^{-1}}{R_1 + \left(R_2^{-1} + R_5^{-1}\right)^{-1}} \\ + V_{\text{cc}} \cdot \dfrac{(R_1^{-1} + R_5^{-1})^{-1}}{R_2 + \left(R_1^{-1} + R_5^{-1}\right)^{-1}} \end{array}\right] \end{cases} \tag{3.11}$$

Low-pass filter

A low-pass filter is a signal conditioning component that allows low-frequency signals to pass through while attenuating higher-frequency noise or unwanted components. It is commonly used to suppress high-frequency interference and to smooth signals before analog-to-digital conversion [40].

Figure 3.8 illustrates the basic schematic of a first-order RC low-pass filter. In this configuration, an input voltage V_{in} is applied across a series resistor R, followed by a capacitor C connected to ground. The filtered output voltage V_{out} is taken across the capacitor.

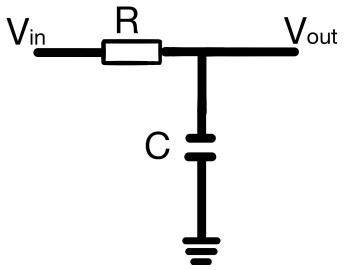


Figure 3.8: *Schematic of a low-pass filter where V_{in} is the input voltage of the circuit and V_{out} is the output voltage of the circuit.*

Low-pass filters can be implemented either passively, as shown in Figure 3.8, or actively using operational amplifiers [40]. The most basic configuration is the first-order RC low-pass filter, where the cutoff frequency f_c is given by:

$$f_c = \frac{1}{2\pi RC} \tag{3.12}$$

R is the resistance and C is the capacitance of the filter. The cutoff frequency represents the point where the output signal power drops to half of the input power, corresponding to a $-3\,\text{dB}$ reduction in amplitude [40].

3.2.3 Additional constraints and components

Beyond the digital and analog signal path design, certain power and reference considerations are needed to ensure the system's stability and precision. In particular, the use of amplifiers that operate with both positive and negative voltages introduces additional requirements on the power supply architecture. This section outlines the functional building blocks required to meet these constraints: a stable regulated voltage, a negative voltage rail, and a precise voltage reference.

Low Dropout Linear Voltage Regulator

A low dropout (LDO) linear regulator is used to derive a clean, stable analog supply voltage from a higher input source. It ensures minimal output voltage variation, even when the input fluctuates slightly or the load conditions change. This clean supply voltage is essential for maintaining low noise levels and consistent performance in sensitive analog circuitry, particularly in data converters and amplifiers. Compared to switching regulators, LDOs are preferred in low-noise applications due to their simpler topology and quieter output [36, Chapter 9].

Switched-Capacitor Voltage Converter

To support analog circuits requiring bipolar operation, a negative voltage rail is derived from the regulated positive supply using a switched-capacitor voltage inverter. This type of converter uses charge-pump techniques to generate an inverted output voltage without the need for inductors. Although limited in output current compared to other power conversion methods, switched-capacitor inverters are compact, efficient, and ideal for generating modest negative supplies in space-constrained systems [36], [41].

Highly Stable Voltage Reference

For precise analog measurements, signal conditioning, and DAC output generation, a highly stable voltage reference is essential. These devices provide a fixed output voltage with extremely low temperature drift, low noise, and excellent line and load regulation. Unlike general-purpose voltage regulators, voltage references are specifically optimized for accuracy and stability, making them critical in systems where the performance of ADCs or DACs depends directly on reference quality. Even small fluctuations in reference voltage can introduce measurable errors in high-resolution systems [42].

3.3 Calculations, simulations and components

With the functionality of each block defined and the design constraints understood, this section presents the required components, supporting calculations, and simulations needed to translate the concept into a practical implementation.

3.3.1 Microcontroller

The microcontroller selected for this system can be seen in figure 3.9(a). This is the Seeed XIAO nRF52840, chosen for its compact form and robust integrated features. One of its key advantages is support for Bluetooth 5.0, made possible by an onboard antenna. Compared to earlier versions, Bluetooth 5.0 offers significantly greater range, speed, and data throughput, making it ideal for applications requiring fast and reliable wireless communication. At its core lies the Nordic nRF52840, a 32-bit ARM Cortex-M4 processor running at 64 MHz. The integrated functionality of a Floating Point Unit (FPU) enables efficient and precise real-number computations, which is particularly beneficial for processing sensor data. In addition, the board provides 2 MB of onboard flash memory, offering some, but limited space for firmware and data storage [43].

Additional features of this microcontroller would be that the compact and power-efficient board is well-suited for small compact applications due to its small footprint (21 $\times$ 17.8 mm) and integrated features where the board is designed for ultra-low power consumption, drawing less than 5 uA in standby mode, which extends battery life. It also includes a battery charging chip, enabling both charging and power management for lithium batteries, simplifying power supply design [43].

Altogether, these features make the Seeed XIAO nRF52840 not only well-suited for processing OECT data, but also leaving the option open for a compact, portable device.

Figure 3.9(a) shows the pin layout of the Seeed XIAO nRF52840 (sense) microcontroller. In

this design, the 5 V pin is used to power the entire system, the GND pin provides the common ground, and the SDA and SCL pins are used for I^2C communication between components.

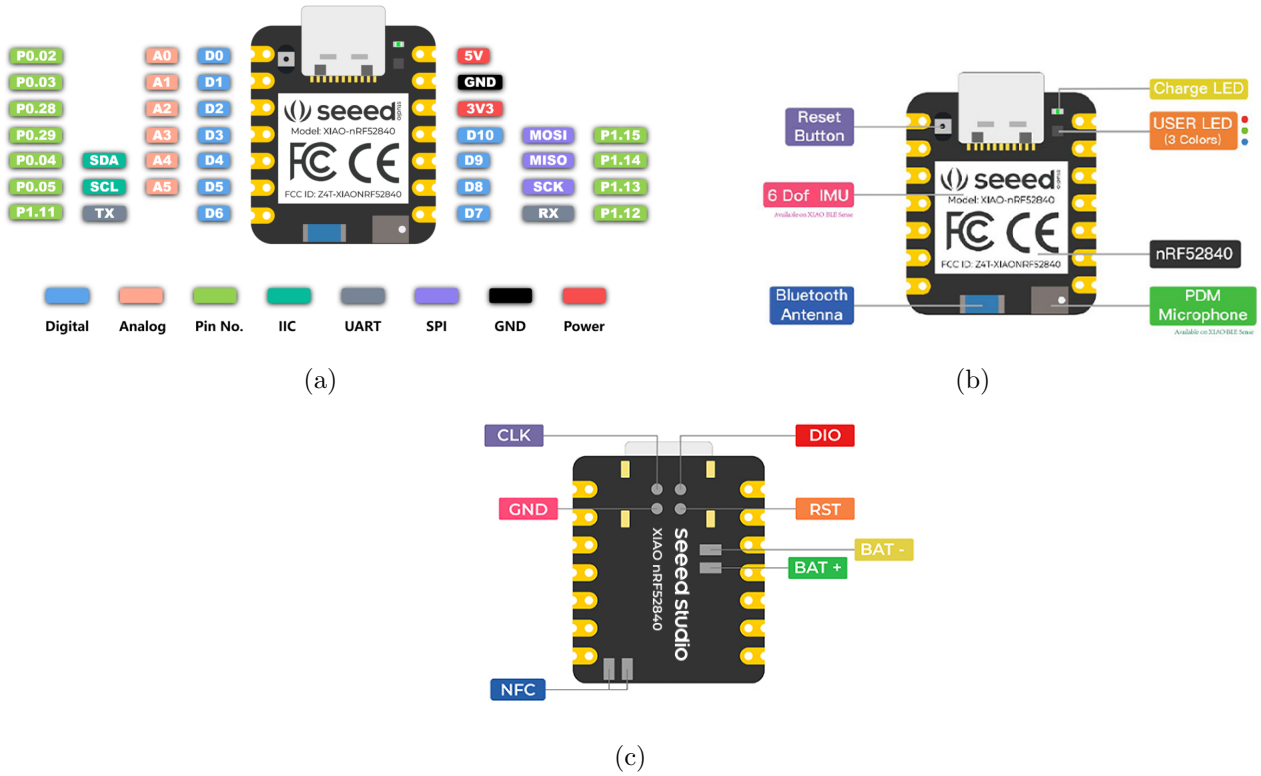


Figure 3.9: *(a) Pin layout of the Seeed XIAO nRF52840 (Sense) microcontroller. (b) Top view showing the Bluetooth antenna, reset button, LEDs, and chip. (c) Bottom view showing additional connections, including BAT+ and BAT- for the positive and negative battery terminals.*

3.3.2 Low dropout linear voltage regulator

This design utilizes the MIC5205-3.3YM5-TR, an efficient low-dropout linear voltage regulator well-suited for noise-sensitive applications. The MIC5205 features an ultra-low noise output, a very low dropout voltage and a low ground current of just 600 µA at 100 mA output. It also offers high output accuracy, with an initial precision better than 1%. In this implementation, the fixed 3.3 V version is used to regulate the 5 V input from the microcontroller down to a clean and stable 3.3 V. This regulated voltage serves as the positive supply rail for all other components in the system.

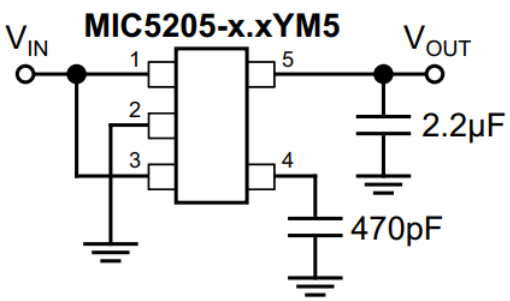


Figure 3.10: *Diagram of the MIC5205. V_{in} is the voltage recieved from the MCU and V_{out} is the regulated output voltage of the LDO.*

For more information about the MIC5205, refer to the datasheet [44].

3.3.3 Switched-capacitor voltage converter

The MAX660 is a compact CMOS charge-pump device that operates as an unregulated inverter or voltage doubler. Requiring only two external capacitors, it efficiently converts a positive input voltage into a corresponding negative output.

Operating over a supply range from 1.5 V to 5.5 V, the MAX660 can deliver up to 100 mA of output current, making it ideal for compact, low-noise systems. It consumes only 120 µA of quiescent current and achieves conversion efficiencies exceeding 90% under typical loads. For applications requiring higher output current or lower output impedance, multiple devices can be connected in parallel.

The operation of the MAX660 relies on two key external capacitors. Capacitor C_1, connected between the CAP+ and CAP- pins, serves as the charge-pump capacitor. It alternately charges and discharges through internal switches, effectively transferring charge to invert the input voltage and generate the negative output. Capacitor C_1, connected between the output V_{out} and ground, functions as the output smoothing capacitor. It helps to filter out voltage ripple caused by the switching operation and provides a steady negative voltage to the load.

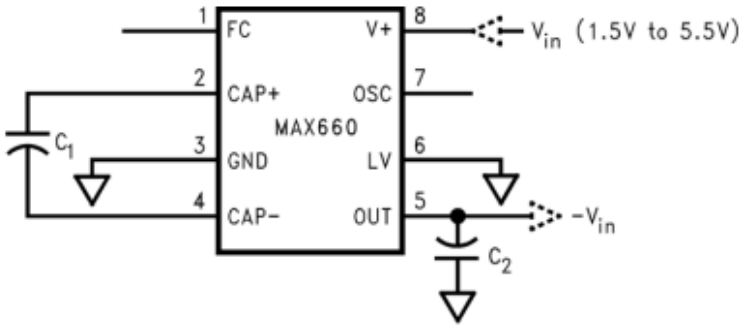


Figure 3.11: *Diagram of the MAX660. V_{in} is the output voltage recieved from the LDO. $-V_{in}$ is the output of the MAX660 serving as the negative voltage supply.*

For more information about the MAX660, see the datasheet [45].

3.3.4 Highly stable voltage reference

This design uses two precision voltage reference ICs from Texas Instruments: the REF35180QDBVR and the REF35330QDBVR. Both belong to the REF35 series and are chosen for their excellent initial accuracy (±0.05%), low noise, and long-term stability.

Operating from a supply range of 2 V to 5.5 V, these references are used to shift analog signals within the system. The REF35180 provides a fixed 1.8 V output and is used to bias the differential amplifier. The REF35330, with a 3.3 V output, is used to shift the output of the summing amplifier.

The diagram of the REF35 voltage reference is shown in Figure 3.12. Where for each option of the REF35 the diagram is the same.

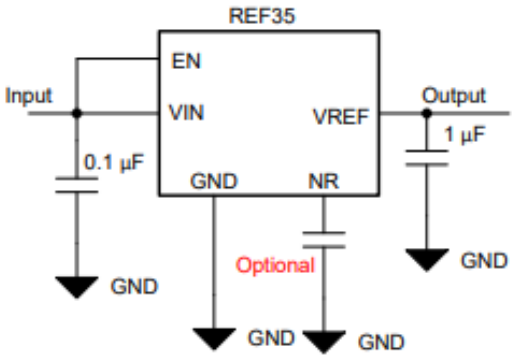


Figure 3.12: *Functional diagram of the REF35 voltage reference. The EN (enable) pin is tied to the input supply to keep the device active, while the VREF pin provides the precise reference output voltage.*

The only difference between the two is their output voltage, which allows them to serve specific roles within the analog signal chain. Since both are from the same product family, they offer consistent thermal and electrical performance across the system.

For more information, refer to the REF35 datasheet [46].

3.3.5 Digital-to-analog converter

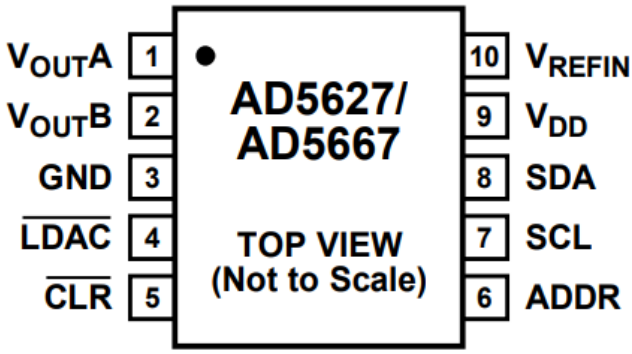


Figure 3.13: *Diagram of the AD5667. Where V_{REFIN} is the reference voltage V_{DD} the supply voltage, SDA and SCL are the I^2C connections, ADDR is the address pin and $V_{OUT}A$ and $V_{OUT}B$ are the 2 output channels*

The AD557RBRMZ-Reel 2 is selected as the digital-to-analog converter (DAC) for this system. It belongs to the nanoDAC family, which consists of low-power, voltage-output DACs available in 12-, 14-, and 16-bit resolutions. These devices operate from a single 2.7 V to 5.5 V supply, are guaranteed monotonic by design, and communicate via an I^2C-compatible serial interface.

In this design, the DAC is powered by the regulated 3.3 V rail provided by the low-dropout regulator. The reference voltage (V_{ref}) is externally connected to the supply voltage (V_{dd}), which means the maximum output voltage of the DAC corresponds to the supply level, i.e., 3.3 V under ideal conditions.

The output voltage (V_{out}) of the DAC is determined by the following equation:

$$V_{\text{out}} = V_{\text{ref}} \cdot \frac{D}{2^N} \tag{3.13}$$

Here, D represents the digital value sent by the microcontroller, and N is the resolution of the DAC in bits. This equation illustrates that the DAC can generate output voltages ranging from 0 V up to V_{ref}, enabling precise analog signal generation within the 0 V to 3.3 V range.

Theoretical Resolution:

Assuming the 16-bit DAC ($N = 16$) and a reference voltage of 3.3 V:

- If $D = 0$, then $V_{\text{out}} = 3.3 \cdot \frac{0}{65536} = 0\,\text{V}$.
- If $D = 32768$ (half-scale), then $V_{\text{out}} = 3.3 \cdot \frac{32768}{65536} = 1.65\,\text{V}$.
- If $D = 65535$ (maximum), then $V_{\text{out}} = 3.3 \cdot \frac{65535}{65536} \approx 3.29995\,\text{V}$.

The smallest possible voltage step, or resolution, is given by:

$$\text{Resolution} = \frac{V_{\text{ref}}}{2^N} = \frac{3.3\,\text{V}}{65536} \approx 0.00005035\,\text{V} = 50.35\,\mu\text{V} \tag{3.14}$$

This means the DAC can increment its output in steps of approximately 50.35 µV allowing for extremely fine control over the analog output signal.

I²C Interface:

The DAC communicates with the microcontroller via the I²C bus, where each device must have a unique address to avoid conflicts. The AD5667 includes an address selection pin, labeled ADDR, which determines its I²C address, as shown in Table 3.1.

Table 3.1: *AD5667 I²C Address Selection*

`ADDR` Connection	I²C Address
VDD	`0x0C`
Open	`0x0E`
GND	`0x0F`

This allows for basic address flexibility, enabling the use of two identical DACs on the same I²C bus. If only one DAC is used, one is free to configure the ADDR pin as he likes depending on the desired address.

The AD5667 includes two independent DAC channels, labeled A and B. These channels can be individually addressed in software, as shown in Table 3.2.

Table 3.2: *DAC Channel Addressing*

Channel Selection	Code
VOUT_A	0x00
VOUT_B	0x01
VOUT_A and VOUT_B	0x02

Communication with the DAC is done by sending a 24-bit command word over I²C.

The first 8 bits (MSBs) contain the command and configuration information. These bits specify which DAC channel is being addressed and how the data should be processed (e.g., write and update, power-down mode, etc.).

The remaining 16 bits contain the actual DAC input data. This is the digital value that determines the output voltage.

For more information about the AD5667, see the datasheet [47].

3.3.6 Analog-to-digital converter

The ADS1115 from Texas Instruments is a high-precision, low-power, 16-bit analog-to-digital converter (ADC) featuring an I^{2}C-compatible interface. It is well-suited for applications requiring accurate conversion of small analog signals, particularly in power- and space-constrained environments.

Figure 3.14 illustrates the functional block diagram of the ADS1115 along with its pinout. The four analog input pins (AIN0 to AIN3) support both single-ended and differential measurements. Communication is handled via the SCL and SDA pins, while the ADDR pin enables selection of up to four different I^{2}C addresses. The ALERT/RDY pin can be configured for comparator-based threshold monitoring or to signal when a conversion is complete.

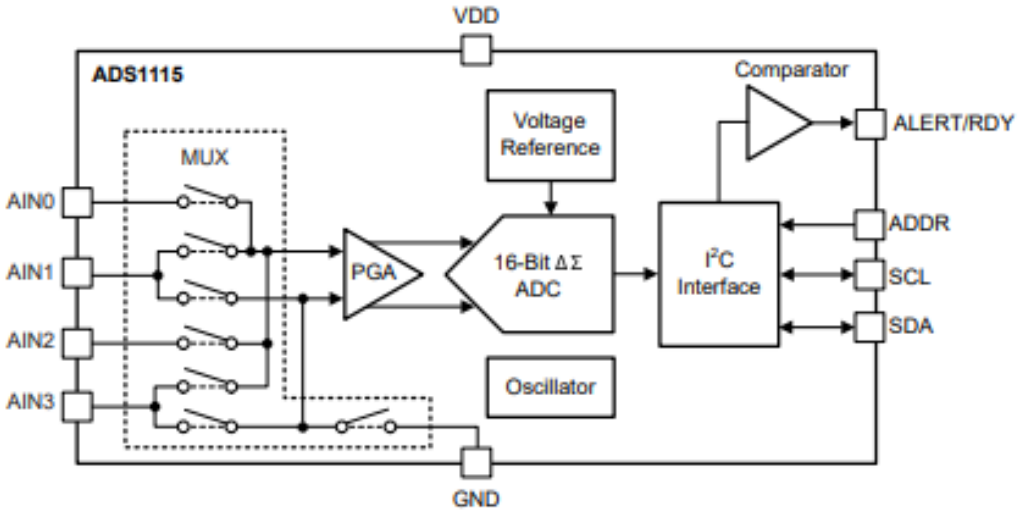


Figure 3.14: *Functional block diagram and pinout of the ADS1115. The diagram shows the analog input pins (left), a multiplexer (MUX) for channel selection, a programmable gain amplifier (PGA), and a 16-bit ADC core. Digital I^{2}C communication pins and the ALERT/RDY pin are also shown (right).*

Supporting both single-ended and differential input configurations, thereby the ADS1115 offers flexibility depending on measurement requirements. In differential mode, the ADC measures the voltage difference between two inputs (e.g., AIN0 – AIN1) and utilizes the full 16-bit output range to represent voltages from −FS to +FS (full-scale), making it ideal for applications requiring high precision and common-mode noise rejection. In single-ended mode, each input channel is measured relative to ground. Although the ADC still outputs 16-bit values, only the positive range (0 to +FS) is used, since the input cannot go below ground. As a result, the most significant bit (MSB), which represents polarity, is always zero in single-ended mode. This represents a resolution of 15 bits. As a summary, while both modes provide 16-bit output, only differential

mode fully utilizes the entire dynamic range. A key feature of the ADS1115 is its programmable gain amplifier (PGA), which adjusts the input range to match the signal amplitude. This ensures the ADC utilizes its full resolution across a variety of input levels. Available full-scale ranges, listed in Table 3.3, span from ±256 mV to ±6.144 V.

In this design, the ADS1115 operates from a 3.3 V supply provided by an LDO regulator, limiting the measurable input voltage to the full-scale range of ±4.096 V with a resolution of 125.0 µV, as shown in Table 3.3. To optimize resolution, the summing amplifier can be designed to constrain its output between 0 V and 2 V. This allows a PGA setting of 2× (±2.048 V), which increases the resolution to 62.5 µV per step.

Table 3.3: *ADS1115 PGA Gain Settings and Corresponding Resolution*

PGA Setting	**Full-Scale Range (V)**	**Resolution (V/LSB)**
2/3×	±6.144 V	187.5 µV
1×	±4.096 V	125.0 µV
2×	±2.048 V	62.5 µV
4×	±1.024 V	31.25 µV
8×	±0.512 V	15.625 µV
16×	±0.256 V	7.8125 µV

Signal-to-Noise Ratio

ADCs inherently introduce noise into measurements. Although the ADS1115 offers a 16-bit resolution, its effective resolution is lower due to various noise sources, especially in low-frequency or DC measurements where (1/f) thermal and component instability can be dominating [48].

The theoretical Signal-to-Noise Ratio (SNR) for an ADC can be estimated by accounting for its nominal bit resolution and the relationship between the sampling rate f_s and the signal bandwidth Δf [48]. This leads to the following formula:

$$\mathrm{SNR}_{\mathrm{dB}} = 6.02 \cdot N + 1.76 + 10 \cdot \log_{10}\left(\frac{f_s}{2\Delta f}\right)$$

This equation provides an estimate of the theoretical SNR under ideal conditions. In real applications, the effective number of bits (ENOB) is typically lower, depending on the sampling configuration and reference voltage quality [48].

I²C Interface:

The ADS1115 communicates via the I²C bus and supports both standard (100 kHz) and fast mode (400 kHz). Its 7-bit I²C address is configured using the ADDR pin, allowing up to four devices on the same bus, as shown in Table 3.4.

Table 3.4: *ADS1115 I²C Address Configuration*

ADDR Pin Connection	**I²C Address**
GND	0x48
VDD	0x49
SDA	0x4A
SCL	0x4B

For more information about the ADS1115, refer to the datasheet [49].

3.3.7 Differential amplifier calculations and simulations

With the reference voltage being set to 1.8 V, and the DAC provides an output ranging from 0 V to 3.3 V. The differential amplifier output voltage can be calculated according to equation (3.4), as defined in Section 3.2.2.

$$V_{\text{out}} = \frac{R_4}{R_3} \cdot (V_{\text{REF}} - V_{\text{DAC}})$$

To achieve an output voltage range approximately centered around 0 V, with symmetric limits near -1 V and $+1$ V, the resistor ratio $\frac{R_4}{R_3}$ is selected as follows:

$$\frac{R_4}{R_3} = \frac{7.15\,\text{k}\Omega}{10\,\text{k}\Omega}$$

Using this ratio, the maximum and minimum output voltages of the amplifier can be calculated as:

$$V_{\text{out,max}} = 0.715 \cdot (1.8 - 0) = 1.287\,\text{V}$$

$$V_{\text{out,min}} = 0.715 \cdot (1.8 - 3.3) = -1.0725\,\text{V}$$

This results in an effective output voltage range of $[-1.0725\,\text{V}, 1.285\,\text{V}]$, which is suitable for biasing the OECT with both positive and negative voltages.

Figure 3.15 presents the results obtained from LTspice based on the theoretical calculations. It shows the simulated input signals applied to the differential amplifier and the corresponding output signal. The simulation uses the resistor values described in this section, illustrating the amplifier's behavior under the expected operating conditions.

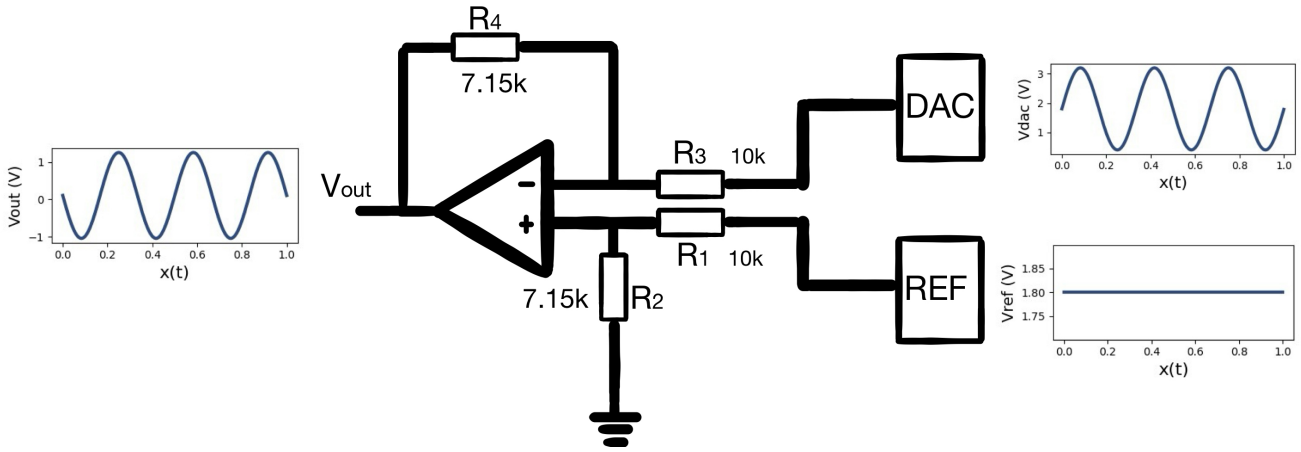


Figure 3.15: *LTspice simulation of the differential amplifier, showing both input and output signals based on the chosen resistor values. The schematic representation of the amplifier is included in the center of the figure.*

Knowing that the full output range of the differential amplifier is approximately $[-1.0725\,\mathrm{V},\ 1.287\,\mathrm{V}]$, the DAC output can be limited to ensure the amplifier output remains within $[-1\,\mathrm{V},\ 1\,\mathrm{V}]$. Using the equation:

$$V_{\text{out}} = 0.715 \cdot (1.8 - V_{\text{DAC}}) \tag{3.15}$$

we can solve for V_{DAC} corresponding to output limits:

$$V_{\text{DAC}} = 1.8 - \frac{V_{\text{out}}}{0.715} \tag{3.16}$$

For $V_{\text{out}} = 1\,\mathrm{V}$:

$$V_{\text{DAC,min}} = 1.8 - \frac{1}{0.715} \approx 0.401\,\mathrm{V}$$

For $V_{\text{out}} = -1\,\mathrm{V}$:

$$V_{\text{DAC,max}} = 1.8 + \frac{1}{0.715} \approx 3.199\,\mathrm{V}$$

Therefore, to limit the amplifier output to the desired range of $[-1\,\mathrm{V},\ 1\,\mathrm{V}]$, the DAC output values should be within the range $[0.401\,\mathrm{V},\ 3.199\,\mathrm{V}]$.

3.3.8 Transimpedance amplifier calculations and simulations

To design the transimpedance amplifier, the first step is to define the expected current ranges and voltage constraints. The differential amplifier provides output voltages ranging from $-1\,\mathrm{V}$ to $+1\,\mathrm{V}$, while the currents to be measured fall within the range of $-20\,\mathrm{mA}$ to $+20\,\mathrm{mA}$ for I_{ds}, and $-2\,\mathrm{mA}$ to $+2\,\mathrm{mA}$ for I_{gs}.

Based on the voltage swing of the differential amplifier, the effective channel resistance R_X of the OECT and the gate-source path can be estimated using Ohm's law as:

$$R_X = \frac{V}{I} = \frac{1\,\mathrm{V}}{20\,\mathrm{mA}} = 50\,\Omega$$

This represents the minimum channel resistance expected at the maximum current for I_{ds}. Similarly, for the smaller current range for I_{gs}:

$$R_X = \frac{1\,\mathrm{V}}{2\,\mathrm{mA}} = 500\,\Omega$$

Although the op-amp supports rail-to-rail operation between $\pm 3.3\,\mathrm{V}$, a swing limit of $\pm 3.0\,\mathrm{V}$ is chosen to provide headroom for voltage shifts in the supply voltages. The transimpedance gain can be calculated out of the equation 3.8 from section 3.2.2:

$$R_f = \frac{V_{\mathrm{TIA}} - V_b}{I} \tag{3.17}$$

Design for I_{ds}

Given the full-scale current range of $\pm 20\,\mathrm{mA}$ and a DAC voltage swing of $\pm 1.0\,\mathrm{V}$, the required feedback resistor is:

$$R_f = \frac{3.0\,\mathrm{V} - 1.0\,\mathrm{V}}{20\,\mathrm{mA}} = 100\,\Omega$$

As shown in Figure 3.16, the LTSpice simulation confirms the expected output behavior with the corresponding feedback resistor of 100 Ω (gain), validating the previous calculations.

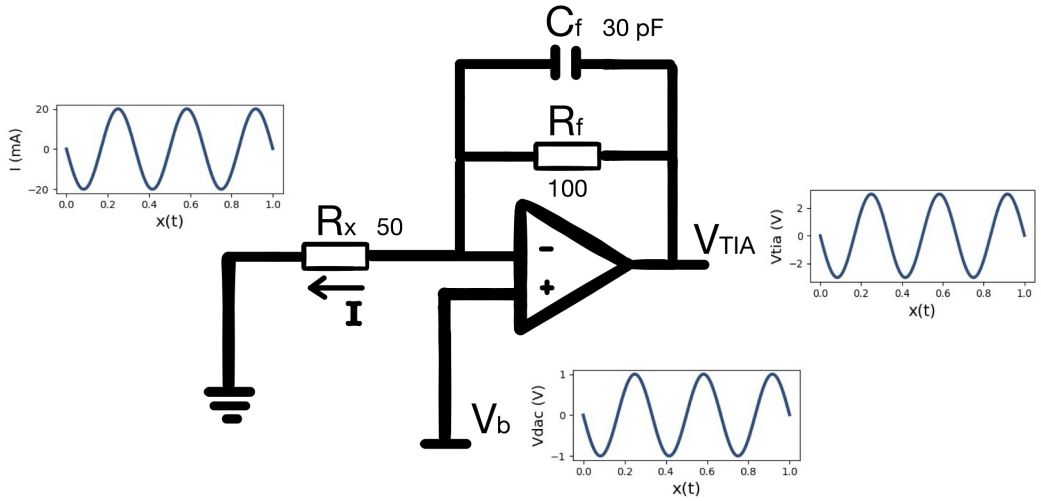


Figure 3.16: *LTSpice simulation of the transimpedance amplifier response for I_{ds}. The plot (left) shows the current flowing through R_X, (bottom) the corresponding DAC voltage after the differential amplifier, and (right) the resulting output voltage V_{TIA}. In the middle is the schematic representation of the TIA with its corresponding values*

To suppress high-frequency noise while maintaining sufficient bandwidth, an initial target cutoff frequency of $f_{-3\,\mathrm{dB}} = 50\,\mathrm{kHz}$ is selected. Based on this, the feedback capacitor would be:

$$C_f = \frac{1}{2\pi \cdot 100\,\Omega \cdot 50\,\mathrm{kHz}} \approx 31.8\,\mathrm{pF}$$

As a practical starting point for experimentation and tuning, this value is rounded to a standard capacitor of 30 pF.

Design for I_{gs}

For the smaller current range of $\pm 2\,\mathrm{mA}$, the required feedback resistor becomes:

$$R_f = \frac{3.0\,\mathrm{V} - 1.0\,\mathrm{V}}{2\,\mathrm{mA}} = 1\,\mathrm{k\Omega}$$

To maintain filtering behavior and simplify the design, the same 30 pF capacitor is used here as in the I_{ds} case. This results in a cutoff frequency that is a factor of 10 lower:

$$f_{-3\,\mathrm{dB}} = \frac{1}{2\pi \cdot 1\,\mathrm{k\Omega} \cdot 30\,\mathrm{pF}} \approx 5.3\,\mathrm{kHz}$$

As with the I_{ds} path, this capacitor value is treated as a the start value for the iterative process of choosing the best fitting value.

As shown in Figure 3.17, the LTSpice simulation confirms the expected output behavior with the corresponding feedback resistor of 1k Ω (gain), validating the previous calculations.

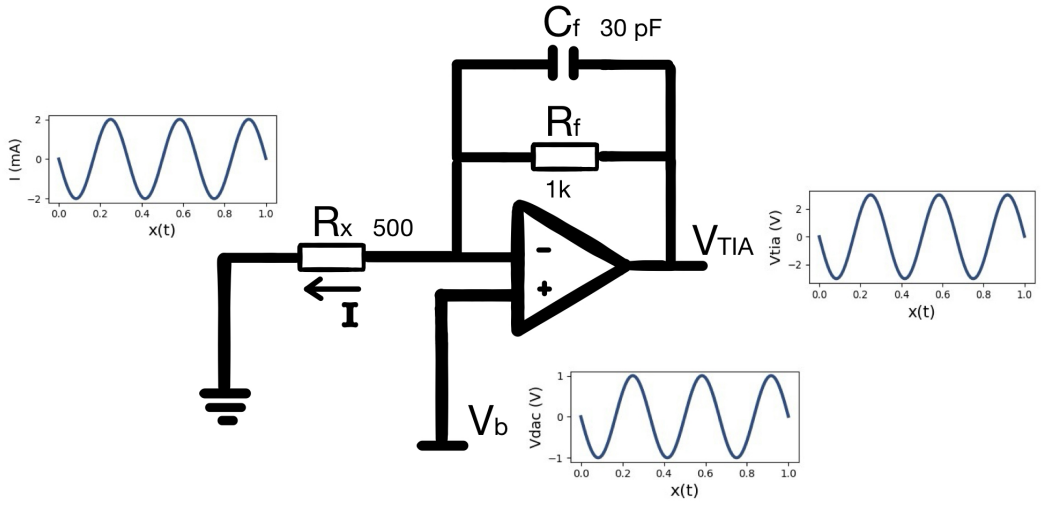


Figure 3.17: *LTSpice simulation of the transimpedance amplifier response for I_{gs}. The plot (left) shows the current flowing through R_X, (bottom) the corresponding DAC voltage after the differential amplifier, and (right) the resulting output voltage V_{TIA}. In the middle is the schematic representation of the TIA with its corresponding values*

3.3.9 Summing amplifier calculations and simulations

As for the summing amplifier, it is now known that the recieving voltage from the TIA will be between -3 V and 3 V. While also knowing that the output voltage should be between 0 and 2V to fit the ADCs expectations. With the previously resistor values mentioned in section 3.2.2 being R1, R3 and R5 being 10kOhms, 10kOhms and 4.99kOhms, where V_{cc} (V_{ref}) is the maximum reference voltage that can be applied in this circuit which is 3.3V.

using drian S. Nastase equation from section 3.2.2 R2 and R4 can be found to configure the wished output voltage.

$$\begin{cases} V_{\text{out,lower}} = \left(1 + \dfrac{R_4}{R_3}\right) \left[\begin{array}{l} V_{\text{TIA,lower}} \cdot \dfrac{(R_2^{-1} + R_5^{-1})^{-1}}{R_1 + \left(R_2^{-1} + R_5^{-1}\right)^{-1}} \\ + V_{\text{cc}} \cdot \dfrac{(R_1^{-1} + R_5^{-1})^{-1}}{R_2 + \left(R_1^{-1} + R_5^{-1}\right)^{-1}} \end{array} \right] \\ V_{\text{out,upper}} = \left(1 + \dfrac{R_4}{R_3}\right) \left[\begin{array}{l} V_{\text{TIA,upper}} \cdot \dfrac{(R_2^{-1} + R_5^{-1})^{-1}}{R_1 + \left(R_2^{-1} + R_5^{-1}\right)^{-1}} \\ + V_{\text{cc}} \cdot \dfrac{(R_1^{-1} + R_5^{-1})^{-1}}{R_2 + \left(R_1^{-1} + R_5^{-1}\right)^{-1}} \end{array} \right] \end{cases}$$

Filling in the known values:

$$\begin{cases} V_{\text{out,lower}} = \left(1 + \dfrac{R_4}{10\,000}\right) \left[\begin{array}{l} (-3) \cdot \dfrac{(R_2^{-1} + (4990)^{-1})^{-1}}{10\,000 + \left(R_2^{-1} + (4990)^{-1}\right)^{-1}} \\ + 3.3 \cdot \dfrac{((10\,000)^{-1} + (4990)^{-1})^{-1}}{R_2 + ((10\,000)^{-1} + (4990)^{-1})} \end{array} \right] \\ V_{\text{out,upper}} = \left(1 + \dfrac{R_4}{10\,000}\right) \left[\begin{array}{l} (3) \cdot \dfrac{(R_2^{-1} + (4990)^{-1})^{-1}}{10\,000 + \left(R_2^{-1} + (4990)^{-1}\right)^{-1}} \\ + 3.3 \cdot \dfrac{((10\,000)^{-1} + (4990)^{-1})^{-1}}{R_2 + ((10\,000)^{-1} + (4990)^{-1})^{-1})} \end{array} \right] \end{cases}$$

The result of solving the system gives $R_2 = 11.00\,\text{k}\Omega$ and $R_4 = 3.01\,\text{k}\Omega$. To simplify the design and allow for slight variations in the TIA supply voltage, R_2 can be rounded to a standard value of $10.00\,\text{k}\Omega$. Recalculating under this constraint gives $R_4 = 2.71\,\text{k}\Omega$, resulting in an output voltage range of approximately

$$V_{\text{out}} \approx [0.091\,\text{V},\ 2\,\text{V}].$$

To provide additional headroom at the upper end of the ADC's input range, R_4 can be further reduced to $2.20\,\text{k}\Omega$, which narrows the output range to

$$V_{\text{out}} \approx [0.091\,\text{V},\ 1.920\,\text{V}].$$

This configuration ensures the output signal remains safely within the ADC's limits.

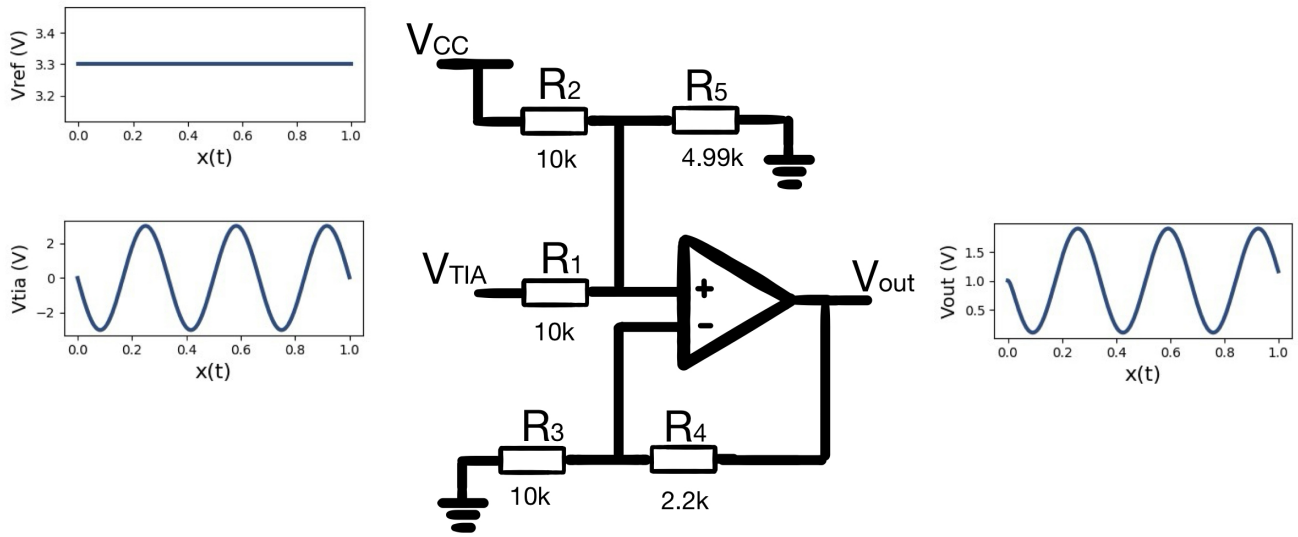


Figure 3.18: *LTSpice simulation of the summing amplifier. The plots on the left show the input voltages from the TIA and the reference source, while the plot on the right shows the resulting output voltage V_{OUT}. The central schematic illustrates the summing amplifier with its corresponding resistor values.*

As shown in Figure 3.18, the simulation confirms the expected output voltage of the summing amplifier using the previously calculated resistor values, validating the theoretical design.

3.3.10 Components for the amplifiers

For measuring both I_{ds} and I_{gs}, a total of six amplifiers will be used: two differential amplifiers (one for each current), and a transimpedance and summing amplifier for each path. In the I_{gs} circuit, the OPAx192 can be selected for the transimpedance and summing amplifiers, while the differential amplifier uses the OPAx323. For the I_{ds} circuit, the OPAx323 can be used for all three roles. This configuration balances performance requirements while also leaving the option open with cost considerations.

OPAx192

The OPAx192 operational amplifier series is particularly well-suited for this application due to its combination of excellent DC precision, wide bandwidth, and rail-to-rail input and output capabilities. It offers a typical input offset voltage of only ±5 µV and an extremely low offset drift of ±0.2 µV/°C.

Its rail-to-rail I/O architecture enables operation across the full supply range, which in this case spans from −3.3 V to +3.3 V, allowing both positive and negative output voltages. Additionally, the OPAx192 provides a high output current capability of ±65 mA, a gain-bandwidth product of 10 MHz, and a slew rate of 20 V/µs.

In summary, the OPAx192 is a high-performance precision op-amp ideal for accurately controlling gate-source and drain-source voltages in a low-current, high-resolution OECT measurement setup.

OPAx323

The OPAx323 is a cost-effective, general-purpose operational amplifier that still offers key performance features such as rail-to-rail input and output, low input bias current (0.5 pA), and high bandwidth. It features a typical input offset voltage of ±150 µV and a gain-bandwidth product of 20 MHz, with a fast slew rate of 33 V/µs.

Comparison

In summary, the OPAx192 is chosen for its superior precision, which is critical for accurate low-current measurements. The OPAx323, on the other hand, is selected to reduce overall cost, as its performance remains sufficient for less demanding stages. This mixed approach is only to allow the idea of cost reduction.

3.3.11 Low-pass filter calculation

To suppress high-frequency noise and ensure signal stability before analog-to-digital conversion, a first-order RC low-pass filter is implemented at the output of each summing amplifier. In this design, a resistor value of $R = 9.09\,\mathrm{k\Omega}$ is paired with a capacitor of $C = 1\,\mu\mathrm{F}$ to form the filter, as shown in Figure 3.19. The cutoff frequency of this configuration is determined using the standard RC low-pass filter formula from section 3.2.2:

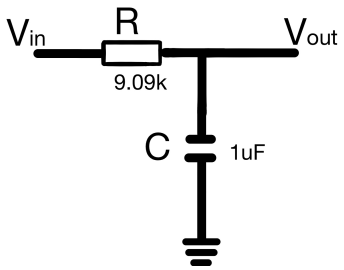


Figure 3.19: *Schematic of the low-pass filter with selected component values $R = 9.09\,k\Omega$ and $C = 1\,\mu F$.*

$$f_c = \frac{1}{2\pi RC}$$

The cutoff frequency is calculated as:

$$f_c = \frac{1}{2\pi \cdot 9090 \cdot 1 \times 10^{-6}} \approx 17.5\,\mathrm{Hz}$$

This means that signal components above approximately 17.5 Hz will be attenuated, while lower frequencies will pass through with minimal attenuation.

The ADC used in this design has an internal switched-capacitor sampling mechanism. According to its datasheet, the ADS1115 performs best when the source impedance is kept below 10 MΩ to allow the input sampling capacitor to charge fully during each acquisition period [48], [49].

Since the resistor used in the low-pass filter is $R = 9.09\,\mathrm{k\Omega}$, it lies within the recommended range and therefore would not compromise the accuracy of the ADC readings.

3.3.12 Analog measurement circuit overview

This section presents the complete analog hardware setup of the system, where each previously described analog component is integrated into a single circuit. A full schematic of the analog design for both channels, implemented in LTspice, is provided in Appendix A.

The analog circuitry on the gate-source side is identical to that of the drain-source side, with the only difference being the gain of the transimpedance amplifier with a factor of 10. As a result, the general architecture of both circuits is the same, as illustrated in Figure 3.20.

To summarize the operation of the circuit: a differential amplifier generates a voltage between $-1\,\mathrm{V}$ and $1\,\mathrm{V}$, which is applied to the non-inverting input of the transimpedance amplifier. This voltage serves as a bias, setting the potential at the inverting input and allowing current to flow through the feedback resistor R_f and the channel of the OECT which was previously mentioned as R_X. The transimpedance amplifier then converts this current into a voltage proportional to the current through R_X.

This output voltage is fed to the non-inverting input of a summing amplifier. Simultaneously, a fixed reference voltage is also applied to this input to shift the resulting signal into a positive voltage range, suitable for the ADC. The feedback configuration of the summing amplifier ensures that the outputs upper limit stays within the desired operating range.

Before reaching the ADC, the output signal passes through a low-pass filter. This stage serves to suppress high-frequency noise and ensure a cleaner signal is digitized.

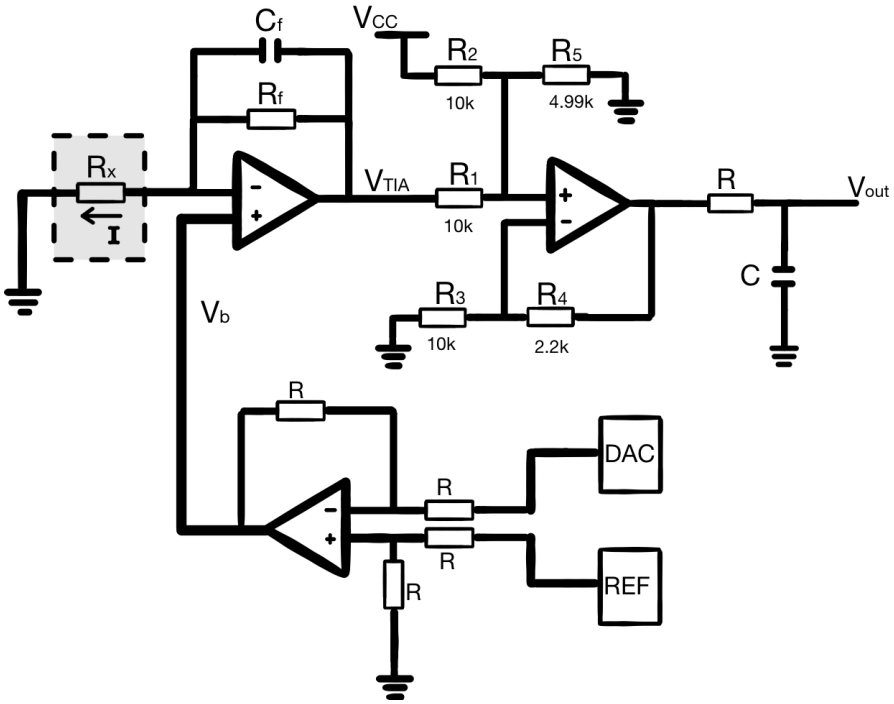


Figure 3.20: *Schematic of the analog measurement circuit. It shows the connection from the differential amplifier to the transimpedance and summing amplifiers, ending with a low-pass filter before ADC input. The shaded area indicates the current measurement path.*

To ensure the measuring system can calculate the I_{gs} and I_{ds}, a traceback to the current flowing through resistor R_X must be performed. This happens by combining previously mentioned formulas and calculations into the TIA current term I.

This can be done by implementing the formula of the TIA into the equation of the summing amplifier:

$$V_{\text{out}} = \left(1 + \frac{R_4}{R_3}\right)\left[V_{\text{TIA}} \cdot \frac{(R_2^{-1} + R_5^{-1})^{-1}}{R_1 + (R_2^{-1} + R_5^{-1})^{-1}} + V_{\text{cc}} \cdot \frac{(R_1^{-1} + R_5^{-1})^{-1}}{R_2 + (R_1^{-1} + R_5^{-1})^{-1}}\right]$$

Knowing that the previously calculated values for the resistors are $R_1 = R_2 = R_3 = 10\,\text{k}\Omega$, $R_4 = 2.2\,\text{k}\Omega$, and $R_5 = 4.99\,\text{k}\Omega$, and that the supply voltage V_{cc} used as a reference is 3.3 V, the full expression for the summing amplifier can now be evaluated numerically.

Thereby first part is the gain:

$$1 + \frac{R_4}{R_3} = 1 + \frac{2200}{10000} = 1.22$$

Then calculating the parallel combination which is repetitive for both voltages because $R_1 = R_2$:

$$(R_2^{-1} + R_5^{-1}) = \frac{1}{10000} + \frac{1}{4990} = 0.0001 + 0.0002004 = 0.0003004$$

$$\Rightarrow (R_2^{-1} + R_5^{-1})^{-1} = \frac{1}{0.0003004} \approx 3328.34\,\Omega$$

Taking all the resistors together:

$$\frac{(R_2^{-1} + R_5^{-1})^{-1}}{R_1 + (R_2^{-1} + R_5^{-1})^{-1}} = \frac{3328.34}{10000 + 3328.34} = \frac{3328.34}{13328.34} \approx 0.24971$$

Substitute this into the summing amplifier formula:

$$V_{\text{out}} = 1.22 \cdot [V_{\text{TIA}} \cdot 0.24971 + 3.3 \cdot 0.24971]$$

$$\Rightarrow 0.30464 \cdot (V_{\text{TIA}} + 3.3)$$

With the simplified summing amplifier equation, the transimpedance amplifier expression from Equation 3.8 can now be directly implemented:

$$V_{\text{TIA}} = V_b + I \cdot R_f \quad \Rightarrow \quad V_{\text{out}} = 0.30464 \cdot (V_b + R_f \cdot I + 3.3)$$

Rewriting this equation in terms of current I yields:

$$\boxed{I = \frac{1}{R_f}\left(\frac{V_{\text{out}}}{0.30464} - V_b - 3.3\right)}$$

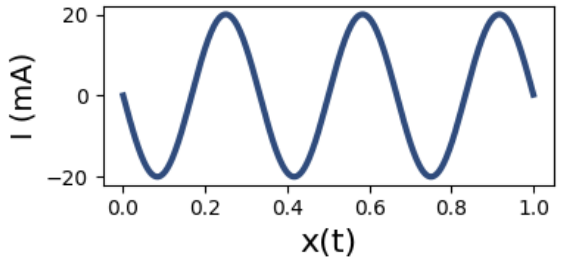
Using this expression, different cases can be considered for both the I_{ds} and I_{gs} current calculations. Testing this equation on the outer bounds with the estimated conditions:

$$V_{\text{out}} \approx [0.091\,\text{V},\ 1.920\,\text{V}], \quad V_b \approx [-1\,\text{V},\ 1\,\text{V}], \quad R_{f,ds} = 100\,\Omega, \quad R_{f,gs} = 1000\,\Omega$$

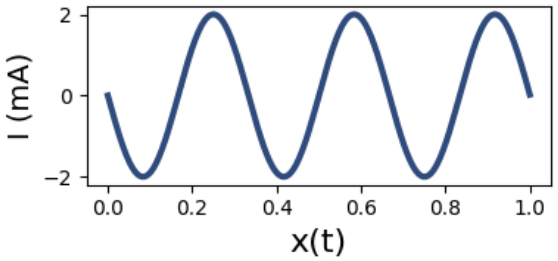
Table 3.5: *Calculated Current Bounds*

Current	Conditions	Lower Bound (mA)	Upper Bound (mA)
I_{gs}	$V_b \in [-1, 1]$, $R_f = 1000\,\Omega$	-2.001	2.003
I_{gs}	$V_b = 0$, $R_f = 1000\,\Omega$	-3.001	3.003
I_{ds}	$V_b \in [-1, 1]$, $R_f = 100\,\Omega$	-20.013	20.030
I_{ds}	$V_b = 0$, $R_f = 100\,\Omega$	-30.013	30.025

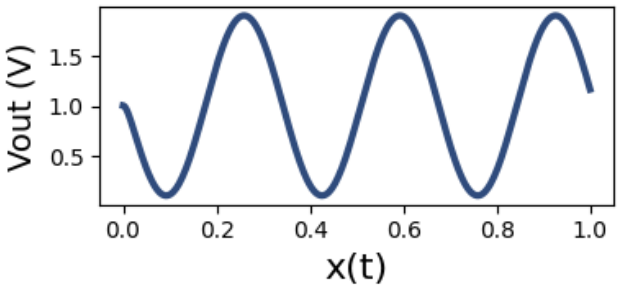
These calculations closely match the previous simulations, as shown in Figure 3.21. Where the calculation for I_{ds} match the -20 to 20mA in Figure 3.21(a), for I_{gs} the -2 to 2 mA in Figure 3.21(b), calculated from the summing amplifiers which ranged from 0.091 to 1.920 V in Figure 3.21(c).



(a) I_{ds} simulation with $R_f = 100\,\Omega$



(b) I_{gs} simulation with $R_f = 1000\,\Omega$



(c) Simulated output of the summing amplifier for full range input

Figure 3.21: *Simulation results for I_{ds} and I_{gs} currents and the resulting summing amplifier output.*

With this confirmation, the equations to calculate the currents for gate-source and drain-source paths can be defined as:

$$\boxed{I_{gs} = \frac{1}{1000}\left(\frac{V_{\text{out}}}{0.30464} - V_b - 3.3\right)} \quad \text{and} \quad \boxed{I_{ds} = \frac{1}{100}\left(\frac{V_{\text{out}}}{0.30464} - V_b - 3.3\right)}$$

These expressions allow for direct estimated computation of the corresponding currents based on the measured output voltage of the summing amplifier and the known bias voltage V_b coming from the differential amplifier.

3.4 PCB design and fabrication

With the circuit architecture and component selection finalized, a custom printed circuit board (PCB) was designed to physically implement the measurement system. The PCB integrates all key digital and analog components with separate connections to the OECT, creating a compact and robust design. Design and layout were performed using KiCad 8.0, which provided full control over schematic capture, layout routing, and electrical rule checking. The full schematic design and PCB layout can be found in Appendix B.

A two-layer PCB was used, with the bottom layer dedicated as a solid ground plane. This design choice improves signal integrity and provides a stable reference for the circuit's analog and digital sections.

3.4.1 Microcontroller integration

Figure 3.22 illustrates the integration of the Seeed XIAO nRF52840 module into the PCB design. The microcontroller is connected to the PCB using through-hole headers. All pins are routed to outer through-hole pads, making each microcontroller pin externally accessible. This also allows the connection of additional microcontrollers or peripheral components if needed. A hole was placed in the center of the footprint to provide access to the bottom side of the module, specifically for the battery connection described in Section 3.3.1.

The rotated view in Figure 3.22(c) shows the top-layer layout, with the XIAO module in the middle and the additional routed connections on the sides.

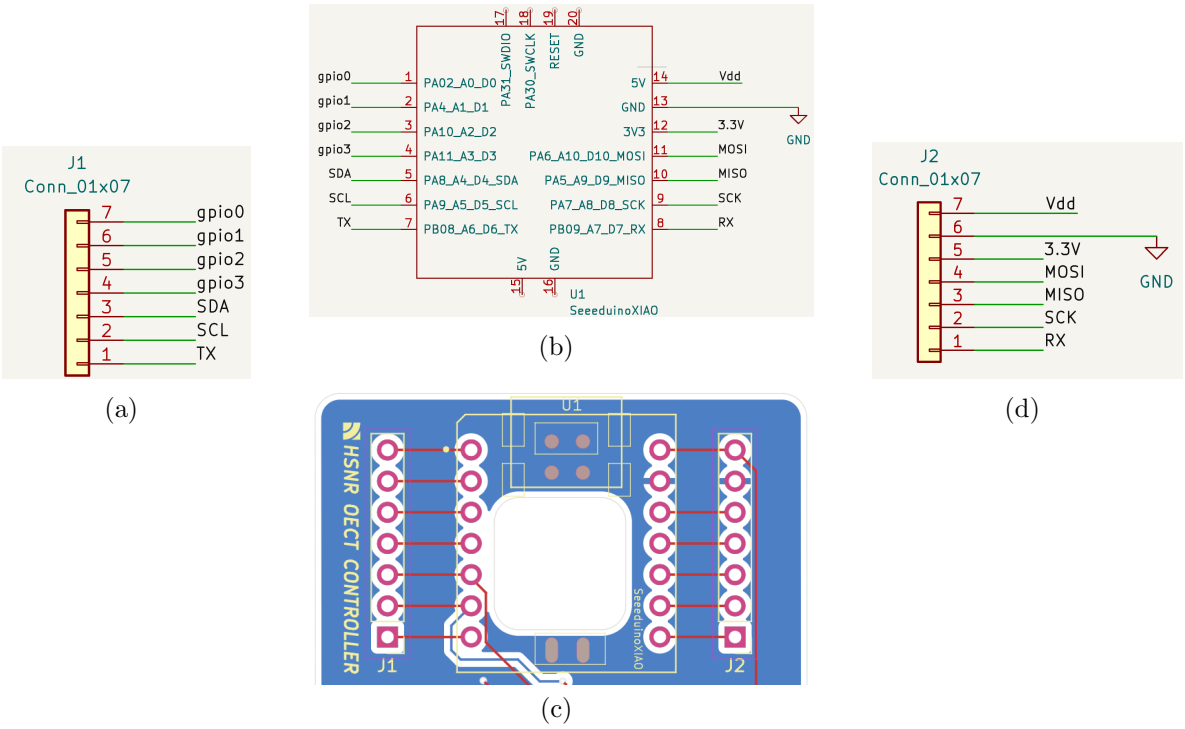
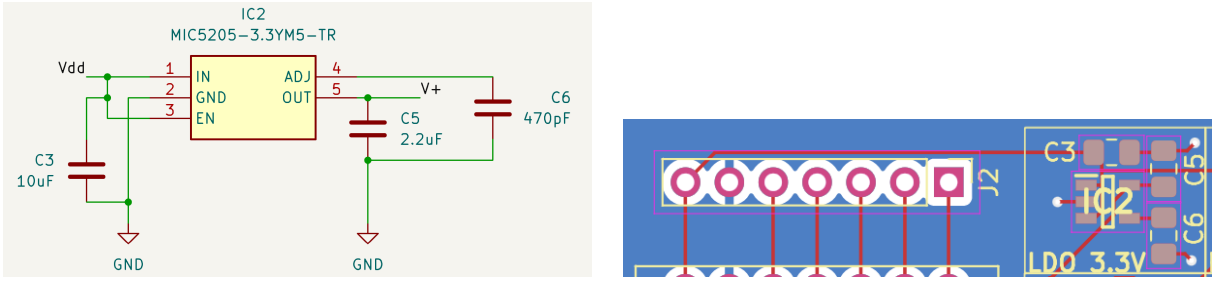


Figure 3.22: *Overview of the KiCad layout and routing for the Seeed XIAO connections. (a) shows the left pin connections corresponding to the left side of the PCB layout in (c), (b) shows the microcontroller module corresponding to the middle part of the PCB layout, and (d) displays the right pin connections corresponding to the right row of through hole pins in the PCB routing.*

3.4.2 Low-dropout regulator implementation

The Low-Dropout Regulator's (LDO) design comes from the previously mentioned UWED device in section 3.1.2 together with its datasheet design mentioned in section 3.3.2 where care was taken to place decoupling capacitors near the output pin to improve stability and reduce noise. Additionally, the ground return paths were kept short to minimize potential interference.

Figure 3.23 shows both the KiCad layout and the PCB view of the LDO section. It includes connections to the 5 V (V_{dd}) input supply from the MCU and the regulated 3.3 V (V_+) output that will be used over the total circuit.



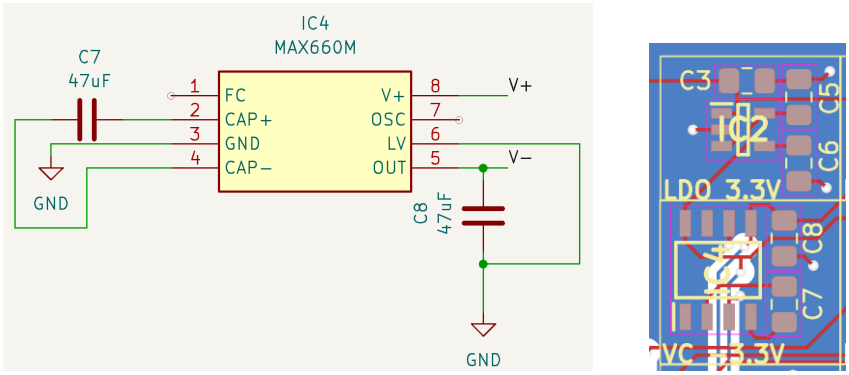
(a) (b)

Figure 3.23: *Layout of the Low-Dropout Regulator (LDO): (a) schematic view in KiCad, and (b) layout view and position of the LDO in the PCB design.*

3.4.3 Switched-capacitor voltage converter integration

The voltage converter in this design comes from the the component's datasheet. While the recommended value for the output capacitors is 150 µF for optimal stability, 47 µF capacitors were used in this design due to component shortage from the manufacturer. According to the datasheet, this reduced value is acceptable but may result in a less stable output.

Figure 3.24(a) shows the KiCad schematic where $V+$ is the input voltage coming from the LDO which is then converted to a negative voltage ($V-$) for the analog circuitry. A decoupling capacitor was also placed close to the output terminal to help suppress noise and ripple.



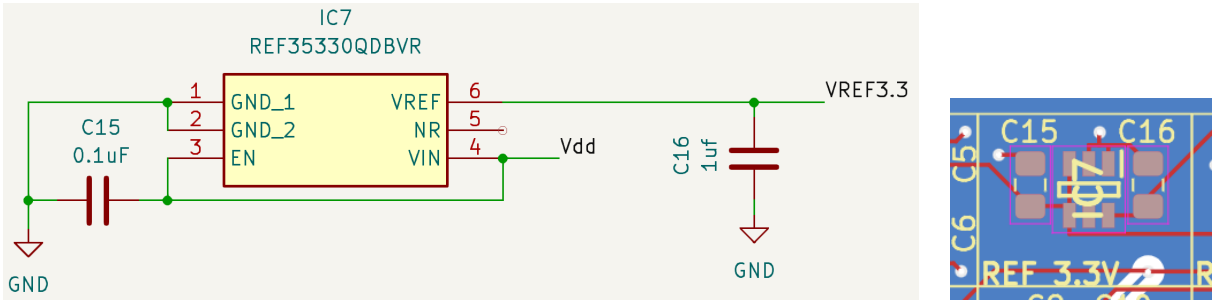
(a) (b)

Figure 3.24: *Voltage converter layout (VC): (a) schematic view in KiCad, and (b) layout view and position of the VC in the PCB design.*

3.4.4 Voltage reference integration

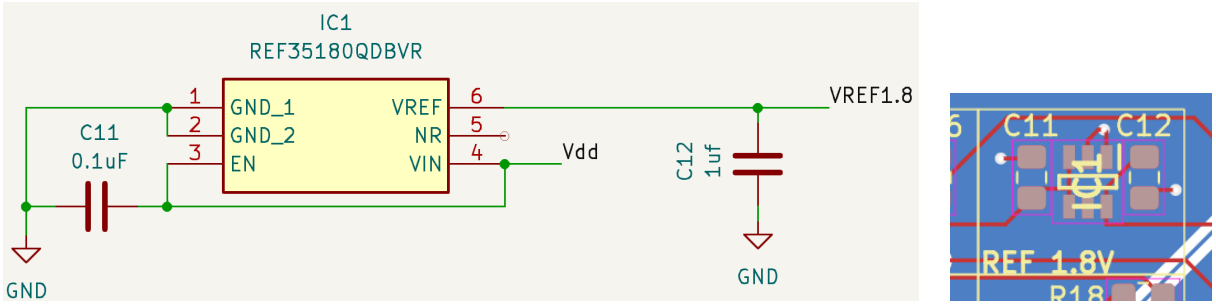
For both the 3.3 V and 1.8 V voltage reference ICs, which are from the same family, the design was based on the datasheet where the same decoupling capacitors were placed near the IC to reduce power supply ripple and ensure a clean reference voltage output.

Figure 3.25(a) and Figure 3.26(a) shows the 3.3 V and 1.8 V voltage reference layout in the KiCad schematic where the input voltage for both is coming from the MCU's 5 V pin (V_{dd}) and the ouput of these are VREF3.3 and VREF1.8. Where VREF1.8 will be used for the differential amplifiers and VREF3.3 will be used for the summing amplifiers.



(a) (b)

Figure 3.25: *Voltage reference integration (REF 3.3 V):(a) schematic view in KiCad, and (b) layout view and position of the REF 3.3 V in the PCB design.*

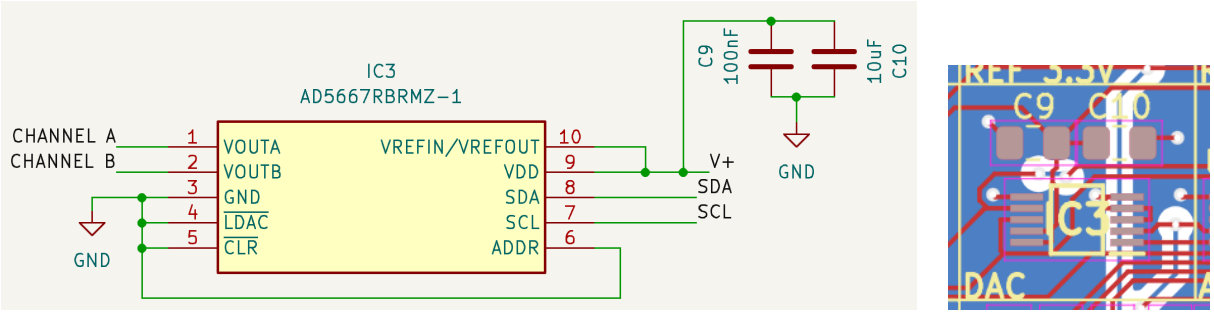


(a) (b)

Figure 3.26: *Voltage reference integration (REF 1.8 V):(a) schematic view in KiCad, and (b) layout view and position of the REF 1.8 V in the PCB design.*

3.4.5 Digital-analog converter integration

The design of the DAC was taken from the open-source UWED device, which can be seen in Figure 3.27(a). Which had a decoupling capacitor at the supply ($V+$) to remove noise. The reference input of the DAC was connected to the $V+$ as well. The SDA and SCL was connected to those of the MCU. CHANNEL A and CHANNEL B are the DAC's output to the differential amplifiers to supply the V_{gs} and V_{ds} voltage. The ADDR pin is connected to the ground, setting it's adress to 0x0F as mentioned in section 3.3.5.

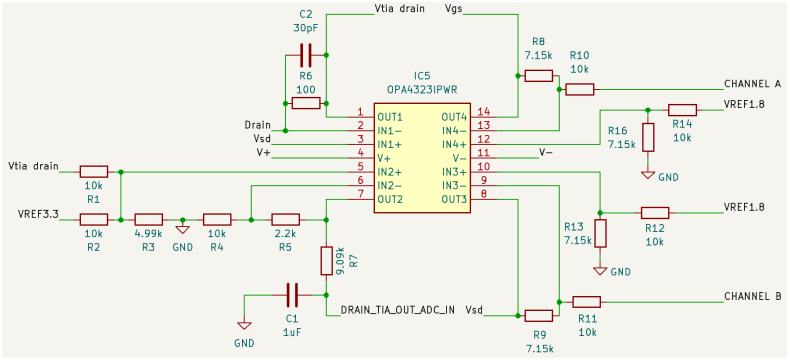


(a) (b)

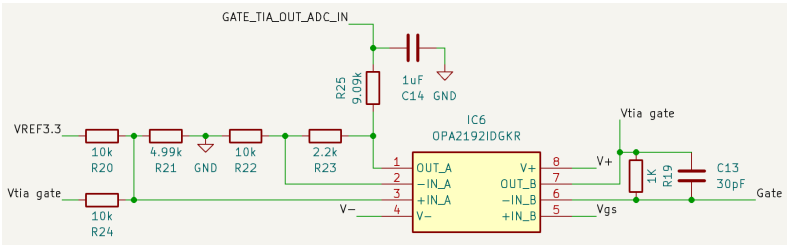
Figure 3.27: *AD5667 digital-analog converter integration (DAC): (a) schematic view of the DAC in KiCad, and (b) the layout view of the DAC in a section labeled as DAC.*

3.4.6 Amplifier integration

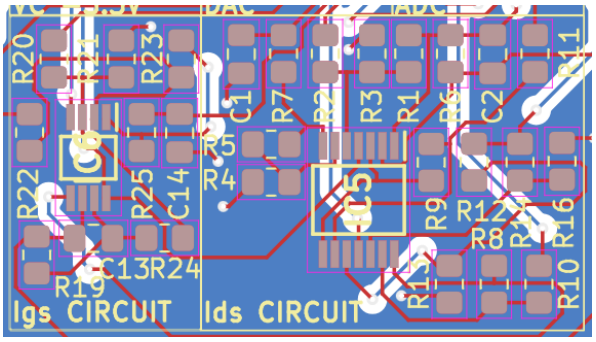
Figure 3.28(a) shows the schematic of the quad OPA4323 operational amplifier. On the right side of the figure, the VREF1.8 inputs and DAC outputs (CHANNEL A and CHANNEL B) are connected to two differential amplifiers, which generate the V_{gs} and V_{ds} control voltages. These connections correspond to the differential amplifier design shown in Figure 3.4 from Section 3.2.2.



(a)



(b)



(c)

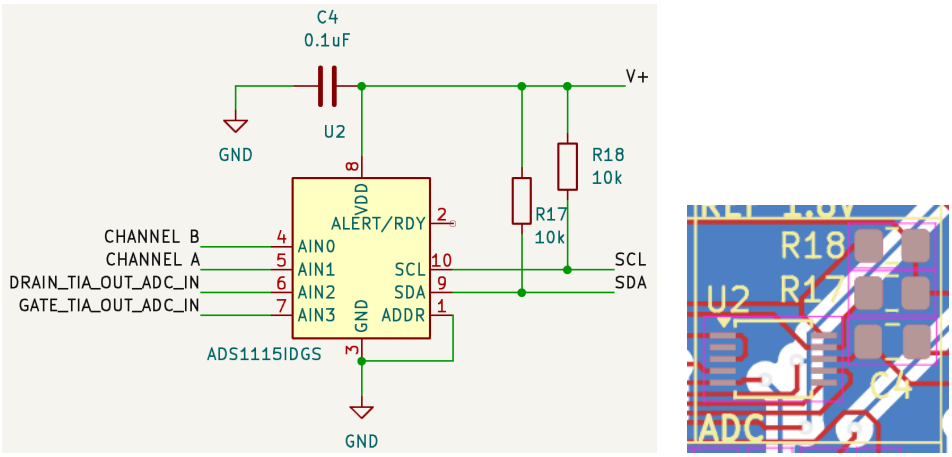
Figure 3.28: *Overview of amplifier in Kicad: (a) OPA4323 schematic, (b) OPAx192 schematic, and (c) PCB layout of both amplifier section. Where section labeled as I_{gs} circuit is the OPAx192 layout and the section labeled as I_{ds} circuit is the OPAx323.*

On the left side of the same figure, the V_{sd} output of the differential amplifier biases the drain terminal, which is routed to an external pin. This section forms the transimpedance amplifier, with the output labeled Vtia drain. This corresponds to the transimpedance configuration shown in Figure 3.6 in Section 3.2.2. The output signal then feeds into the summing amplifier stage, seen again on the left of the figure. Here, a VREF3.3 voltage reference is added to shift the signal, as described in Figure 3.7 from Section 3.7. The summing amplifier output is then filtered using a low-pass filter, with the final signal labeled DRAIN TIA OUT ADC IN. This filter corresponds to Figure 3.8 in Section 3.2.2.

Figure 3.28(b) shows the schematic of the dual OPA2192 operational amplifier, which is used for the I_{gs} side. On the right side, the V_{gs} signal that comes from the differential amplifier in Figure 3.28(a) biases the gate, which is also connected to an external pin. The output of the transimpedance amplifier is labeled Vtia gate and is routed on the left side to a summing amplifier stage, along with the VREF3.3 reference. As with the I_{ds} side, the final output is passed through a low-pass filter before digitization, which is called GATE TIA OUT ADC IN.

3.4.7 Analog-digital converter integration

The design for the ADC was taken from the datasheet mentioned in section 3.3.6. The 4 channels are connected to Channel B and Channel A of the DAC and the two outputs of the summing amplifiers DRAIN TIA OUT ADC IN and GATE TIA OUT ADC IN. The ADC is supplied with the $V+$ coming from the LDO, the ADDR pin is connected to the ground, setting the adress to 0X048 as mentioned in table 3.4 in section 3.3.6. The SDA and SCL lines are connected to the MCU and both have a pull-up resistor as recommended by the datasheet mentioned in section 3.3.6.



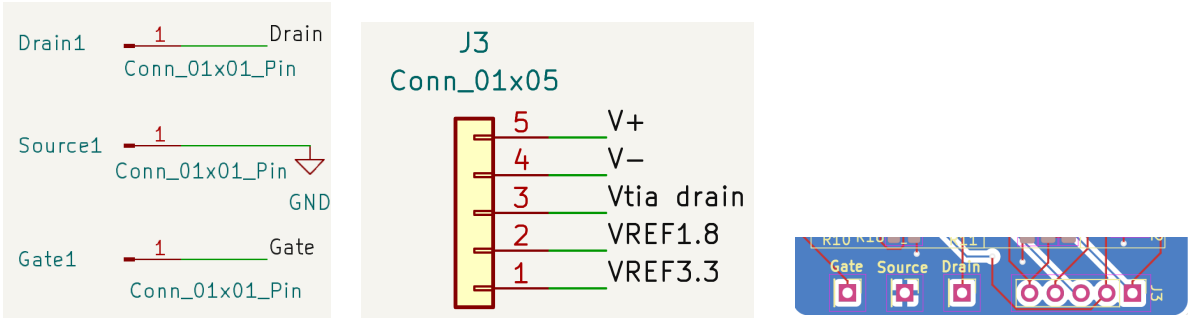
(a) (b)

Figure 3.29: *ads1115 analog-digital converter integration (ADC): (a) schematic view of the ADC in KiCad, and (b) the layout view of the ADC in a section labeled as ADC.*

3.4.8 Connections to gate, drain, and source

External through-hole connections were added to interface with the gate, drain, and source electrodes, as shown in Figures 3.30(a) and 3.30(c). These connections allow for easy access to the OECT terminals for measurement and testing.

In addition to the main electrode terminals, several extra pins were routed to internal measurement points. These optional test points, shown in Figure 3.30(b), are included to support future debugging or circuit optimization.



(a) (b) (c)

Figure 3.30: *(a) schematic view of through-hole pin headers for gate, drain, and source in KiCad. (b) Additional test point connections for debugging. (c) PCB layout view of the external connections.*

3.4.9 Price list

Table 3.6: *Component Pricelist Table*

Designator	Value	Price (€)
C1,C14	1uF	0.0744
C12,C16	1uF	0.0744
C2,C13	30pF	0.1180
C3,C10	10uF	0.1800
C4,C11,C15	0.1uF	0.1260
C9	100nF	0.1260
C5	2.2uF	0.3420
C6	470pF	0.0090
C7,C8	47uF	0.1200
IC1	REF35180QDBVR	3.4050
IC2	MIC5205-3.3YM5-TR	1.5505
IC3	AD5667RBRMZ-1	33.8760
IC4	MAX660M	2.6190
IC5	OPA4323IPWR	1.8840
IC6	OPA2192IDGKR	3.9540
IC7	REF35330QDBVR	3.4080
R1,R2,R4,R10,R11,R12,R14,R17,R18,R20,R22,R24	10k	0.0408
R3,R21	4.99k	0.0360
R5,R23	2.2k	0.0072
R6	100	0.0036
R7,R25	9.09k	0.0380
R8,R9,R13,R16	7.15k	0.0380
R19	1k	0.0034
U2	ADS1115IDGS	1.8810
U1	SeeeduinoXIAO	11.3100

The price list shown in Table 3.6 presents the components required for a single device, excluding costs for PCB manufacturing and assembly. The Designator column indicates the labels assigned to each component in the KiCad schematic, while the Value column specifies the component's value or type. The Price (€) column lists the price for each component.

The total cost of components for one device is approximately €60. However, since JLCPCB requires a minimum order quantity of two units for assembly, the total cost for two devices, including components and assembly, amounts to approximately €120. All components were sourced directly from JLCPCB and assembled using their assembly service option.

3.5 Software and firmware design

3.5.1 Microcontroller hardware setup

The core of the measurement system is the Seeed nRF52840 module. This module is a Bluetooth 5.0 System-on-Chip (SoC) from Nordic Semiconductor. Its integration into the measurement device enables interaction between the OECT Controller hardware and the desktop application.

3.5.2 Implementing CircuitPython on the seeed nRF52840

CircuitPython is an open-source Python implementation designed for microcontrollers, providing a high-level and quick scripting environment for hardware control [50].

The following steps were used to implement CircuitPython on the nRF52840 module:

1. **Download CircuitPython Firmware:** The appropriate CircuitPython firmware image for the nRF52840 was downloaded from the Adafruit CircuitPython releases repository giving an .uf2 file.
2. **Put the Module into Bootloader Mode:** Once connecting the MCU to a desktop, the nRF52840 module can be placed into bootloader mode by pressing the reset button twice.
3. **Copy the CircuitPython UF2 Firmware:** Once the module appeared as a USB storage device (BOOT drive), the downloaded .uf2 firmware file was copied directly to the drive. The module automatically rebooted into CircuitPython mode.
4. **CircuitPython Filesystem Setup:** After reboot, the module appeared as a USB drive named CIRCUITPY, where the user code and libraries were placed.
5. **Install Required Libraries:** The following CircuitPython libraries were installed into the lib folder of the CIRCUITPY drive:
    - adafruit bus device: For handling I^2C communication.
    - adafruit ads1x15: For interfacing with ADS1115 ADCs over I^2C.
    - adafruit ble: For Bluetooth Low Energy functionality, including advertising and services.
6. **Develop and Deploy Python Script:** The measurement firmware was written in a Python script (e.g., code.py, main.py) and placed onto the CIRCUITPY drive.

This process provided a setup for testing, and updating the embedded software on the nRF52840.

3.5.3 Firmware architecture

Once CircuitPython was installed on the nRF52840, the embedded firmware was developed to handle signal acquisition and BLE communication. The firmware consists of 3 parts:

- **Initialization:** Sets up the I^2C protocol to communicate with the DAC and ADC, also sets up the DAC and ADC for voltage controlling and initializing BLE settings.
- **Main Loop:** Continuously monitors BLE connection status, reads sensor data, sends updates via BLE, and listens for control commands.
- **Event Handling:** Handles BLE connection and disconnection.

Library Imports and Setup

The firmware begins by importing essential libraries and modules that support I^2C communication, ADC and DAC control, BLE communication, and data handling. The lookup tables LUT_A and LUT_B are used for a calibrated DAC output coming from section 4.2.

```
import time
import board
import busio
import math
from adafruit_bus_device.i2c_device import I2CDevice
import adafruit_ads1x15.ads1115 as ADS
from adafruit_ads1x15.analog_in import AnalogIn
from adafruit_ble import BLERadio
from adafruit_ble.advertising.standard import ProvideServicesAdvertisement
from adafruit_ble.services.nordic import UARTService

from lutB import LUT_B --> Lookup table for CHANNEL B
from lutA import LUT_A --> Lookup table for CHANNEL A
```

The first initialization is the I^2C protocol to allow detection of the addresses from the DAC and ADC.

```
i2c = busio.I2C(board.SCL, board.SDA)
```

DAC Initialization

The firmware communicates with an AD5667R DAC over the I^2C bus, which can be found in section 3.3.5. A helper class (AD5667) is defined to simplify sending 24-bit word commands to the DAC, which expects 8 command bits and a 16-bit data word.

```
DAC_ADDRESS = 0x0F

DAC_A = 0x00
DAC_B = 0x01

class AD5667:
    def __init__(self, i2c, address):
        self.i2c_device = I2CDevice(i2c, address)

    def write_data(self, command, value):
        if value < 0 or value > 65535:
```

```
            raise ValueError("Value must be between 0 and 65535")

        msb = (value >> 8) & 0xFF
        lsb = value & 0xFF

        with self.i2c_device as i2c:
            i2c.write(bytes([command, msb, lsb]))

dac = AD5667(i2c, DAC_ADDRESS)

def find_best_dac_value(target_voltage, lut):
    return lut[min(lut.keys(), key=lambda v: abs(v - target_voltage))]
```

The variable DAC_ADDRESS specifies the I^2C address of the AD5667R DAC, while DAC_A and DAC_B represent the command bits used to select the two output channels of the DAC. The AD5667 class encapsulates the I^2C communication protocol required to interact with the DAC, constructing and sending 24-bit commands composed of a command byte and a 16-bit data word, which is split into a most significant byte (MSB) and a least significant byte (LSB). The write_data method ensures that the input value is within the valid 16-bit range, splits it into two bytes, and transmits the formatted data over I^2C to the DAC. Afterwards, the DAC instance is initialized with the I^2C bus and the DAC's address. Finally, a function called find_best_dac_value() helps in looking for the digital value which matches the target output voltage inside the lookup tables.

ADC Initialization

The firmware sets up an ADS1115 ADC connected via the I^2C bus. This converter reads analog signals from the measurement system, as mentioned in section 3.3.12.

```
# Create ADS1115 object
ads = ADS.ADS1115(i2c)
ads.gain = 2

# Initialize ADC channels
chan0 = AnalogIn(ads, ADS.P0)
chan1 = AnalogIn(ads, ADS.P1)
chan2 = AnalogIn(ads, ADS.P2)
chan3 = AnalogIn(ads, ADS.P3)
```

The ADS1115 ADC is initialized with a function from the ads1x15 library and connects to the I^2C bus. The gain is set to 2, configuring the ADC's input range for higher resolution in the desired voltage range, which is mentioned in section 3.2.2. Four analog input channels are initialized (P0 to P3), each capable of reading voltages from different parts of the measurement setup, connections of these channels can be found in section 3.4.

Parsing of Received Values

The firmware implements two parsing functions to configure the required measurement parameters and synchronization data transmitted through the BLE UART interface.

```
def parse_received_time(received_time):
    global last_update
    try:
```

```
        _, time_part = received_time.split()
        hh, mm, ss = map(int, time_part.split(":"))
        last_update = time.monotonic()
        return hh, mm, ss
    except ValueError:
        return None

def parse_received_setup(received_setup):
    try:
        drain_source_voltage, gate_voltage, cycles, duration = map(float,
   received_setup.split("/"))
        cycles = int(float(cycles))
        return drain_source_voltage, gate_voltage, cycles, duration
    except ValueError as e:
        return None, None, None
```

The parse_received_setup function decodes setup instructions provided as a string with fields separated by slashes (e.g., "0.5/0.3/2/1"). It extracts the drain-source voltage, gate voltage, number of cycles, and duration in minutes. The function converts these values to floating-point numbers.

The parse_received_time function processes time synchronization messages received over BLE (e.g., "TIME 12:34:56").

Main Loop and Measurement Logic

The main loop of the firmware uses the entire operation of the measurement system, handling BLE connection management, data acquisition, control commands, and data transmission. Upon startup, the system waits for a BLE connection from the external application. Once connected, it enters the measurement logic implemented in the log_current_over_time function.

```
RESET_COMMAND = "#AXH"

while True:
    while not ble.connected:
        pass  # Wait for BLE connection

    while ble.connected:
        log_current_over_time()

    reset_device()  # Reset everything when disconnected
    while uart.in_waiting:
        uart.read(uart.in_waiting)
    ble.start_advertising(advertisement, interval=0.1)
    time.sleep(1)

def log_current_over_time():
    # Wait for setup commands
    while duration == 0:
        dac.write_data(DAC_A, find_best_dac_value(0, LUT_A))
        dac.write_data(DAC_B, find_best_dac_value(0, LUT_B))
        # Listen for setup data or reset command

    # Synchronize with time received from control software
```

```
    while received_time is None and duration != 0:
    # Apply drain-source voltage
    dac.write_data(DAC_B, dac_value_B)
        # Wait for time sync and adjust DACs

    # Start measurement cycles
    for i in range(cycles):
        # Apply initial DACs, start timer
        while ble.connected and received_time is not None and duration != 0:

            # Apply gate voltage
            if elapsed_time == 10 #--> timing of gate voltage
                dac.write_data(DAC_A, dac_value_A)

            # Measure currents
            Ids = chan2.voltage #--> ADC voltage channel 2
            Igs = chan3.voltage #--> ADC voltage channel 3
            # transmit data
            sensor_data = f"{elapsed_time:.2f},{Ids:.4f},{Igs:.4f}\n"
            uart.write(sensor_data.encode("utf-8"))
            # listen for reset
             if uart.in_waiting > 0:
                raw_data = uart.read(20)
```

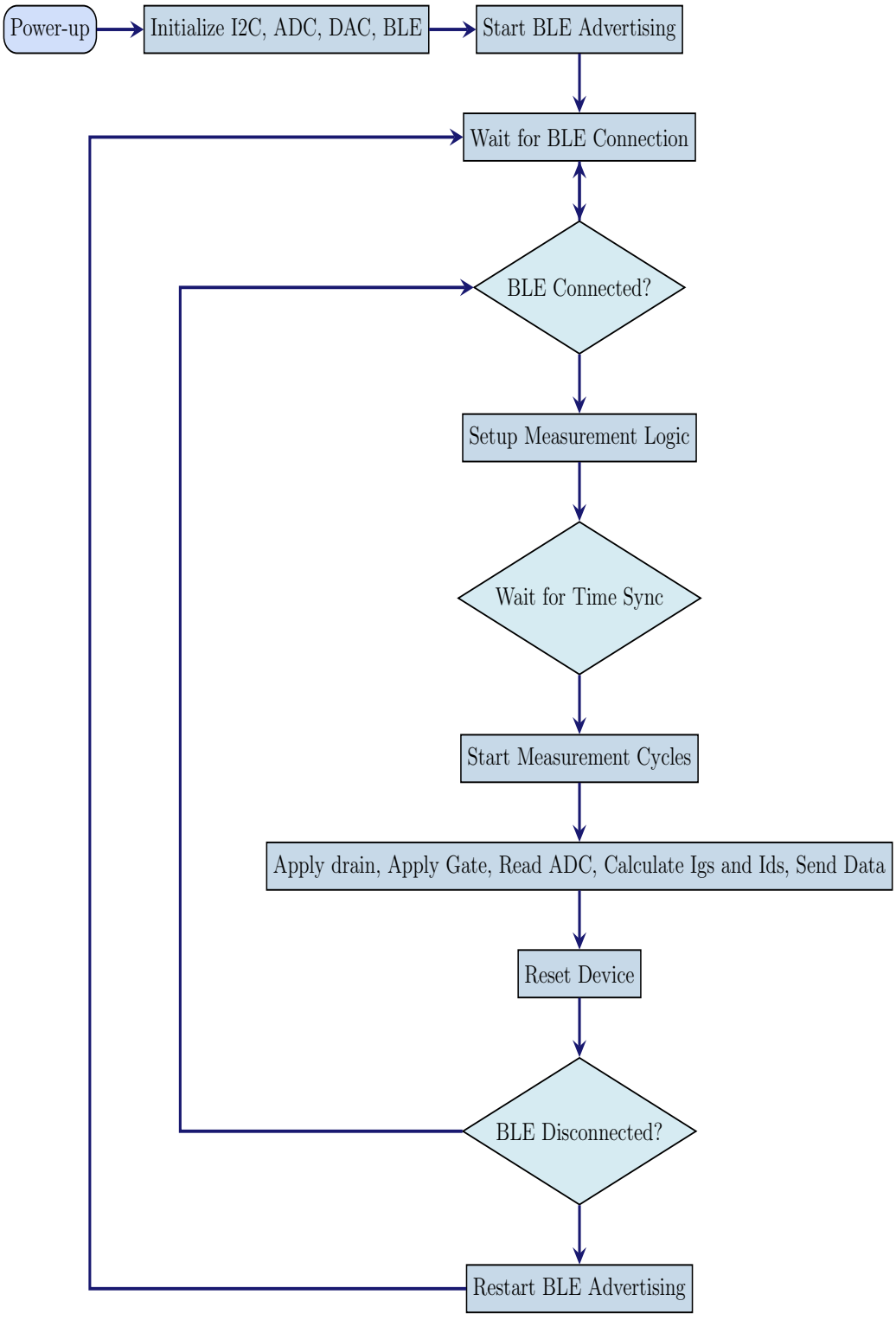
The "log current over time" function, which handles parameter setup, DAC voltage adjustment, and data acquisition. This function waits for setup parameters and time synchronization before starting measurement cycles. Once the setup is complete it first applies the drain-source voltage before starting the cycles, this ensures that the applied drain-source voltage is the same for all cycles. During each cycle, it applies the gate voltage after 10 seconds, measures drain-source and gate currents. While doing all this it also measures time, which is then packaged together with the currents and transmitted. After it completed the measurements duration the gate voltage is removed again before starting the next cycle. It listens for reset commands throughout. Upon disconnection, the firmware resets all parameters and goes back to BLE advertising.

Summary of firmware

The code operates as follows: after powering up, the microcontroller initializes the various components, including I^2C, ADC, DAC, and BLE. Once initialization is complete, it starts advertising for a Bluetooth connection. When a device connects, the system waits to receive the setup parameters, such as the drain-source and gate-source voltages, the number of measurement cycles, and the duration of the measurement in minutes. After receiving these parameters, it waits for a start signal, which is sent as the current time by the user. Upon receiving this signal, the device begins the measurement process, applying the specified drain-source and gate-source voltages, and repeating the measurements for the specified number of cycles until the duration is complete. Once all cycles and the duration have been completed, the device resets and waits for new setup parameters. Throughout these steps, the microcontroller continuously checks for incoming messages from the user, including reset commands that cause the system to restart the setup process.

A flowchart of the code where the device undergoes one measurement cycle without interruption is displayed in the following workflow diagram.

Workflow Diagram



3.5.4 Bluetooth communication

On the embedded side, the nRF52840 uses CircuitPython's bleio module to implement BLE functionality. The system is configured as a BLE peripheral, exposing services and characteristics. Specifically, it uses standard UUIDs defined by the Nordic UART Service (NUS) to ensure communication between the embedded system and the desktop application. These standardized services simplify development and ensure compatibility with a wide range of BLE clients (applications) [51].

Bluetooth Low Energy (BLE) is particularly well-suited for embedded applications due to its low power consumption, making it ideal for battery-operated devices that require efficient wireless communication [51], [52].

The NUS service and characteristics are defined as follows:

- **Service UUID:** 6E400001-B5A3-F393-E0A9-E50E24DCCA9E
- **TX Characteristic (Notify):** 6E400003-B5A3-F393-E0A9-E50E24DCCA9E
- **RX Characteristic (Write):** 6E400002-B5A3-F393-E0A9-E50E24DCCA9E

The Flutter-based desktop application operates as a BLE central device, scanning for and connecting to the measurement device. Upon establishing a connection, the application subscribes to the TX characteristic to receive streaming measurement data from the peripheral (nRF52840) and writes to the RX characteristic to send commands (e.g., DAC adjustment parameters) to the microcontroller [52], [53].

By default, the standard BLE Maximum Transmission Unit (MTU) is 23 bytes, which corresponds to a payload of 20 bytes for data transmission. This means that each BLE packet can carry up to 20 characters (or digits) in a single transmission [54]. In practice, BLE central devices, such as smartphones or desktop applications, often use a connection interval between 30–50 ms by default, which determines how frequently data packets are exchanged. This interval represents a balance between energy efficiency and responsiveness and may vary depending on the requirements of the connected application [55].

For example, if the sensor readings are elapsed_time = 12.37, Ids = 15.3241, and Igs = 1.3242, the formatted string becomes 12.37,15.3241,1.3242. When this string is UTF-8 encoded for transmission, it results in the following byte array:

[49, 50, 46, 51, 55, 44, 49, 53, 46, 51, 50, 52, 49, 44, 49, 46, 51, 50, 52, 50]

This array contains 20 bytes in total, and the communication is configured to occur in both directions: from the application to the device and from the device to the application, using this same data format.

3.5.5 Windows application

A custom-built Windows application was developed using Flutter, a popular cross-platform UI (User Interface) framework. Flutter enables the development of applications for multiple platforms such as desktop, web, and mobile, all compiled from a single codebase [56]. This cross-platform capability provided the flexibility to develop a control interface for the OECT Controller while ensuring scalability for potential future expansions.

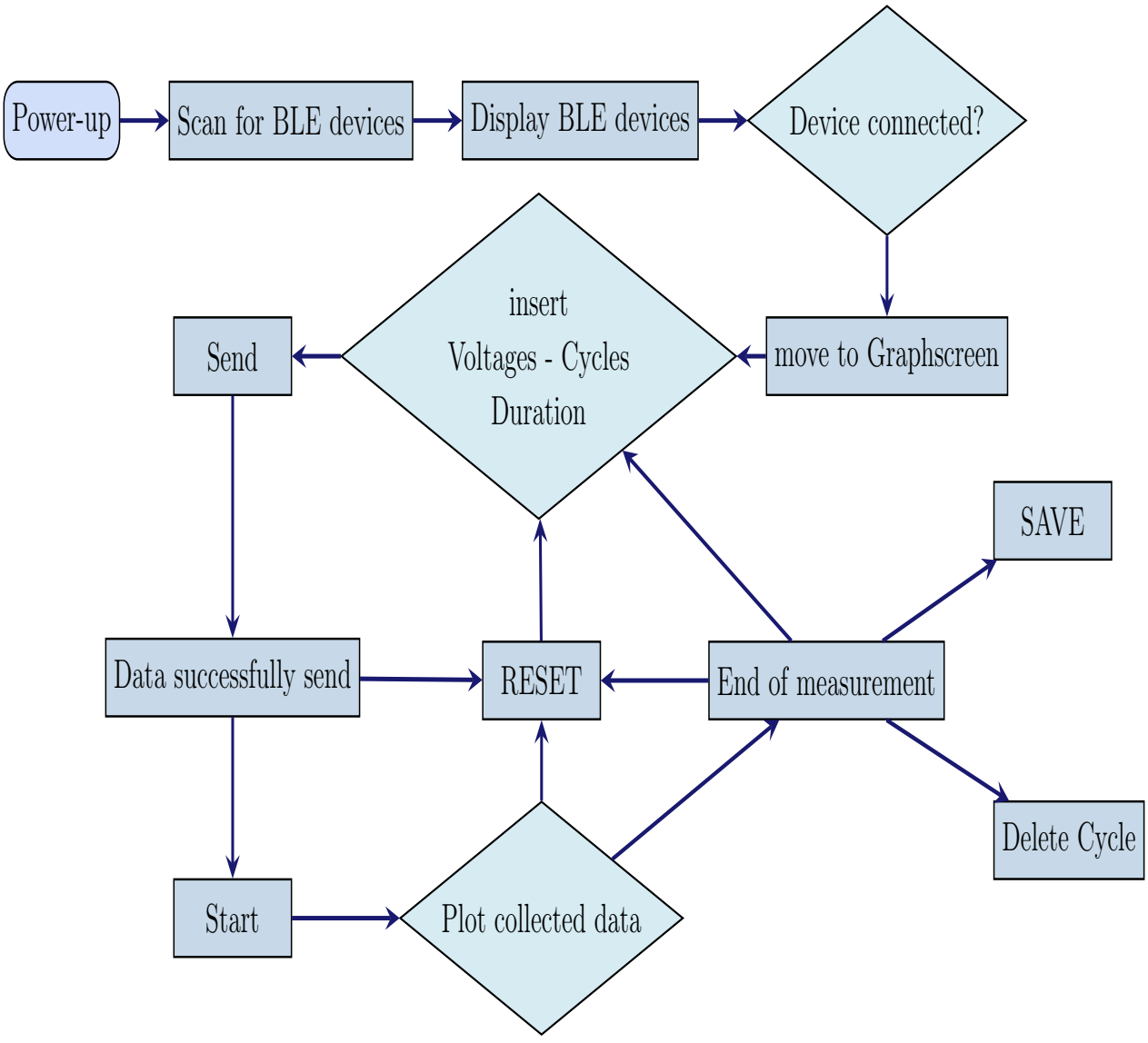
The decision to use Flutter was influenced by its rich set of widgets and support for reactive programming, which accelerated the development process. Its compatibility with Windows desktop applications made it a suitable choice for this project, allowing the creation of a user-friendly control application. In addition, Flutter's libraries of pre-built components and customizable widgets simplified the development of a consistent, high-quality interface with minimal effort [56].

Flutter has been used by companies like Google (for Google Ads and parts of Google Pay) and

BMW (for the My BMW app). Other users, such as Philips Hue as well. These users highlight Flutter's reliability and versatility [56]. By using Flutter's prehanded functionalities and its freedom in creativity, the OECT Controller's desktop application was able to achieve a standard of design and functionality.

The Windows application operates as follows: upon starting the program, it scans for available BLE devices and displays a list of those containing the name "OECT Device ...". When a device is selected, the program attempts to connect. If the connection is successful, it navigates to a new screen where text fields allow adjustment of parameters such as drain-source and gate-source voltages, the number of measurement cycles, and the measurement duration. Once these parameters are sent, the program confirms whether the message was successfully transmitted or if an error occurred. After sending the parameters, a start button becomes available to initiate time synchronization. Once synchronization is complete, the program begins collecting and plotting incoming data points in real time. At the end of the measurement, the user can save the data and start a new measurement, restarting the loop. Additionally, the user can reset the system at any time to adjust parameters and restart the process with an empty plot.

Workflow Diagram



Chapter 4

Results and Discussion

To validate the performance of the physical measurement system, several testing procedures were developed to assess both the voltage output and current sensing functionalities.

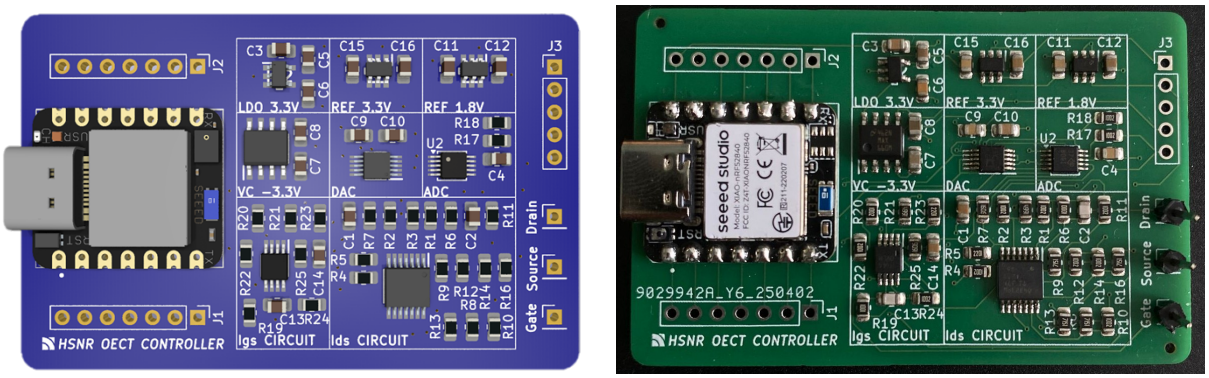
For voltage control, the output of the digital to analog converter is swept across its full range, with each voltage level verified using a multimeter. For current sensing, a known reference current is sourced into the system, and the measured output is compared to the expected value.

To evaluate both the voltage application and current sensing simultaneously, Ohm's law is applied using a known resistor: a specific voltage is applied, and the resulting current is measured and compared to the theoretical value.

Finally, the complete system is tested using a benchmarked N-channel junction field effect transistor (N JFET), where both V_{gs} and V_{ds} are swept to analyze the input and output behavior of the I_{ds} and I_{gs} measurement circuits.

4.1 PCB design

Starting with the PCB design verification. Figure 4.1 and Figure 4.2 show the comparison between the designed PCB in KiCad and the manufactured and assembled PCB by JLCPCB for the measuring system. Figure 4.1 shows that all major components are organized into clearly labeled sections in case of debugging and signal tracing.

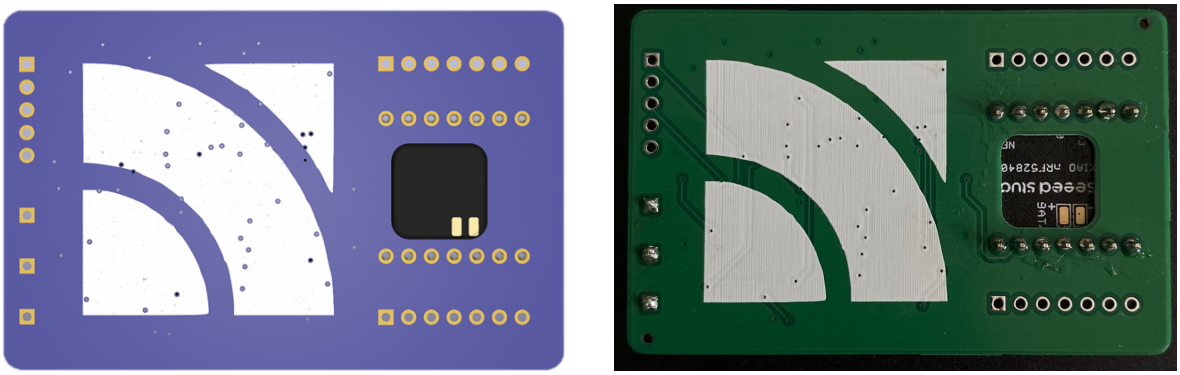


(a) (b)

Figure 4.1: *Top (b) and bottom (a) views of the manufactured OECT controller PCB.*

In Figure 4.1(a) and Figure 4.1(b), the microcontroller is positioned on the left side of the PCB, with its connections routed to both the top and bottom layers. The bottom side features the name of this device: *HSNR OECT CONTROLLER*. The central area of the PCB contains the main hardware blocks, each clearly labeled for identification. On the right side, the connectors for the *Gate*, *Drain*, and *Source* electrodes are positioned, with additional validation connections located directly above them.

Figure 4.2(a) and Figure 4.2(b) display the bottom view of the PCB. In the middle is the Hochschule Niederrhein logo, and a hole below the microcontroller exposes the pads for an optional battery connection to the MCU.



(a) (b)

Figure 4.2: *Top (b) and bottom (a) views of the designed OECT controller PCB in KiCad.*

The manufactured printed circuit board measures 6 cm by 4 cm, aligns well with the original design, and shows no noticeable connectivity issues that could impact the intended functionality of the device. A green solder mask was used, as it is the most economical option offered by manufacturers like JLCPCB. Testing confirmed stable performance, with no errors detected during the initialization process, as detailed in Section 3.5.3.

However, this PCB remains a prototype, intended to integrate all components onto a single board without isolating and validating individual connections. As a potential improvement, monitoring each signal line during operation could provide more insights into system limitations and help assess the signal integrity of the layout more thoroughly.

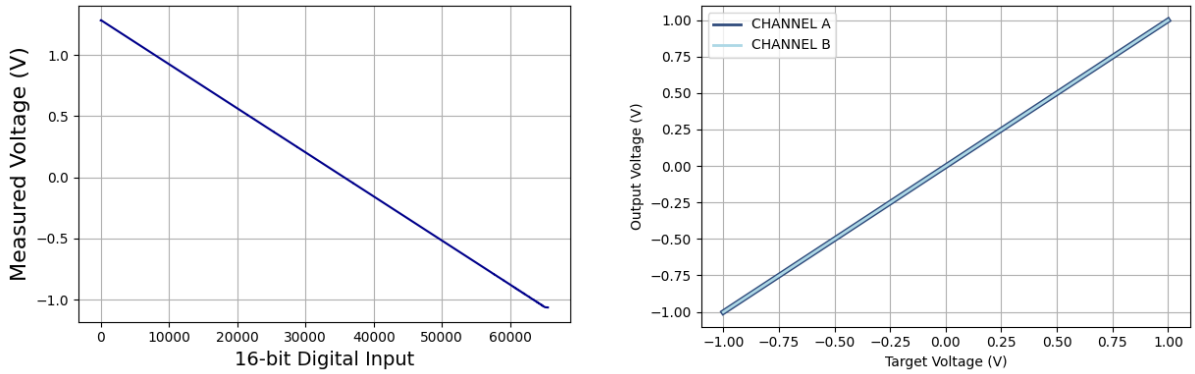
4.2 DAC validation and calibration

To evaluate the performance of the voltage applying side, the digital to analog converter and the differential amplifier are tested using a known resistor placed at the R_x position, as described in Section 3.3.12. A multimeter (PeakTech 4000) is connected in parallel to measure the resulting output voltage. A Python script is used to sequentially read the digital values going to the DAC, ranging from 0 to its full-scale value (65535). After each update, the corresponding output voltage is recorded by that same script, via the multimeter.

This procedure enables the generation of a voltage to code lookup table, allowing for precise voltage control in future measurements. Two resistors, 55 Ω and 550 Ω, were used to test both DAC channels, selected to match the calculated values of R_x from Section 3.2.2. This ensures

that the circuit operates well within its dynamic range during calibration and avoids saturation or clipping effects.

Figure 4.3(a) shows the measured output voltage from the differential amplifier, plotted against the corresponding digital input values to the DAC. The measured voltages range from a minimum of $-1.0644\,\mathrm{V}$ to a maximum of $1.2843\,\mathrm{V}$, demonstrating the combined linearity of the DAC and the differential amplifier. These values align closely with the calculated ones presented in Section 3.2.2. At the maximum output of the differential amplifier, a flattening of the voltage response is observed, which may result from non-linearity or saturation effects. However, since the required output voltage reaches the $\pm 1\,\mathrm{V}$ range of the OECT, the DAC and differential amplifier perform as intended.



(a) (b)

Figure 4.3: *(a) Measured output voltage of the differential amplifier plotted against DAC digital input value. (b) Measured output voltage versus target voltage, showing calibration linearity across both DAC channels.*

To ensure accurate voltage generation, a lookup table was created that maps measured output voltages to their corresponding digital code values. This aligns the target voltages with the required digital input values for the DAC. Table 4.1 provides an example of this lookup table: for Channel A, it includes voltages ranging from $-1.00\,\mathrm{V}$ to $-0.91\,\mathrm{V}$, and Channel B, covering voltages from $1.00\,\mathrm{V}$ to $0.91\,\mathrm{V}$, as presented in Table 4.1.

Table 4.1: *Example of the DAC lookup table for Channel A (negative range) and Channel B (positive range).*

Channel A		**Channel B**	
Target V	**Digital Code**	**Target V**	**Digital Code**
-1.00	63389	1.00	7899
-0.99	63093	0.99	8173
-0.98	62814	0.98	8453
-0.97	62538	0.97	8729
-0.96	62271	0.96	9007
-0.95	61984	0.95	9283
-0.94	61706	0.94	9563
-0.93	61428	0.93	9839
-0.92	61158	0.92	10115
-0.91	60876	0.91	10393

Figure 4.3(b) illustrates the performance of the differential amplifier combined with the calibrated digital-to-analog converter, showing the measured output voltage plotted against the target voltage. The system accurately covers the full range from $-1\,\mathrm{V}$ to $1\,\mathrm{V}$, with an error of approximately $\pm 0.2\,\mathrm{mV}$. For reference, a $0.2\,\mathrm{mV}$ error on a $0.01\,\mathrm{V}$ step corresponds to a 2% relative error. This demonstrates that the output stage of the OECT controller performs as intended and meets the design objectives of this thesis, enabling the user to apply a reliable and accurate voltage to the OECT.

However, the voltage application side of the system could benefit from further optimization. The UWED device, mentioned in Section 3.1.2, implements a dual amplifier filtering technique to achieve greater voltage stability and increased accuracy [32]. While this approach enhances performance, it also increases component usage and circuit complexity.

4.3 Current sensing

To validate the accuracy of the current sensing circuit, a known current is applied using a precision Source Measurement Unit (SMU). The measured current from the evaluation unit is then compared to the SMU (Keysight B9xxBL) reference to study the precision and linearity of the current sensing functionality. This validation method evaluates the performance of the transimpedance amplifier, the summing amplifier, and the ADC converter of the OECT controller.

Since the two systems start their measurement at different times, their data is aligned by normalizing the time index to a 0–1 range and interpolating the SMU data onto the evaluation unit's x-axis. This allows comparison between 2 datasets that differ in a time-scale [57]. With this an accuracy can be calculated between the two datasets and verify the performance of the transimpedance and summing amplifier stages, as well as the ADC.

The error between the measured and expected currents is given by:

$$\text{Error} = I_{\text{measured}} - I_{\text{expected}} \tag{4.1}$$

From this, the measurement accuracy can be determined using the following formula:

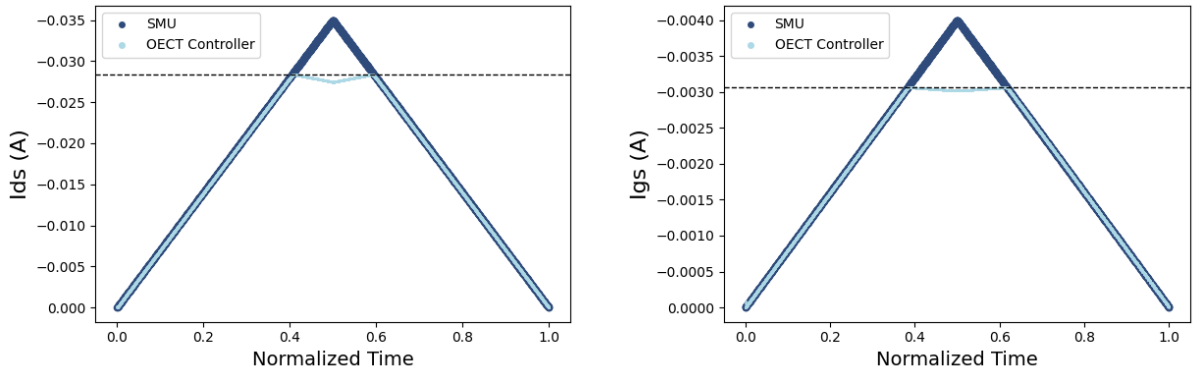
$$\text{Accuracy } (\%) = \frac{|\text{Error}|}{I_{\text{expected}}} \tag{4.2}$$

Figure 4.4 shows a comparison between the current measurements performed by the OECT controller and those sourced by a SMU. The SMU applies a linearly decreasing current.

In Figure 4.4(a), the dashed line shows the minimum measurable current on the I_{ds} channel by the OECT controller, measured at $-28.3768\,\mathrm{mA}$. Similarly, Figure 4.4(b) shows the I_{gs} channel with a minimum measurable current of $-3.0600\,\mathrm{mA}$. For the I_{gs} channel, the minimum closely approaches the calculated lower bound from Section 3.3.12, indicating that the system performs as intended for negative current measurements on this channel.

In contrast, the minimum current measured on the I_{ds} side differs by approximately $1.7\,\mathrm{mA}$ from the calculated lower bound presented in Section 3.3.12. This unexpected behavior may result from the calibration process, as the device was calibrated only on the voltage output side,

while the current sensing side remained uncalibrated. Consequently, the current calculation still contains a systematic error, as it was derived using estimated resistor values and ideal op-amp conditions.

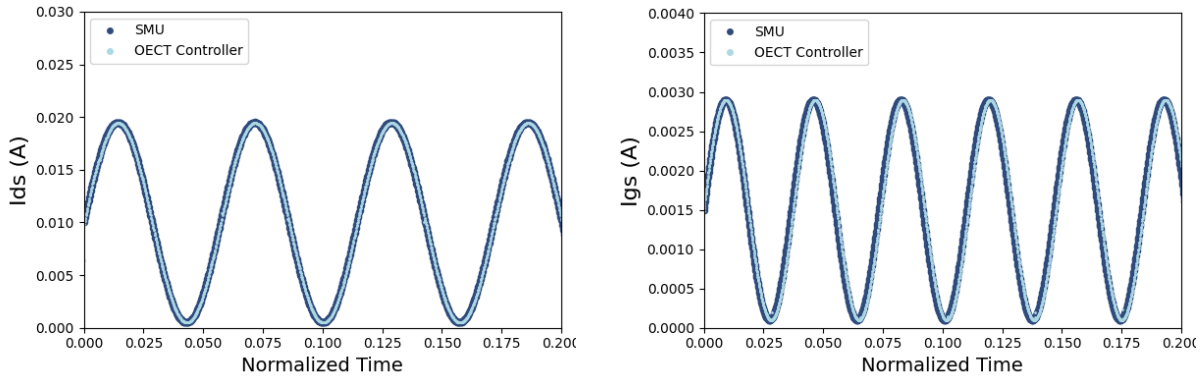


(a) (b)

Figure 4.4: *Comparison of current measurements between the SMU and the OECT controller for the I_{ds} (a) and I_{gs} (b) channels. The dashed line indicates the minimum current measurable by the OECT controller. The x-axis represents normalized time.*

Additionally, this error also contains the inherent offset of the OPAx323, particularly in the I_{ds} circuit, where the op-amp is used in all three stages. In contrast, in the I_{gs} circuit, the OPAx323 is only used in the differential amplifier, contributing offset only to the voltage output side of the circuit. This difference could further enlarge the offset and measurement difference observed on the I_{ds} side compared with the expected value.

The average measurement accuracy for the I_{ds} channel is 97.01%, while the I_{gs} channel achieves an average accuracy of 95.57%. These values fall within the intended accuracy range for the sensing side.



(a) (b)

Figure 4.5: *Comparison of I_{ds} (a) and I_{gs} (b) measurements for a dynamic 0.1 Hz sine wave current sourced by the SMU. The x-axis shows normalized time, zoomed in to the 0–0.2 range to highlight the area near the signal's rising edge and falling edge.*

Figure 4.5 illustrates the OECT controller's response to a dynamic, positive 0.1 Hz sine wave current applied by the SMU, with the current applied for different durations across the two channels. On both channels, the OECT controller operates effectively on the sensing side, demonstrating

that the desired measurement ranges are achieved, as described in Section 3.3.12. However, on the I_{gs} side, a slight phase shift in the alignment of the two datasets is observed, which remains constant over time. This shift is more likely caused by the data alignment procedure rather than systematic errors or inherent delay, although this cannot be excluded without performing multiple measurement cycles.

The accuracy of the measurements in this test is shown in Figures 4.5(a) and 4.5(b), with the I_{ds} channel achieving an average measurement accuracy of 97.88% and the I_{gs} channel reaching 90.83%. Although these values differ noticeably from the previously reported negative current measurements, this difference is likely due to the same data alignment issues, rather than systematic errors. It is also important to note that the current sensing side was uncalibrated in both cases, which did have an impact on the results. Nevertheless, the findings confirm that the current sensing functionality of the device functions as intended and meets the design objectives of this thesis, enabling the user to sense current from the OECT.

4.4 Ohm's law validation

To evaluate the overall accuracy of the measurement system, known resistor values of 55 Ω and 550 Ω are connected between the measurement terminals (Drain, Source and Gate). By applying a known voltage across these resistors and measuring the resulting current, the performance of both the voltage applying and current sensing sides of the system can be validated against the theoretical value derived from Ohm's law.

The expected current is calculated using:

$$I_{\text{expected}} = \frac{V_{\text{applied}}}{R} \tag{4.3}$$

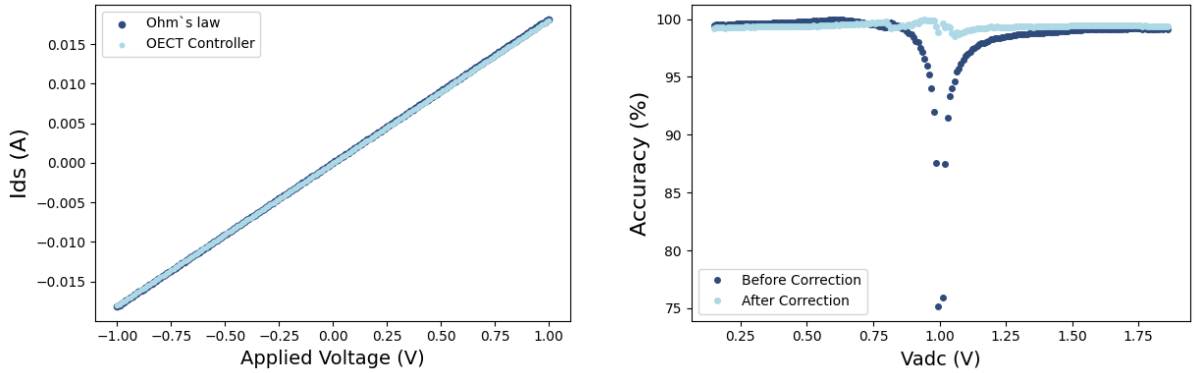
Using this expected current, the measurement accuracy can be determined with the same formula introduced in Section 4.3. This validation step also supports refinement of the current calculation formulas for I_{gs} and I_{ds}, as described in Section 3.3.12.

Figure 4.6(a) compares the theoretical current, calculated using Ohm's law for a 55 Ω resistor, with the measured I_{ds} current from the OECT controller. The applied voltage from channel B ranges from −1 V to 1 V in steps of 0.01 V. The comparison reveals a systematic offset of −43.11 μA between the measured and theoretical currents.

This offset may be caused because of several factors. First, the formula used to calculate I_{ds} (as described in Section 3.3.12) was derived using estimated resistor values without accounting for their tolerance. Second, the inherent offset of the OPAx323 operational amplifier, mentioned in Section 3.3.10, could contribute to the observed deviation. Third, the error of ±0.2 mV on the voltage application side may also influence the measurements. Finally, the inherent noise of the ADC component, described in Section 3.3.6, adds to the overall offset.

Combining these factors, a systematic offset in the measured current was likely to occur.

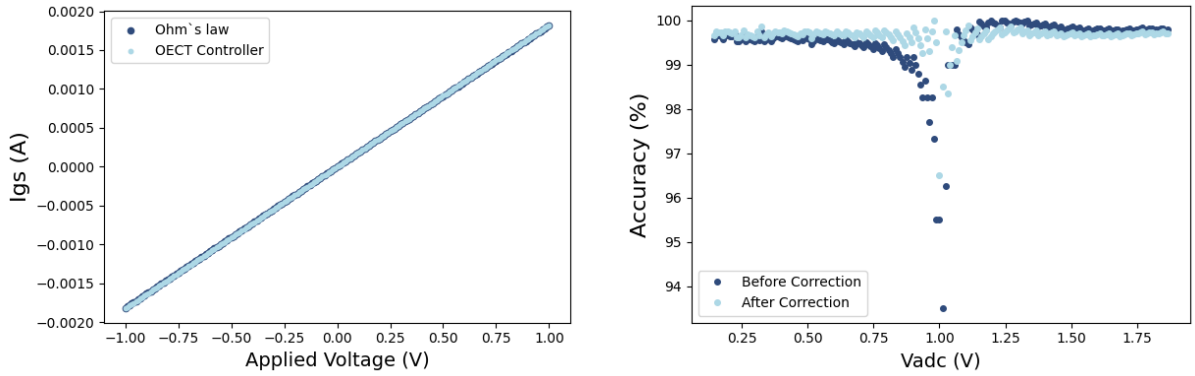
Before applying this offset correction, the mean measurement accuracy is 98.52%. After correction, the mean accuracy improves to 99.39%.



(a) (b)

Figure 4.6: *(a) Comparison between the theoretical current (Ohm's law) and the measured I_{ds} from the OECT Controller using a 55 Ω resistor. (b) Accuracy of the current measurement before and after offset correction, plotted versus the voltage read by the ADC.*

Figure 4.6(b) shows the accuracy of each applied voltage, between the measurements before and after applying the offset, plotted against the voltage read by the ADC. The ADC input voltage remains between 0 V and 2 V as intended through the use of the summing amplifier mentioned in section 3.2.2. Notice the accuracy drops to approximately 75% near an applied voltage of 0 V, where current values are smallest and measurement noise or error has a larger relative impact.



(a) (b)

Figure 4.7: *(a) Comparison between the theoretical current (Ohm's law) and the measured I_{gs} from the OECT Controller using a 550 Ω resistor. (b) Accuracy of the current measurement before and after offset correction, plotted versus the ADC voltage.*

Figure 4.7(a) compares the theoretical current, calculated using Ohm's law for a 550 Ω resistor, with the measured I_{gs} current from the OECT controller. The applied voltage from channel A ranges from −1 V to 1 V in steps of 0.01 V. The comparison reveals a systematic offset of −1.45 μA between the measured and theoretical currents.

When compared to the systematic offset observed in the I_{ds} circuit, this offset is significantly smaller. This difference could be because of similar factors to those identified in the I_{ds} circuit. In the I_{gs} circuit, the OPAx192 operational amplifier was used, which has a lower offset voltage and higher precision, as described in Section 3.3.10. Additionally, the transimpedance amplifier in this circuit uses a higher feedback resistor (gain), contributing to improved measurement accuracy. It is also worth noting that the resistors used as R_X to test these current measurements were not

high-precision resistors, which may have introduced additional error due to their tolerance not being accounted for.

Before applying this offset correction, the mean measurement accuracy is 99.50%. After correction, the mean accuracy improves to 99.65%.

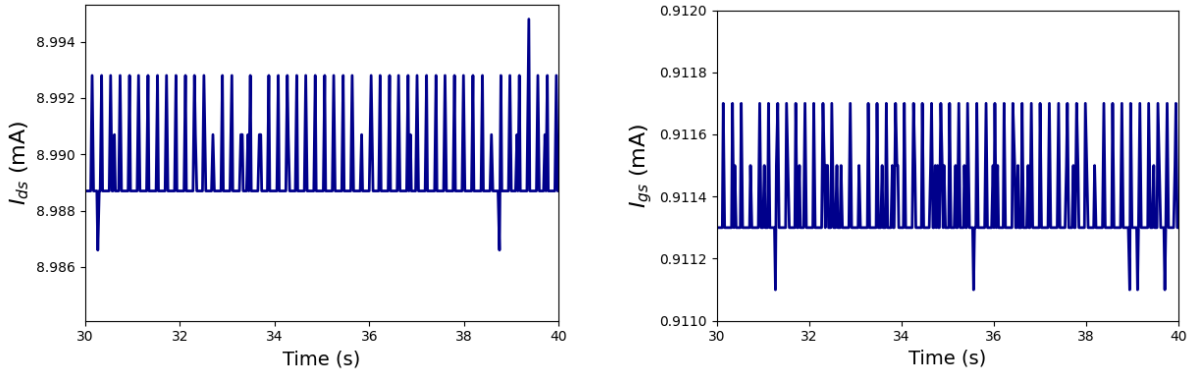
Figure 4.7(b) shows the accuracy of each applied voltage, comparing measurements before and after applying the offset, plotted against the ADC input voltage. The ADC input voltage ranges in between 0 V to 2 V, as intended through the use of the summing amplifier mentioned in section 3.2.2. Notably, the accuracy drops to approximately 93.50% near an applied voltage of 0 V. This decrease is likely due to the same cause identified in the I_{ds} circuit, where the current values are smallest and measurement noise or error has a larger relative impact.

4.5 Signal-to-noise

To evaluate the signal quality of the measurement system, the noise was observed for the I_{ds} and I_{gs} current measurements by applying a stable voltage over a resistor of known value (e.g., 55 Ω and 550 Ω), while the current fluctuations over time were recorded to determine the noise level.

Figure 4.8(a) shows the noise on the I_{ds} channel when a constant voltage is applied across a 55 Ω resistor. The fluctuation on the signal is approximately 8 μA.

Figure 4.8(b) presents the noise on the I_{gs} channel with a 550 Ω resistor under similar constant voltage conditions. The observed fluctuation is approximately 0.6 μA.



(a) (b)

Figure 4.8: *Measured signal noise with constant voltage applied across (a) a 55 Ω resistor for I_{ds} channel and (b) a 550 Ω resistor for I_{gs}.*

This noise represents the entire systems noise, spanning from the DAC to the ADC, and including the differential amplifier, transimpedance amplifier, and summing amplifier. Although the ADC introduces its own noise, as discussed in Section 3.3.6, the observed noise difference between the two channels is likely due to the factor of 10 difference in the feedback resistor (R_f) of the transimpedance amplifier. This difference in R_f results in a corresponding factor of 10 difference in the cut-off frequency of the transimpedance amplifier, as described in Section 3.2.2. Furthermore, the difference in amplifier components used in the two circuits contributes to this difference: the I_{ds} circuit uses a lower-cost general-purpose op-amp, while the I_{gs} circuit uses a higher-precision, more expensive op-amp.

However, this problem can be addressed by implementing additional filtering techniques beyond just a feedback capacitor on the transimpedance amplifier and a low pass filter at the output of the summing amplifier. Another approach is to adjust the sample rate of the analog to digital converter, as discussed in Section 3.3.6, where lower sampling rates tend to introduce less noise from the ADC itself.

A simpler method is to apply averaging, where a defined number of consecutive data points are collected and the mean value is used as the output. This technique reduces noise at the cost of sampling speed [58].

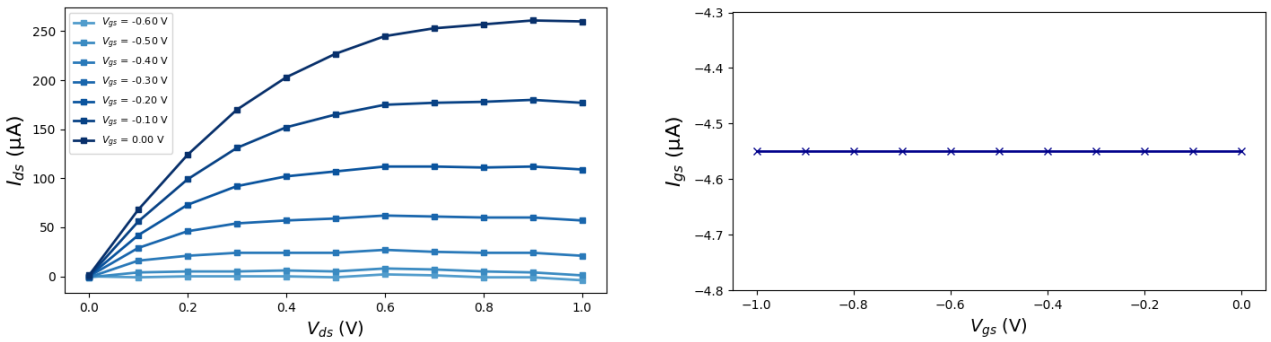
4.6 Transistor test results

As a final validation step, the accuracy and functionality of the complete measurement system is tested with a benchmark transistor, which can be tested under controlled conditions. In this setup, known voltages are applied to the gate and drain terminals of the transistor, while the resulting gate-source current I_{gs} and drain-source current I_{ds} are measured by the system.

The device under test is the J201, an N-channel junction field effect transistor (N-JFET). This transistor was selected because its threshold voltage falls within the operational limits of the measurement system [59], and because JFETs have behavior that is closely aligned with that of organic electrochemical transistors [60].

Junction field effect transistors regulate the flow of current between the drain and source terminals through a semiconducting channel, which is modulated by the gate voltage. In N-channel devices, a negative gate to source voltage increases the depletion region and narrows the channel, thereby reducing current flow. This type of depletion mode operation, where the device is normally conductive and becomes less conductive as gate voltage increases, resembles the behavior of many organic electrochemical transistors [60].

To evaluate measurement accuracy, the electrical characteristics of the J201 are compared with those obtained from a reference setup consisting of two precision power supplies (SPS5081X) and a calibrated multimeter (PeakTech 4000). This comparison enables a direct view of the OECT controller's ability to capture the transistor's behavior.



(a) (b)

Figure 4.9: *Measured characteristics of a J201 N-channel JFET using the OECT Controller. (a) Transfer characteristics (I_{ds} vs V_{ds}) for varying V_{gs}. (b) Gate current I_{gs} showing a constant current of approximately 4.55 μA.*

Figure 4.9 shows the measured characteristics of the J201 N-channel JFET using the OECT controller. Figure 4.9(a) shows the transfer characteristics (I_{ds} versus V_{ds}) for varying gate to source voltages (V_{gs}) from 0 to $-0.6\,\mathrm{V}$ in steps of $0.1\,\mathrm{V}$. The drain to source voltage (V_{ds}) was swept from 0 to $1\,\mathrm{V}$ in steps of $0.5\,\mathrm{V}$. Figure 4.9(b) shows the corresponding gate current (I_{gs}), where a nearly constant gate leakage current of approximately $4.55\,\mu\mathrm{A}$ was observed.

While the expected gate leakage current of the J201 N channel JFET is approximately $100\,\mathrm{pA}$ [61], the measured value of $4.55\,\mu\mathrm{A}$ highlights the error introduced when measuring currents near zero.

Figure 4.10 compares the transfer characteristics of the J201 N channel JFET, measured using the OECT controller and the reference setup at Hochschule Niederrhein. The OECT measurements (solid lines) closely align with the reference measurements (dotted lines), with an absolute maximum deviation of approximately $8\,\mu\mathrm{A}$.

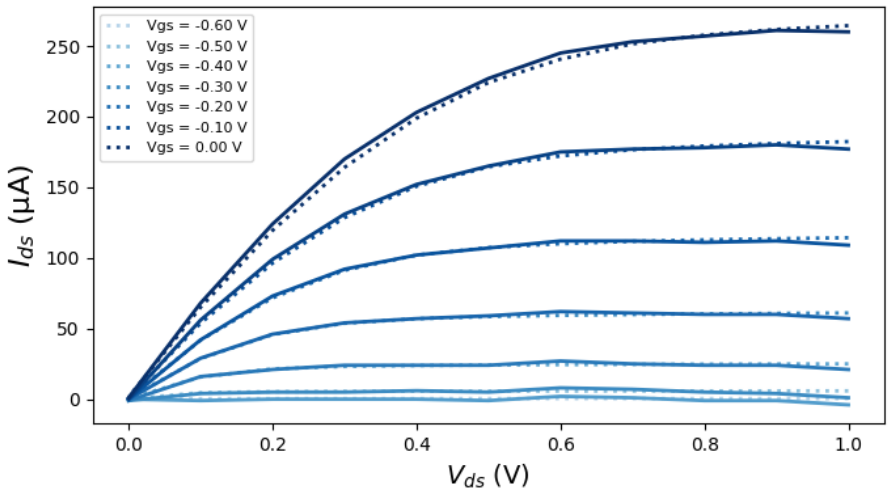


Figure 4.10: *Comparison of transfer characteristics of the J201 N-channel JFET measured with the OECT Controller (solid lines) and the setup at Hochschule Niederrhein (dotted lines).*

While this comparison shows generally good similarity, the differences observed between the OECT controller and the HSNR reference setup could be attributed to previously discussed factors. The absolute deviations measured here are consistent with the earlier noted signal to noise characteristics of both circuits, where noise fluctuations on the I_{DS} channel reached approximately $8\,\mu\mathrm{A}$.

The more noticeable differences at $V_{\mathrm{DS}} = 0.6\,\mathrm{V}$ and $1.0\,\mathrm{V}$ may result from limitations in DAC calibration, which introduces an error of approximately $\pm 0.2\,\mathrm{mV}$. As a result, voltages estimated as $0.6\,\mathrm{V}$ and $1.0\,\mathrm{V}$ may in reality be $0.6002\,\mathrm{V}$ and $0.9998\,\mathrm{V}$, which is an uncertainty that applies across the entire DAC output range.

Furthermore, the current sensing side was only "calibrated" by adding the average offset derived from the total range measured during the Ohm's law validation to the formula used to calculate both currents. This approach still results in small errors at individual measurement points. The combination of these factors likely explains the differences observed between the OECT controller and the HSNR setup.

A potential method for improving calibration on the sensing side involves redesigning the current sensing validation procedure. For each known sourced current, the corresponding raw byte value

read by the ADC could be recorded. Iterating this process across the full input range of the ADC would generate a lookup table that maps each digital code to a precise current value. Implementing this method for both sensing channels could significantly enhance current measurement accuracy. However, a limitation of this approach is the constrained memory capacity of the microcontroller, as discussed in Section 3.3.1, which may not be sufficient to store a detailed lookup table.

In addition to calibration techniques, further improvements in ADC and DAC stability could be achieved by using dedicated high precision voltage reference components, as discussed in section 3.2.3. Currently, the reference voltages for both the ADC and DAC are derived from the main supply lines, which are also shared with other system components. This can introduce variability and noise, whereas stable reference voltages would ensure more consistent and accurate performance [42].

4.7 OECT Measurement Setup with OECT controller

To complete the measurement setup for characterizing OECTs, a PCBite kit is used. This kit includes a magnetic platform with four holders and three flat cables connected to gold plated probes. The setup is shown in Figure 4.11, where the OECT controller is mounted on the PCBite platform and connected to the gate, drain, and source terminals, as described in Section 3.4.8. Specifically, the yellow cable connects to the gate, the blue cable to the drain, and the black cable to the source.

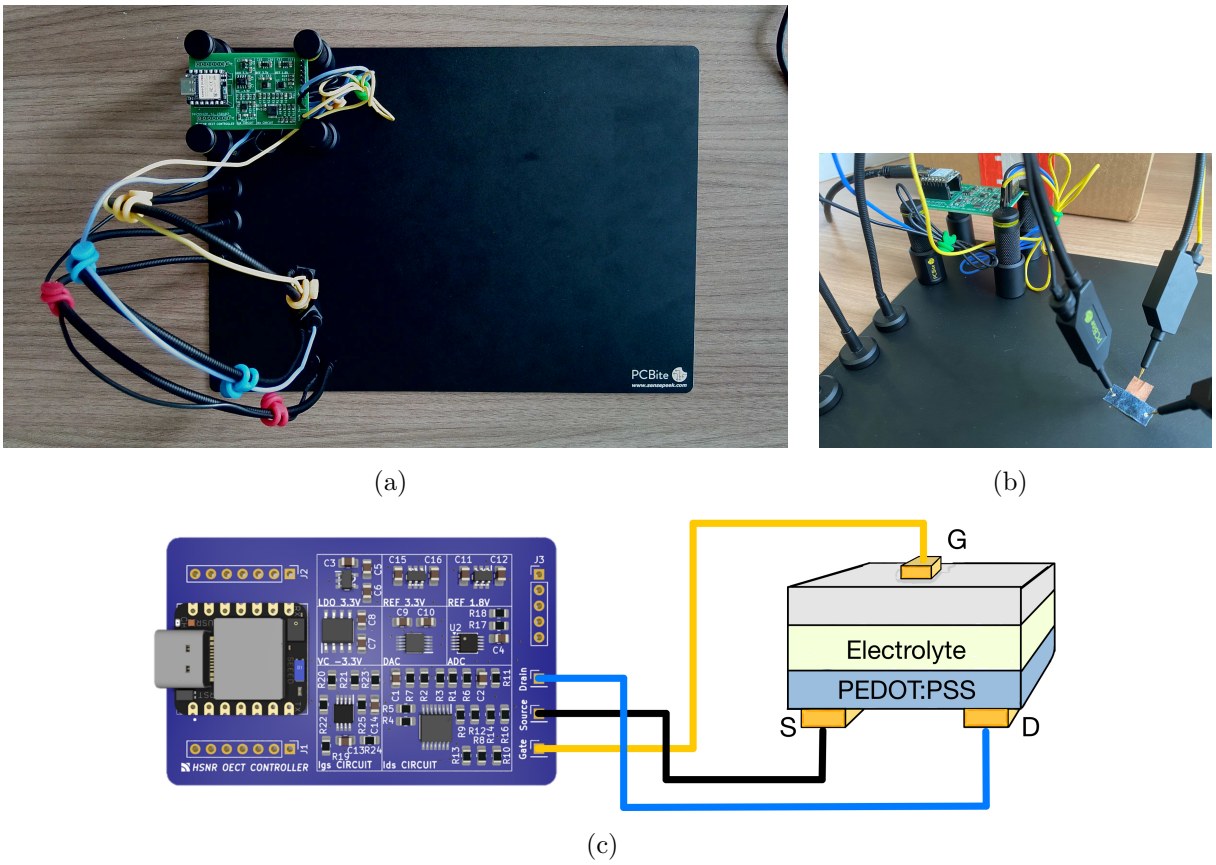


Figure 4.11: *OECT measurement setup using the PCBite platform. (a) The OECT controller placed on the magnetic platform. (b) Probe connections to the textile based OECT device. (c) Schematic illustration of gate (yellow), drain (blue), and source (black) probe connections.*

Figure 4.11 presents the complete setup. Figure 4.11(b) shows the probes placed on the surface of the textile based OECT device, following the connection method described in Section 2.2.5, and Figure 4.11(c) provides a schematic view of this configuration.

This configuration currently offers a practical and effective solution for connecting the OECT controller to the textile sensor. Although the controller is still in a prototype stage, holding it between the magnetic holders of the PCBite kit and using flat cable connections to gold plated probes ensures reliable connectivity. These probes meet the material requirements outlined in Section 2.2.4, and their flexibility allows for precise positioning on the sensor. Additionally, the compact size of the PCBite kit enhances the portability of the setup.

4.8 Custom Windows application

To enhance the interaction with the OECT controller and ease the measurement process, a custom Windows-based graphical user interface (GUI) was developed. This application allows users to control measurement parameters, monitor signals in real time, manage data, and perform multiple measurement cycles efficiently. The interface is designed to provide a user-friendly experience while enabling detailed control over the OECT controller. The measurement procedure of the Windows application and the OECT controller is based on the transient behavior of OECTs, as described in Section 2.3, in which the drain-source current is measured over time.

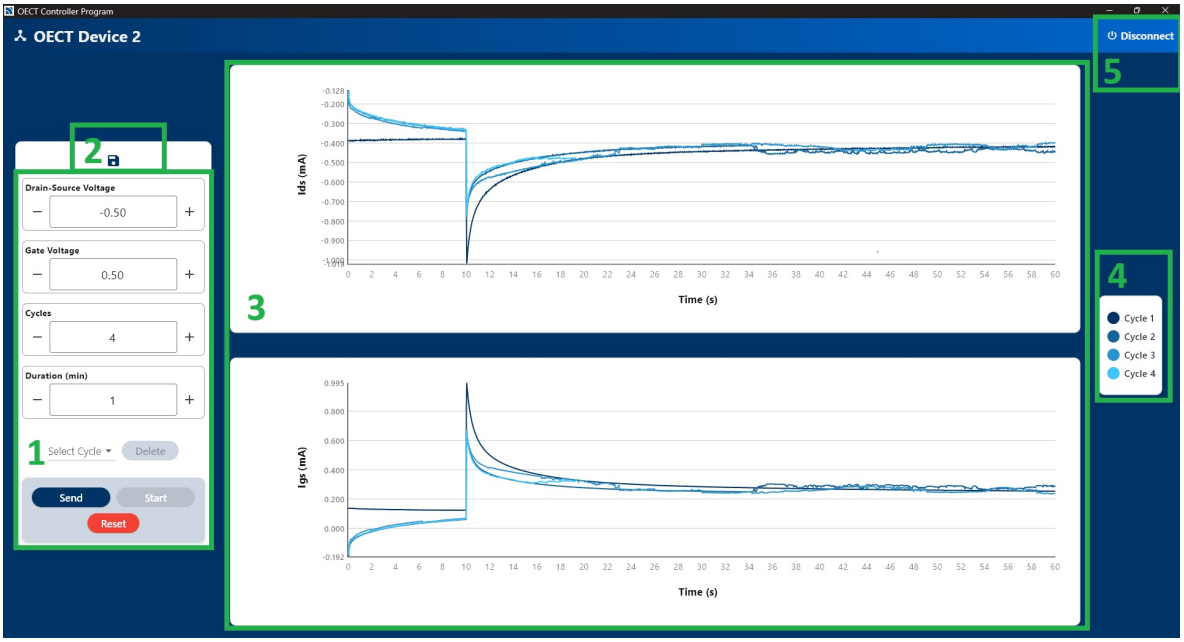


Figure 4.12: *Graphical interface of the custom Windows application. The green area, labeled as (1), contains fields to adjust measurement parameters, transmit them to the controller, initiate or reset measurements, and an option to delete a measurement cycle. Above this section, labeled as (2), is a save icon that enables exporting data to a .csv file. The central area, labeled as (3), contains two real-time plots: the top graph displays the drain current (I_{ds}), while the bottom graph shows the gate current (I_{gs}). On the right side, labeled as (4), is a legend for each data set (cycle), where users can select and rename individual cycles. In the top-right corner, labeled as (5), is the disconnect button.*

An overview of the application layout is shown in Figure 4.12, which highlights the key functional areas. The parameter control panel (1) allows users to define measurement settings such as V_{ds}, V_{gs}, and the duration of the measurement. These parameters can be transmitted to the controller,

and the user can initiate or reset the measurement sequence or delete specific measurements. Above this panel, the data export section (2) provides the option to save recorded data in .csv format for later analysis. The central plotting area (3) visualizes the drain-source current (I_{ds}) and gate-source current (I_{gs}) in real time with a sampling rate of 40 Hz. The legend panel (4) lists all recorded cycles, enabling users to rename individual datasets. A disconnect button (5) is located in the top right corner of the interface to safely terminate communication with the OECT controller.

During each initiated measurement, the drain-source voltage is applied at the start and removed once all cycles are completed. The gate voltage is consistently applied 10 seconds after the start of each measurement cycle and removed at the end of each cycle. The application allows multiple OECT devices to be measured sequentially, with each new measurement added to the same plot for direct comparison between datasets. If a measurement is invalid or affected by error, the corresponding cycle can be selectively removed.

Table 4.2 presents an example of the measured data exported to a .csv file, demonstrating the data structure produced by the application. Each dataset (cycle) occupies three columns, where the first row of each cycle is for the cycle name, followed by columns representing the time points of the measurements and the corresponding I_{ds} and I_{gs} values.

Table 4.2: *Example exported data from application to Excel*

	Cycle 1			Cycle 2	
Time (s)	Ids (mA)	Igs (mA)	Time (s)	Ids (mA)	Igs (mA)
0	1.0729	-0.9031	0	0.8616	-1.5002
0.02	1.0688	-0.904	0.03	1.4339	-1.6463
0.05	1.0627	-0.8808	0.05	1.3888	-1.6083
0.07	1.0421	-0.8898	0.07	1.3786	-1.5811
0.09	1.0524	-0.8871	0.1	1.3642	-1.5634

As a user interface, this application fulfills its intended purpose and significantly simplifies the measurement process. However, no considerations were made for connection loss handling or application testing, indicating that there is considerable room for improvement. Despite these limitations, the application functions effectively, enabling users to easily collect data and adjust parameters to control an OECT.

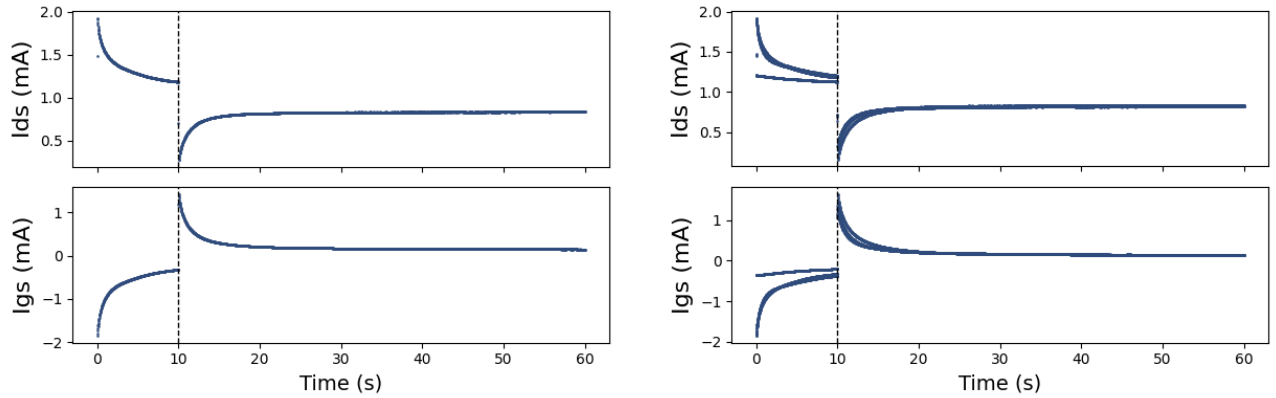
4.9 Textile OECT measurement with OECT controller

With the previously described PCBite setup and custom Windows application, textile OECT measurements can be performed effectively. As discussed earlier, the application and the OECT controller are designed to work together to measure current over time. According to the B-M model introduced in Section 2.3, two types of OECT behavior can be observed, one of which is the transient behavior [26].

This transient behavior is characterized by a stable I_{ds} when only a V_{ds} is applied. When a positive V_{gs} is introduced, the current typically shows either a monotonic decay or a spike followed by a recovery phase. Removing the gate voltage produces a corresponding inverse

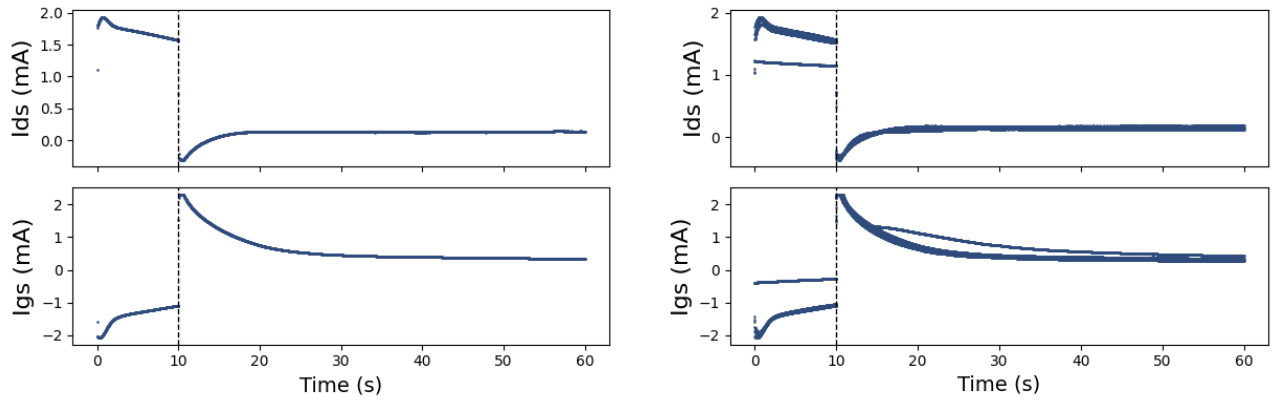
response. Additionally, the I_{gs} generally mirrors the shape of the I_{ds} response but is typically 10 to 50 times smaller in magnitude [27].

Figure 4.13(b) shows the transient response of the textile-based OECT, measured using the OECT controller and custom Windows application, over four consecutive measurement cycles under a drain voltage of 0.5 V and a gate voltage of 0.45 V. In each cycle, the gate voltage is applied at $t = 10$ s, resulting in a spike in I_{ds}, followed by a recovery phase during which I_{ds} stabilizes at a value lower than its initial level. The gate voltage is removed at $t = 60$ s, before the next cycle begins. This reveals a spike followed with a gradual decay in I_{ds} at the onset of each new cycle, along with a progressive increase in I_{gs}. Notice the first cycle shown in Figure 4.13(b), which is the more straight I_{ds} and I_{gs} during the initial phase (0–10 s) compared to the other cycles.



(a) (b)

Figure 4.13: *(a) Transient response of the OECT with a gate voltage of 0.45 V and drain voltage of 0.5 V during a single measurement cycle. (b) Transient response across four measurement cycles under the same conditions.*



(a) (b)

Figure 4.14: *(a) Transient response of the OECT with a gate voltage of 0.90 V and drain voltage of 0.5 V during a single measurement cycle. (b) Transient response across four measurement cycles under the same conditions.*

Figure 4.13(a) highlights the second cycle from the four shown in Figure 4.13(b). The spike and recovery behavior observed in the drain to source current (I_{ds}) has been well documented in the literature [26], [27], [62], where the initial spike corresponds to the rapid vertical injection of

ions into the PEDOT:PSS channel. This is followed by a slower lateral redistribution of the ions across the channel, resulting in the gradual recovery of the current.

Figure 4.14 presents results similar to those in Figure 4.13, but with a gate voltage of 0.9 V applied. A larger spike is observed at $t = 10\,\text{s}$ in both the I_{ds} and I_{gs} measurements when the gate voltage is applied. In the I_{gs} graph, the positive limit of the current range is reached, while at the beginning of the next cycle, the lower bound of the I_{gs} range is reached. Comparing Figure 4.14(a) and Figure 4.13(a) indicates that the saturation of I_{gs} influences the behavior of I_{ds}.

In both cases, with different gate voltages applied, a decrease in current is observed following the application of the gate voltage, eventually reaching a steady state. Comparing the steady-state currents in Figure 4.13 and Figure 4.14 shows that a higher gate voltage results in a lower steady-state current. Furthermore, the application and removal of the 0.9 V gate voltage produces a higher current spike compared to the 0.45 V gate voltage.

While Figure 4.13(b) and Figure 4.14(b) show slight variations between cycles, this effect is likely due to the gate voltage being applied too soon in each subsequent cycle. As a result, the recovery phase following the removal of the gate voltage may not be fully completed before the next gate voltage is applied, leading to minor inconsistencies in the transient response.

A likely cause for the influence of I_{gs} saturation on the measured I_{ds} can be explained from the behavior of the transimpedance amplifier, as explained in Section 3.2.2. This amplifier regulates its output to maintain the inverting input at a fixed bias voltage (V_{gs}) through negative feedback. However, when the input current becomes too large, the required output voltage may exceed the op-amp's range, forcing the amplifier into saturation. In this state, the feedback loop breaks down, and the inverting input can no longer be held at the intended bias level which means that the actual applied gate voltage differs from its target value (biased voltage).

During the recovery phase of the OECT, as I_{gs} gradually decreases, the output remains pinned at its limit until the current falls low enough to bring the output voltage back within the op-amp's linear range. Only then is feedback re-established, allowing the inverting input to iteratively return to its intended bias (V_{gs}), and accurate current-to-voltage conversion resumes. As a result, the measured I_{ds} is also affected, where the initial spike becomes distorted, and the gate-induced response progresses through small steps until the full gate bias is restored. Only after this bias is re-established does the typical recovery behavior begin.

This issue can be addressed by replacing the feedback resistor of the transimpedance amplifier in the I_{gs} circuit with a resistor of less than $1000\,\Omega$, thereby increasing the measurable current range at the expense of resolution.

Comparing these results with the B-M model discussed in Section 2.3 suggests that the behavior of the textile-based OECT measured with the OECT controller aligns with a spike-and-recovery model. However, while Gentile et al. [27] report that I_{gs} is typically 10–50 times lower than I_{ds}, this raises questions about the underlying behavior within the sensor or the OECT controller itself. Tests with the J201 transistor indicated no apparent interaction between the I_{ds} and I_{gs} circuits.

The observed amount of I_{gs} with the OECT controller could come from incomplete isolation between the gate and the channel in the textile-based OECT, where the non-woven channel

material might penetrate the electrolyte layer and come into contact with the gate electrode. This observation does support the importance of measuring the gate-source current, as it provides insights into the construction and layering of the OECT itself.

The results obtained from measuring a textile-based OECT using the developed OECT controller and its corresponding Windows application demonstrate that the system is capable of capturing the transient response of the device. These findings confirm that the controller meets its design objectives and is suitable for characterizing OECT behavior in practical applications.

Chapter 5

Conclusion and Future Outlook

Conclusion

This thesis aimed to develop a measurement system capable of accurately characterizing the electrical properties of textile-based organic electrochemical transistors (OECTs), with a focus on reliability and user-friendliness. To achieve this, a compact custom-built measuring unit was designed, integrating a microcontroller-based hardware platform with a custom Windows application for data acquisition and parameter adjustment. The system includes essential analog components such as an analog-to-digital converter (ADC), digital-to-analog converter (DAC), differential amplifier, transimpedance amplifier, and summing amplifier, all integrated on a 6 cm × 4 cm printed circuit board. The entire unit was assembled at a cost of approximately 60 €/unit and communicates wirelessly with the host application via Bluetooth Low Energy.

The system successfully applied drain-source and gate-source voltages in the range of −1 V to 1 V, with an error of 0.2 mV. Current measurements for I_{ds} and I_{gs} were achieved over a range of ±20 mA and ±2 mA, with an accuracy exceeding 99% in Ohm's law validation tests. A maximum absolute error of 8 μA was observed during transistor tests for I_{ds}, when compared to a high-quality measurement setup at HSNR. Validation against a source measuring unit confirmed that the system's sensing side achieved an accuracy exceeding 90%. These results demonstrate that the developed measurement system meets the primary objectives of this thesis, showcasing both accuracy and reliability in effectively measuring the electrical behavior of textile-based OECTs.

This work addressed key research sub-questions. The electrical behavior of the textile-based OECTs were successfully captured by the system, showing behavior consistent with the B-M model and providing real-time I_{ds} and I_{gs} data. The use of gold-plated probes as electrode materials was found to be effective and compatible with the textile-based OECTs. In terms of hardware and software integration, the combination of microcontroller-based circuitry, precise analog components, and a custom software interface enabled accurate control and measurement of the system. Finally, the system performed well when compared to high-quality source measuring units, staying within the target maximum deviation of 10%.

Several limitations were identified during the development and evaluation of the device. One key issue was the calibration of the current sensing system, which relied on a basic offset correction approach and resulted in residual errors. A more accurate method would involve repeating the current sensing validation by sourcing known current values through the device and recording the corresponding raw digital outputs from the ADC. These values could then be used to create

a calibration dataset and implement a lookup table, similar to the approach used for DAC calibration. A simplified variation of this method would be to repeat the Ohm's law validation process using the same principle. In this case, the OECT controller applies a known voltage across a resistor with a known resistance value. Instead of calculating the current, the raw ADC output is recorded at each voltage step. These raw values can then be mapped to the expected current values, coming from Ohm's law, to form a lookup table linking ADC output to current.

Measurement precision was further affected by noise and the use of a lower feedback resistor in the transimpedance amplifier for I_{ds}, which reduced performance in low-current measurements. These issues could be addressed through improved analog filtering in the circuitry surrounding the transimpedance amplifier. The Open-source potentiostat design from UWED offers a useful strategy for analog filtering around the DAC and differential amplifier stages, improving voltage stability and resolution [32].

Component selection also contributed to variation in performance. Different operational amplifiers were used in the I_{ds} and I_{gs} measurement paths, which led to differences in offset and accuracy between the channels. Using the same high-precision amplifier for all amplifier stages would eliminate this lack of similarity. Signal stability could be further improved by refining the voltage reference sources. Currently, the reference voltages for the ADC and DAC are derived from the shared supply voltage line. Employing dedicated high-precision voltage reference ICs for these components would enhance stability on both the voltage application and measurement sides. Finally, communication between the device and the Windows application could benefit from improvements in both transmission speed and data size handling.

In conclusion, this thesis presents the design, development, and validation strategies for a custom measurement system engineered for textile-based OECTs. The microcontroller-based system integrates both hardware and software components to provide a reliable, accurate, and user-friendly platform for OECT characterization, offering valuable insights into OECT behavior. The resulting device, *HSNR OECT CONTROLLER*, even with its limitations, is capable of characterizing textile-based OECTs enabling material scientists at Hochschule Niederrhein in Mönchengladbach, Germany, to study OECT functionality, stability, reproducibility, and overall performance with ease.

Future outlook

Despite the progress made, and after addressing the previously mentioned limitations, there are several directions in which the system could be further developed and improved.

Further optimization could begin with improving the validation and calibration methods. Establishing stable and reliable calibration procedures would streamline future validation efforts and promote more consistent device performance.

The device presented in this thesis functions as a unit which is capable of controlling the voltages and read the currents of OECTs, and its design already includes the potential for battery integration, allowing for greater portability. A future version could also involve embedding the system in a 3D-printed test kit equipped with a LiPo battery and integrated measurement pins, while keeping the OECT exposed to allow analyte application. This concept would enable the creation of a compact, pocket-sized portable test kit for OECTs.

Another possible improvement involves expanding the system's measurement capabilities to support multiple OECTs simultaneously through multiplexing.

In addition to hardware improvements, the custom Windows application could be further developed to offer more advanced characterization functions. For example, it could include automated acquisition of transfer characteristics, based on the B-M model discussed in Section 2.3. Additional features such as real-time voltage control with live signal monitoring, hysteresis measurements, and multi-device communication could also be integrated.

Ultimately, with the simplicity of CircuitPython, which does not require an integrated development environment and allows the microcontroller to be programmed as easily as editing a text file, the Windows application software could evolve into a more interactive user experience. In this envisioned setup, the user would communicate either through text or speech with the application, which would then dynamically adjust the microcontroller code to perform specific measurements based on user input. Although still an ambitious idea, this approach could one day result in a flexible and intelligent OECT characterization platform that adapts in real time to the needs of the experimentalist.

As the textile based OECT continues to evolve and achieves higher reproducibility, the measurement system can be redesigned to reflect these advancements, enabling iterative refinement of all aspects of the setup. Once the OECT reaches a more finalized design stage, where optimal operating voltages are well understood, the measurement device itself could be further miniaturized. In this scenario, the final version of the OECT controller could consist of a single printed circuit board with an integrated microcontroller unit, eliminating the need for external control components. This compact design could enable broader functionalities, including integration into wearable devices.

Overall, the measurement platform developed in this work provides valuable support for the ongoing development of textile-based OECTs by enabling easier characterization of their electrical properties. Looking ahead, such platforms are essential for bridging the gap between emerging organic electronics and real-world applications, ultimately contributing to the advancement of flexible, wearable, and bio-integrated technologies.

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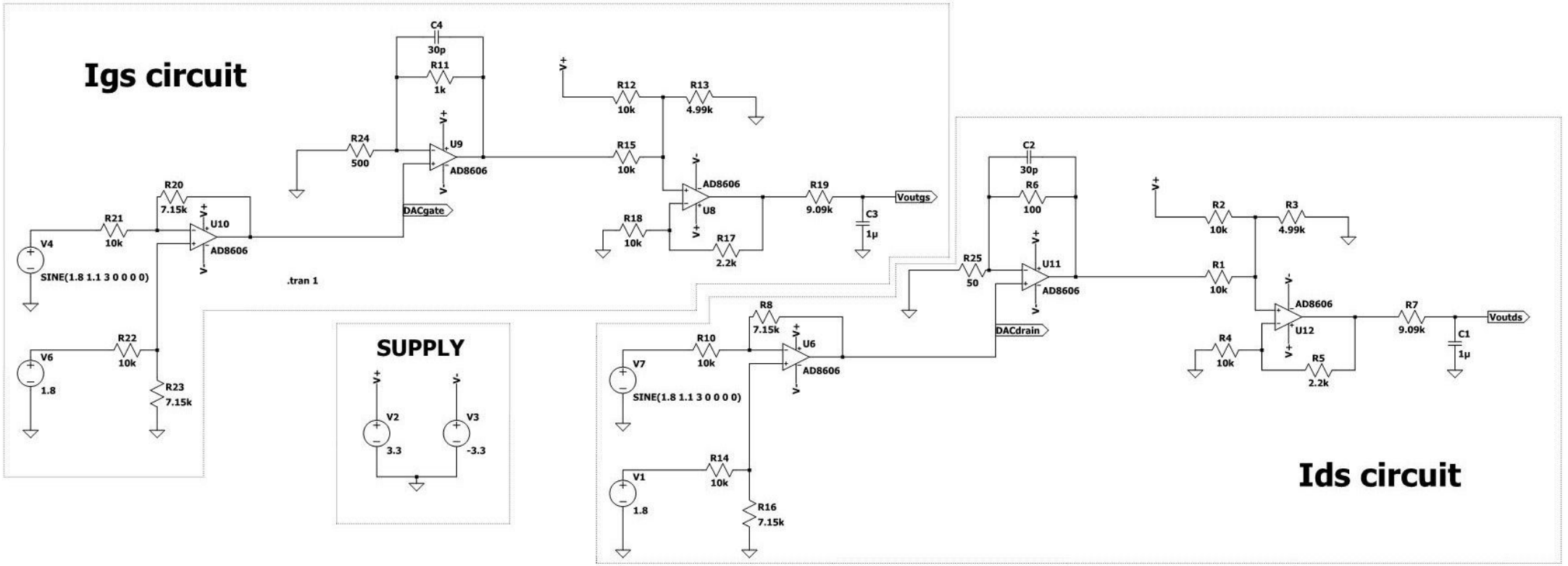
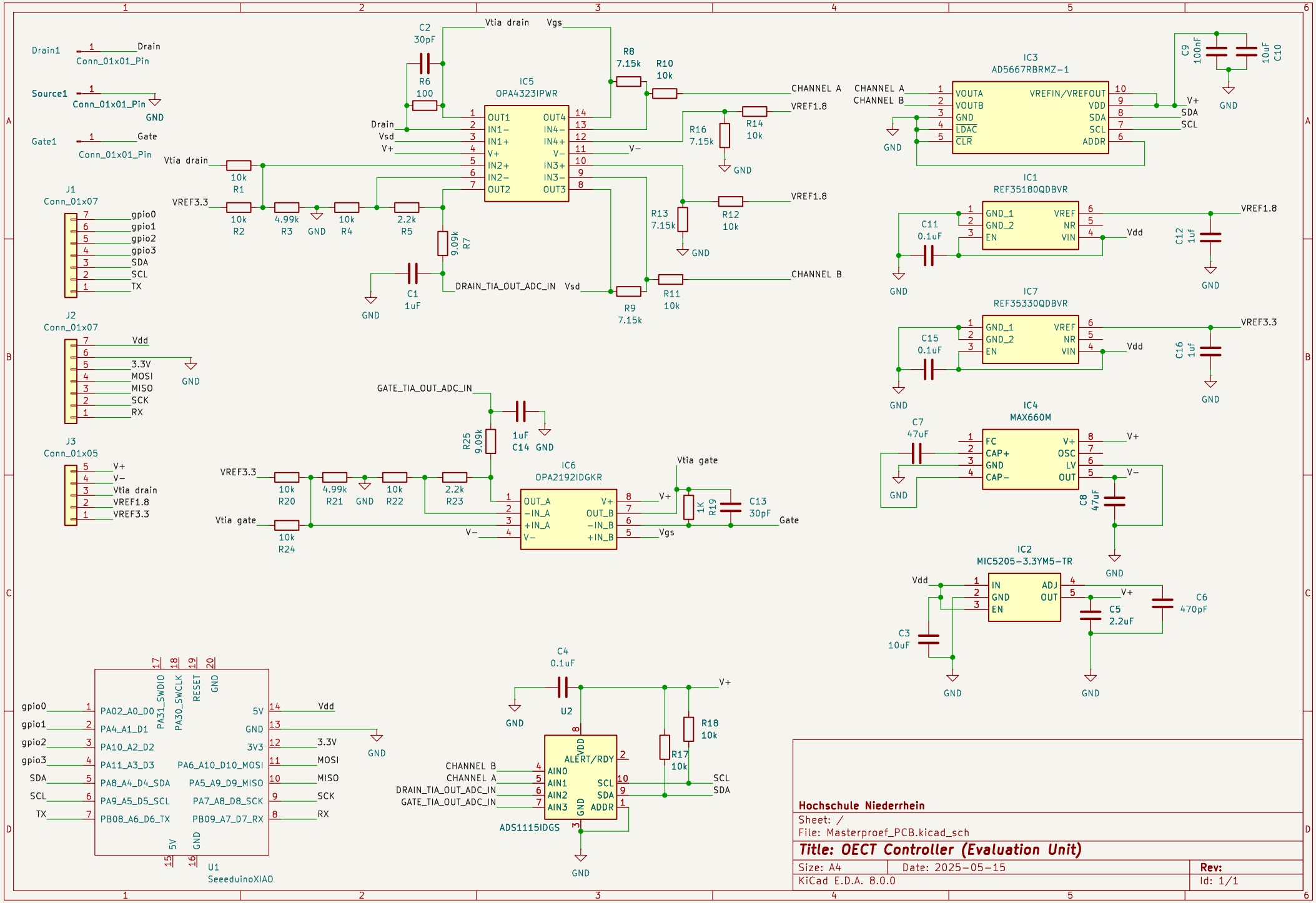
Appendix A

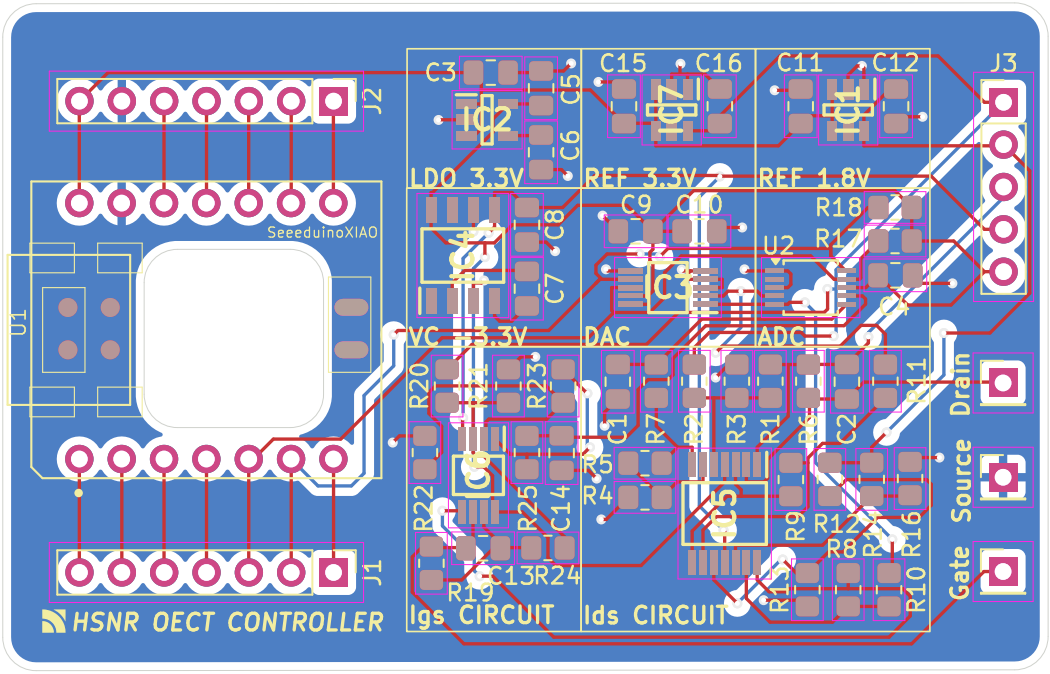
Attachment - LTSpice schematic

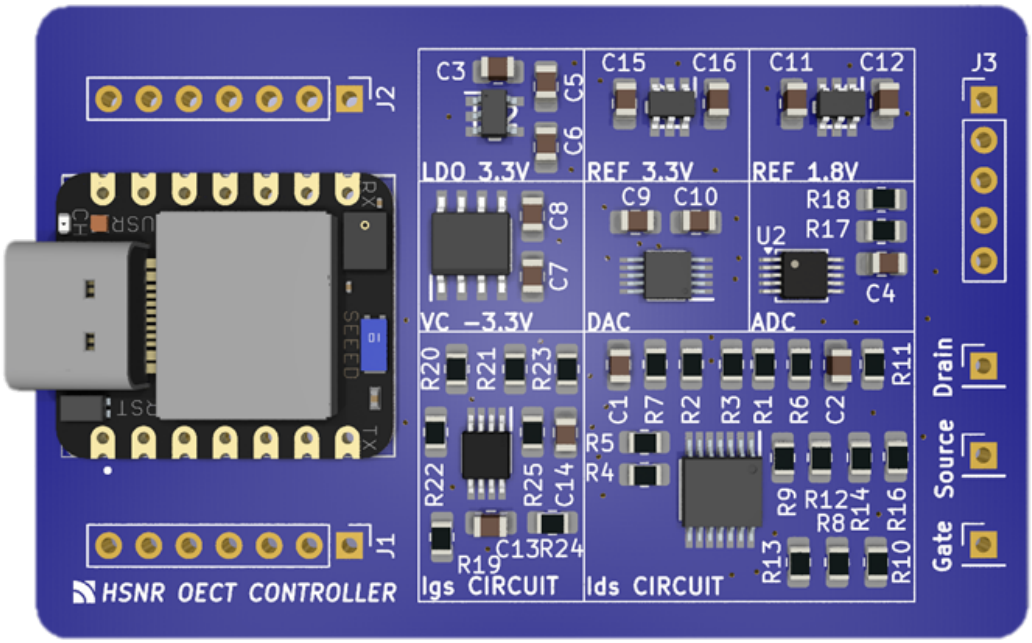

Igs circuit
C4
30p
R11
1k
R24
500
U9
AD8606
R12
10k
R13
4.99k
R15
10k
AD8606
U8
R19
9.09k
Voutgs
C3
1µ
R18
10k
R17
2.2k
DACgate
R20
7.15k
R21
10k
U10
AD8606
V4
SINE(1.8 1.1 3 0 0 0 0)
R22
10k
V6
1.8
R23
7.15k
.tran 1
SUPPLY
V2
3.3
V3
-3.3
C2
30p
R6
100
R25
50
U11
AD8606
DACdrain
R8
7.15k
R10
10k
U6
AD8606
V7
SINE(1.8 1.1 3 0 0 0 0)
R14
10k
V1
1.8
R16
7.15k
R2
10k
R3
4.99k
R1
10k
AD8606
U12
R7
9.09k
Voutds
C1
1µ
R4
10k
R5
2.2k
Ids circuit

Appendix B

Attachment - PCB Design KiCad


Drain1
Drain
Conn_01x01_Pin
Source1
GND
Gate1
Gate
J1
Conn_01x07
gpio0
gpio1
gpio2
gpio3
SDA
SCL
TX
J2
Vdd
3.3V
MOSI
MISO
SCK
RX
J3
Conn_01x05
V+
V−
Vtia drain
VREF1.8
VREF3.3
C2
30pF
R6
100
Vtia drain
Vgs
IC5
OPA4323IPWR
OUT1
IN1−
IN1+
V+
IN2+
IN2−
OUT2
OUT4
IN4−
IN4+
V−
IN3+
IN3−
OUT3
R8
7.15k
R10
10k
CHANNEL A
VREF1.8
R16
7.15k
R14
10k
R1
10k
R2
10k
R3
4.99k
R4
10k
R5
2.2k
R7
9.09k
C1
1uF
DRAIN_TIA_OUT_ADC_IN
R13
7.15k
R12
10k
R9
7.15k
R11
10k
CHANNEL B
IC3
AD5667RBRMZ−1
VOUTA
VOUTB
LDAC
CLR
VREFIN/VREFOUT
VDD
SDA
SCL
ADDR
C9
100nF
C10
10uF
IC1
REF35180QDBVR
GND_1
GND_2
EN
VREF
NR
VIN
C11
0.1uF
C12
1uf
Vdd
IC7
REF35330QDBVR
C15
0.1uF
C16
1uf
GATE_TIA_OUT_ADC_IN
R25
9.09k
1uF
C14
R20
10k
R21
4.99k
R22
10k
R23
2.2k
IC6
OPA2192IDGKR
OUT_A
−IN_A
+IN_A
V−
V+
OUT_B
−IN_B
+IN_B
Vgs
Vtia gate
R19
1K
C13
30pF
Gate
R24
10k
IC4
MAX660M
FC
CAP+
CAP−
OSC
LV
OUT
C7
47uF
C8
47uF
IC2
MIC5205−3.3YM5−TR
IN
ADJ
C3
10uF
C5
2.2uF
C6
470pF
U1
SeeeduinoXIAO
PA02_A0_D0
PA4_A1_D1
PA10_A2_D2
PA11_A3_D3
PA8_A4_D4_SDA
PA9_A5_D5_SCL
PB08_A6_D6_TX
PA31_SWDIO
PA30_SWCLK
RESET
5V
3V3
PA6_A10_D10_MOSI
PA5_A9_D9_MISO
PA7_A8_D8_SCK
PB09_A7_D7_RX
C4
0.1uF
U2
ALERT/RDY
AIN0
AIN1
AIN2
AIN3
R18
10k
R17
10k
ADS1115IDGS
Hochschule Niederrhein
Sheet: /
File: Masterproef_PCB.kicad_sch
Title: OECT Controller (Evaluation Unit)
Size: A4
Date: 2025−05−15
Rev:
KiCad E.D.A. 8.0.0
Id: 1/1


SeeeduinoXIAO
HSNR OECT CONTROLLER
LDO 3.3V
REF 3.3V
REF 1.8V
VC −3.3V
DAC
ADC
Igs CIRCUIT
Ids CIRCUIT
Gate
Source
Drain


HSNR OECT CONTROLLER
LDO 3.3V
REF 3.3V
REF 1.8V
VC −3.3V
DAC
ADC
Igs CIRCUIT
Ids CIRCUIT
Gate
Source
Drain