Faculteit Industriële Ingenieurswetenschappen

master in de industriële wetenschappen: elektronica-ICT

Masterthesis

Designing an amplifier for biomedical signals in IGZO

Mauro Vranckx

Scriptie ingediend tot het behalen van de graad van master in de industriële wetenschappen: elektronica-ICT

PROMOTOR :
Prof. dr. ing. Kris MYNY

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UHASSELT KU LEUVEN

Preface

I would like to begin this master's thesis by expressing my heartfelt appreciation to my supervisors, prof. dr. ing. Kris Myny, ing. Yari Nowicki and ir. Muhammed Dawood Asghar, whose unwavering support and guidance helped me through this journey and encouraged me to push further to reach the conclusion presented in this thesis. Thank you for al your feedback, and most importantly, your time.

Second, I would like to thank my girlfriend, who helped me understand various biological topics and supported me with patience and unwavering encouragement. I am also grateful to my parents and brother, who, despite not having much insight into the subject, were always eager to hear about the latest developments and remained supportive throughout the process. Lastly, I want to thank the students who worked alongside me during this time. Their dedication and sense of healthy competition pushed me to achieve more.

Thank you all.

With this thesis, a new chapter in life begins. I hope this thesis will encourage and inspire you, and others, to delve deeper into the field of analogue circuits for flexible electronics, as it holds broad and meaningful potential for real-world applications in everyday life.

Contents

List of Tables

List of Figures

Acronym List

OPAMP	Operational Amplifier
ECG	Electrocardiogram
CMRR	Common-Mode Rejection Ratio
PM	Phase Margin
AFE	Analogue Front-End
CMOS	Complementary Metal-Oxide-Semiconductor
TFT	Thin-Film Transistors
LTPS	Low-Temperature Polycrystalline Silicon
a-Si	Amorphous Silicone
a-IGZO	Amorphous Indium-Gallium-Zinc-Oxide
CS	Common-Source
CG	Common-Gate
CM	Common-Mode
UGBW	Unity Gain Bandwidth
SDA	Simple Differential Amplifier
DCDA	Diode Connected Differential Amplifier
BDA	Bootstrapped Differential Amplifier
TBDA	Transconductance Boosting Differential Amplifier
ADC	Analogue to Digital Converter

Abstract

The field of flexible electronics is gaining increasing interest due to its wide applicability in society, including the recording of electrocardiograms (ECG) using a flexible patch. The amplification of the heart signal is essential to enable an accurate ECG recording. The focus of this master's thesis is on the design of an operational amplifier (OPAMP) that can be integrated on a flexible chip made from indium gallium zinc oxide (IGZO), with the aim of improving the accuracy and quality of the ECG signal processing.

The OPAMP was designed using a 600nm IGZO TFT process technology node of the PragmetIC Semiconductor foundry. The designed OPAMP utilizes chopping to suppress noise. Furthermore, an ECG signal obtained from a medical study is applied to the OPAMP, to evaluate its performance in real-time signal amplification.

The OPAMP operates with a supply voltage of 3 V and achieves a gain of 54.34 dB. The common-mode rejection ratio (CMRR) is 57.15 dB, with a total system bandwidth of 425.25 kHz. The phase margin is measured at 60°, indicating a stable system, with a total power consumption of 106.3 µW. The results show that the OPAMP is suitable for use in a flexible patch. Moreover, the noise-suppressing techniques enhance signal quality and accuracy with a small compromise in the gain. The obtained signal contains a small ripple, which can be addressed in future research.

Abstract in Dutch

Flexibele elektronica kent toenemende belangstelling vanwege de brede toepasbaarheid in de samenleving, waaronder het registeren van elektrocardiogrammen (ECG) met behulp van een flexible pleister. Voor het opnemen van een ECG is het versterken van het hartsignaal essentieel. Deze masterproef richt zich op het ontwerpen van een operationele versterker (OPAMP) geïntegreerd op flexibele chip gemaakt van indium-gallium-zinkoxide (IGZO), met het doel de kwaliteit en accuraatheid van de ECG-signaalverwerking te verbeteren.

Voor het ontwerpen van de OPAMP wordt de 600nm IGZO TFT technologie van PragmatIC Semiconductors gebruikt. De ontworpen OPAMP maakt gebruik van chopping om ruis te onderdrukken. Daarnaast wordt er een ECG-signaal van een medische studie aangelegd op de OPAMP, om de prestatie ervan te evalueren op het gebied van realtime signaalversterking.

De ontworpen OPAMP functioneert bij een voedingspanning van 3 V en behaalt een versterking van 54,34 dB. De common-mode rejection ratio (CMRR) bedraagt 57,15 dB, waarbij de totale bandbreedte van het systeem 425,25 kHz bedraagt. Het systeem verbruikt 106.3 µW, met een fasemarge van 60°. De bekomen resultaten tonen aan dat de OPAMP geschikt is voor een toepassing in een flexibele pleister. Bovendien dragen de ruisonderdrukkende technieken bij aan een verbeterde signaalkwaliteit en accuraatheid, ten koste van een minimale afnamen in versterking. Het bekomen signaal bevat een kleine rimpel, waarvoor toekomstig onderzoek kan uitwijzen hoe deze het beste weggewerkt kan worden.

Chapter 1

Introduction

1.1 Motivation

Technological advancements have significantly impacted human health care [1], with the two fields becoming increasingly intertwined, as evidenced by recent developments involving artificial intelligence (AI) and wearable devices. These wearable devices can be developed with thin-film transistors (TFTs), which can conform to the shape of the patient's body. Such systems enable diagnosis from virtually anywhere [2],[3]. These rely on continuous collection of critical physiological data such as heart rate, blood pressure, body temperature, among other parameters.

Such information can be obtained by using Analogue Front-End (AFE) circuits, which convert the analogue data to digital formats that can be processed and interpreted by an AI model or medical expert. These circuits need low-noise, high-gain amplifiers to enhance the resolution and peak voltage, thereby ensuring accurate and reliable data acquisition. To achieve the low-noise aspect, an Operational Amplifier (OPAMP) is commonly used. These components are designed to amplify the difference between two input signals, which facilitates suppression of common-mode noise present on both inputs, thereby improving signal quality.

Accurate signal processing at hardware level is not only necessary for a correct diagnosis but also for enabling the early detection of various medical conditions [4],[5].

1.1.1 Emerging Technologies, Systems and Security

The Emerging Technologies, Systems and Security (ES&S) [6] research group at KU Leuven researches secure and efficient hardware implementations for both flexible and silicon-based electronics. One of their ongoing studies focuses on the integration of AI into flexible chips, a promising approach for applications in clinical trials, as previously discussed. In this context, there is a need to analyse an electrocardiogram (ECG), a time-dependent representation of the heart's electrical activity [7], that can be achieved through the implementation of an AFE.

The research group works with PragmatIC to create the flexible wafers in Amorphous Indium Gallium Zinc Oxide (a-IGZO) technology, as demonstrated in the GRASP project [8]. Overall, a-IGZO transistors are preferred because of their lower leakage current and lower production cost compared to other thin-film transistors [9].

1.2 Problem Statement

1.2.1 Electrocardiogram Signals

The heart contracts due to the polarization of the heart muscle fibre membranes [10], which can be detected on the skin's surface by placing 12 leads in different locations. A less accurate, yet more practical approach is the single-lead implementation, which is particularly advantageous for integration on flexible substrate. Figure 1.1 shows a visual representation of such a signal.

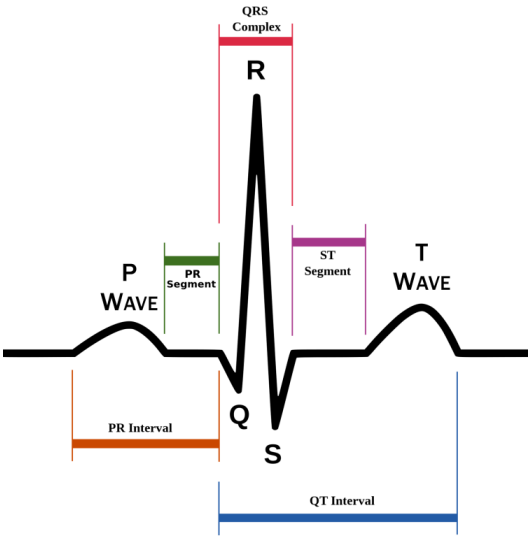


Figure 1.1: Visual Representation of an ECG Signal [11, p. 181]

This signal consists of multiple intervals with varying amplitudes, each corresponding to the depolarization of different parts of the heart muscle. The lowest amplitude ranges between 1.0 and 1.4 mV for healthy males and 0.7 to 1.0 mV for healthy females [12]. Additionally, these signals have a low driving capability, meaning they are unable to effectively drive circuits with a low input impedance.

1.2.2 Noise Sources

It has been established that active components and resistors are primary noise sources within an electronic system. The two predominant categories are white and 1/f noise. White noise is characterized by its presence across all frequencies, while 1/f noise is limited to a certain corner frequency. Figure 1.2 displays the 1/f and white noise elements in relation to the frequency.

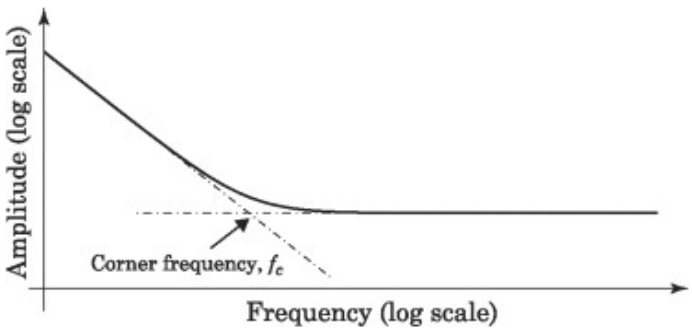


Figure 1.2: White and 1/f Noise in Function of Frequency [13, p. 123]

White or thermal noise is attributed to the pseudo-random movement of free carriers within the material [14], and is solely dependent on the material's temperature. Additionally, these carriers move to eliminate the electrical fluctuation created by the black body radiation. The power created due to white noise is modelled by Equation 1.1 [15].

$$P_{noise} = 4kTB \tag{1.1}$$

Equation 1.1 shows that white noise can be calculated using the temperature of the material T, the Boltzmann constant, and the bandwidth of the system B.

The most prevalent noise at lower frequencies is the 1/f noise, which is believed to be created from trapping and releasing free carriers within the material's oxide traps [16]. These can be created by defects in the a-IGZO atomic structure, with oxygen vacancies being a known example [17]. The trapped free carriers can not participate in current transport and therefore cause noise.

The time constant, denoted by τ, of each trap determines the duration of charge trapping (τ_+) and releasing (τ_-). The magnitude of the time constants characterizes the classification of traps as either slow or fast [18]. If the period of the signal is shorter than the time required for the trap to capture a charge carrier, then the capture process will be inhibited [19]. This shows that, at higher frequencies, a reduced number of traps become available to trap charge carriers.

1.2.3 Material Constraints

The ECG signal comprises a range of frequencies from 0 to 100 Hz [12], placing it within the 1/f noise spectrum of a-IGZO transistors. The noise created by a-IGZO transistors exhibits a maximum power spectral density of $10^{-18}A^2/Hz$ [20], which is lower than other TFT technologies [21]. This indicates that the OPAMP itself will introduce noise into the amplified signal, which reduces the resolution. If not properly accounted for, noise may be misinterpreted by the AI model or medical professionals as an early indicator of a medical condition in clinical applications.

a-IGZO technology has a low hole mobility due to the intrinsic characteristics of the material [22], which prevents the practical use of PMOS transistors, and by extension, the implementation of complementary metal-oxide-semiconductor (CMOS) circuits. As a result, the OPAMP must be constructed exclusively with NMOS transistors, limiting the achievable gain.

Since the OPAMP is intended for use on a flexible patch, its power consumption must also be strictly limited. This is necessary to enable remote usage of the patch and to ensure the patients safety.

1.3 Objectives

The primary objective of this masters thesis is to design and implement the amplification stage of an AFE, with the goal of achieving high amplification and low noise, whilst preserving the critical information and signal structure. This goal can be divided into several sub-objectives.

The first objective involves the use of an OPAMP to improve the Common-Mode Rejection Ratio (CMRR). This is achieved by a differential pair, which needs to be carefully optimized to provide additional amplification while maximizing the CMRR. The initial amplification stage plays a

critical role in determining the overall noise performance, as it predominantly governs the extent to which noise is amplified throughout the system.

The second objective is to ensure that the output of the differential pair is amplified without compromising the stability of the system. This enables the provision of feedback to the system, while preventing oscillation from occurring.

The third objective ensures that noise created by the system itself is removed or lowered. This creates a clean output signal suitable for accurate digital conversion. Finally, a high input impedance is essential in the amplifier to prevent loading the ECG signal source. This creates an accurate voltage measurement without signal attenuation.

1.4 Method

1.4.1 Differential Stage

The OPAMP was designed using the PragmatIC 600 nm technology for a-IGZO within the Virtuoso Cadence simulation environment. This tool facilitates both schematic circuit design and physical layout implementation. Additionally, the simulator includes a built-in local optimization feature, which enables automated adjustment of transistor sizing to meet specified target values for predetermined performance parameters. The differential stage was optimized for a high CMRR while maintaining an appropriate level of voltage amplification.

1.4.2 Amplification Stage

To improve the gain further, a cascaded amplifier will be added at the output. The stability of a system is characterized by the Phase Margin (PM). Which is defined as the difference between measured phase angle and 180° when the amplification is 0 dB [23]. To ensure that the system does not oscillate whilst having a usable settling time, the PM should be between 45° and 70° [24].

1.4.3 Chopping

To mitigate noise introduction by the system itself, a technique known as chopping is implemented. This method involves translating the input signal to a frequency above the 1/f noise corner, thereby significantly reducing the low-frequency noise component [25]. This frequency translation is achieved through the use of mixers, which may be implemented in either active or passive configuration [26]. To lower power consumption and reduce system complexity, the passive mixer configuration is selected for this work. These mixers perform modulation of the input signal around a specified frequency, which is set to 1 or 5 kHz in the context of this master's thesis. After modulating, the signal is amplified and subsequently demodulated, with the gain preserved throughout the process.

1.5 Thesis Outline

This masters thesis is divided into 5 different chapters, with each addressing a specific aspect of the research:

- **Second chapter:** examines the advantages of a-IGZO over alternative TFT technologies. Furthermore, it investigates various OPAMP design approaches relevant to the context of IGZO-based circuits and low noise applications.
- **Third chapter:** discusses several amplifier architectures which are designed and explained in detail.
- **Fourth chapter:** discuses the different test benches used to evaluate the differential amplifiers. The results from these test benches are observed and discussed. Whereafter, the amplifiers with promising results will be tested on a chopped ECG signal.
- **Fifth chapter:** gives a short recap on what has been established and gives recommendations for future work.

Chapter 2

Literature Study

2.1 Introduction

The integration of analogue signals into digital systems is a well established concept that has been extensively studied in the literature. This is particularly true for Analogue Front-End (AFE) circuits designed for ECG signal acquisition, where implementations using materials such as a-IGZO and many others have also been explored. This chapter reviews previously implemented AFE designs and used materials to serve as a foundation for the AFE developed in this master's thesis.

2.2 Thin-Film Transistor Technologies

2.2.1 Low-Temperature Polycrystalline Silicon

Low-Temperature Polycrystalline Silicon (LTPS) is a type of polycrystalline silicone created at comparatively lower temperatures. Unlike crystalline silicon (c-Si), LTPS consists of multiple silicon grains separated by grain boundaries, which act as a potential barrier inhibits charge carrier movements and can significantly influence electrical properties [27]. Although LTPS exhibits lower conductivity compared to c-Si, it still outperforms other TFT technologies. This is reflected in an electron mobility which ranges from 50 to 100 $\frac{cm^2}{V^2s^2}$ [9]. One key advantage of LTPS is its ability to support both NMOS and PMOS transistors. However, the fabrication process of LTPS is more complex than that of a-IGZO, resulting in higher production costs [9].

2.2.2 Amorphous Silicone

Amorphous Silicone (a-Si) differs from its crystalline counterpart primarily in its atomic structure. Unlike crystalline silicon, which exhibits a well-ordered lattice, a-Si consists of a continuous random network. This non-crystalline configuration enables the material to maintain a solid state with mechanical stability, despite the absence of long-range atomic order [28]. However, this structural disorder significantly reduces electron mobility compared to crystalline silicon. For a-Si, typical electron mobility ranges from 0.5 to 1 $\frac{cm^2}{V^2s^2}$ [9]. Similar to a-IGZO, a drawback of this technology is the inability to effectively fabricate PMOS transistors. In comparison to a-IGZO and LTPS, a-Si has a relatively low production cost, which remains one of its primary

advantages.

2.2.3 Amorphous Indium Gallium Zinc Oxide

a-IGZO exhibits an electron mobility in the range of 10 to 40 $\frac{cm^2}{V^2s^2}$, and is comparatively more cost-effective to manufacture than LTPS [9]. Although its electron mobility is lower than that of LTPS, it significantly outperforms a-Si, making a-IGZO a promising material for the development of flexible integrated circuits. One notable drawback, as discussed before, is the absence of PMOS transistors.

2.3 Amplifiers

2.3.1 Single-Stage Amplifier

Before delving deeper in the workings of differential stages and a-IGZO-based implementations, it is essential to first understand the single-stage amplifier, as it forms the foundational building block of most amplifier architectures. Among these, the common-source (CS) amplifier is recognized as one of the three primary configurations [29]. The implementation of a CS amplifier is shown in Figure 2.1.

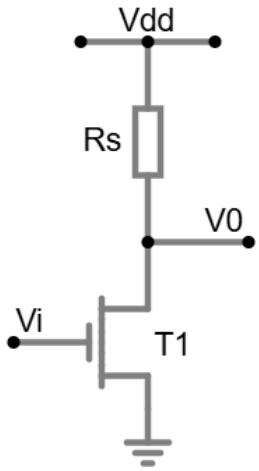


Figure 2.1: Common-Source Amplifier

To analyse the response of the output voltage V_0 to variations in the input V_i, a sweep is applied at the V_i node ranging from ground to V_{dd} [30]. When $V_i = 0$ V the transistor remains off, and V_0 is pulled op to V_{dd}. As V_i approaches the threshold voltage V_{th}, transistor T_1 begins conducting, leading to an increase in the drain current I_d. This rise in current results in a voltage drop across the resistor R_s, thereby reducing V_0. The current induced by changing the gate voltage V_g of a transistor operating in the saturation region is described by Equation 2.1 (if channel-length modulation is neglected), and the transconductance of the MOSFET by Equation 2.2

$$I_D = \frac{1}{2} C_{ox} \mu_n \frac{W}{L} (V_{GS} - V_{th})^2 \tag{2.1}$$

$$g_m = C_{ox} \mu_n \frac{W}{L} (V_{GS} - V_{th}) \tag{2.2}$$

The gain of a CS amplifier is given in Equation 2.3, and is derived from [30].

$$A_v = -g_m R_s \tag{2.3}$$

Equation 2.3 indicates that the voltage gain of a CS amplifier is dependent on the transconductance of the used MOSFET and the output resistance. The negative sign in the gain expression signifies a 180° phase shift between the input and output. Furthermore, considering Equation 2.2, it becomes evident that the gain is also a function of the gate-to-source voltage V_{GS}, thereby introducing a degree of nonlinearity into the amplification behaviour.

The design of a CS amplifier involves a series of trade-offs, as each design choice affects the overall performance. Based on Equations 2.3 and 2.2 a reduction in channel length and an increase in the width of a transistor would be preferred. However, enlarging the transistor dimensions, particularly the width, would increase the input capacitance and thus introduce a greater parasitic load [30]. This added capacitance can significantly degrade the frequency response by lowering the bandwidth and limiting overall gain, particularly at high frequencies. Increasing the resistance value of R_s effects the voltage gain A_v. However, if the voltage drop across R_s approaches $V_i - V_{th}$, transistor T_1 may be driven out of the saturation region, which limits the output swing.

Due to limited area and achievable transistor parameters on silicon or a-IGZO substrates, the use of a diode-connected load may present a viable alternative for certain circuit configurations. Figure 2.2 depicts the implementation of a diode-connected circuit, which is characterized by the use of a diode-connected transistor instead of a resistive load.

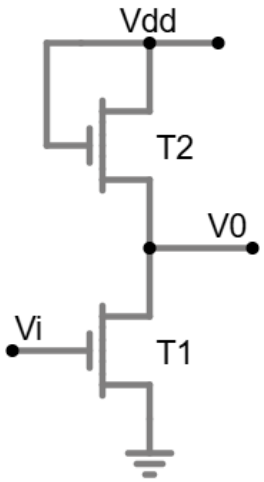


Figure 2.2: Diode-Connected Load

Transistor T_2 in Figure 2.2 will always operate in the saturation region be cause $V_{DS} = V_{GS}$. The gain of this circuit is obtained in [30, P. 54] and shown in Equation 2.4.

$$A_v = -g_{m1} \frac{1}{g_{m2} + g_{mb2}} \tag{2.4}$$

In this equation, g_{mb2} accounts for the body effect of transistor T_2, which is not present in a-IGZO. Furthermore, the term g_{m2} introduces non-linearity due to the variations in V_{GS}, as the source node is connected to V_0, which itself varies with the input signal. It is important to note that the diode connected transistor could, in principle, be implemented using a PMOS device. However as stated before a-IGZO limits the use of PMOS transistors.

2.3.2 Differential Amplifier

Simple single-ended amplifiers increases a signals voltage with respect to a fixed reference, whilst a differential signal is determined by the voltage between two nodes, neither of which is directly tied to ground or V_{dd} [30]. Such signals oscillate around a DC offset which is known as the common-mode voltage (CM). Signal integrity can be compromised by surrounding electromagnetic interference resulting from capacitive or inductive coupling. This issue is particularly pronounced in single-ended signals, where such interference is more challenging to mitigate. In differential signals, however, interference affects both lines similarly, thus preserving the voltage difference between them and enhancing robustness against noise [30]. Such implementations have a high common-mode rejection.

Differential amplifiers are constructed using two single-ended amplifiers and are designed to amplify the voltage difference between two signals. Figure 2.3 presents a transistor-level schematic of a differential amplifier.

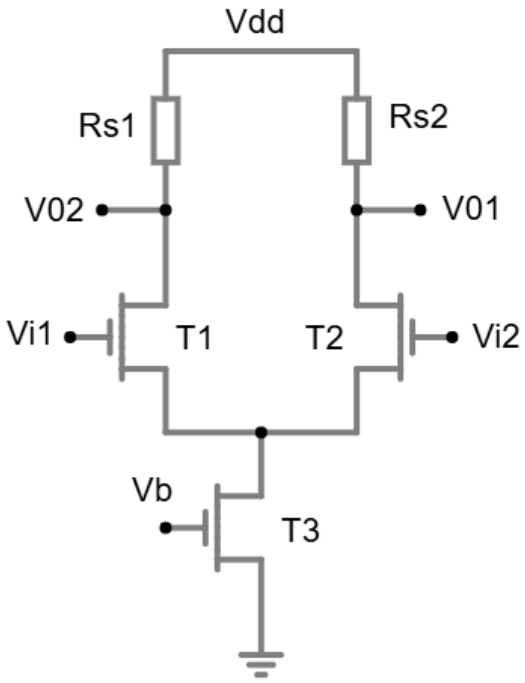


Figure 2.3: Differential Amplifier Circuit

Transistor T_3 in Figure 2.3, maintains a constant tail current flow, which ensures that the output CM level remains independent of the input CM voltage. A stable tail current is necessary to enhances the Common-Mode Rejection Ratio (CMRR), as it enforces Equation 2.5.

$$I_{D3} = I_{D2} + I_{D1} \tag{2.5}$$

This equation shows that $I_{D3}/2$ flows through T_1 and T_2 if both signal have the same input voltage. Consequential, a voltage value of $V_{dd} - R_D I_{D3}/2$ will be present at both output terminals, which is equal to the output CM value.

Assume that the gate voltage of transistor T_2 is higher than that of transistor T_1, which causes T_2 to conduct current whilst T_1 remains turned off. Consequential, a current equal to I_{D3} flows through transistor T_2, producing a voltage at node V_{01} equal to $V_{dd} - R_{s2}I_{D3}$. As the input voltage V_{i1} increases beyond the threshold voltage V_{th1}, transistor M_1 begins conducting. Due to the current coupling through I_{D3}, the current I_{D2} must decrease in order to ensure that the value of I_{D3} remains constant. This reduction in the current I_{D2} decreases the voltage drop over R_{s2}, thereby increasing the voltage at node V_{02}. As I_{D1} increases to a value equal to I_{D3}, causing I_{D2} to become sufficiently low causing transistor T_2 to be turned of [30].

The maximum output voltage swing of a differential amplifier starts from V_{dd} to $V_{in,CM} - V_{th}$ as described in [30, p. 106]. This implies that $V_{in,CM}$ needs to assume the lowest possible value. To ensure that I_{D1} and I_{D2} won't influence the I_{D3} current, transistor T_3 needs to operate in the saturation region and Equation 2.6 needs to be met. The lowest possible value of $V_{in,CM}$ can be derived from the following equations.

$$V_{DS3} \geq V_{GS3} - V_{th3} \tag{2.6}$$

$$V_{DS3} = V_{D3} - 0V = V_{S1} - 0V \tag{2.7}$$

$$V_{GS1} = V_{G1} - V_{S1} <=> V_{S1} = V_{G1} - V_{GS1} \tag{2.8}$$

If the gate voltage of transistor T_1 is equal to $V_{in,CM}$ then:

$$V_{S1} = V_{in,CM} - V_{GS1} \tag{2.9}$$

Substituting Equation 2.9 into 2.6, Equation 2.10 can be obtained [30].

$$V_{in,CM} \geq V_{GS1} + (V_{GS3} - V_{th3}) \tag{2.10}$$

Where equation 2.10 shows the minimum common-mode input voltage that can be used for a given differential amplifier. The amplification that can be achieved is determined by the small signal analyses in [30] and can be found in Equation 2.11.

$$\frac{(V_x - V_y)}{(V_{i1} - V_{i2})} = -g_m R_s \tag{2.11}$$

2.3.3 Current Mirror

Equation 2.1 holds under the condition that $V_{DS} \geq V_{GS} - V_{th}$, indicating that NMOS transistors are well-suited for use as a current source. In the saturation region, the drain current remains effectively constant with respect to variations in the drain-source voltage, provided that channel-length modulation if neglected. Under these assumptions, the current is primarily governed by the gate-source voltage. Since the current through transistor T_1 remains constant despite variations in the voltage across it, the transistor can be modeled as a high output impedance. A transistor level representation of a current mirror is depicted in Figure 2.4.

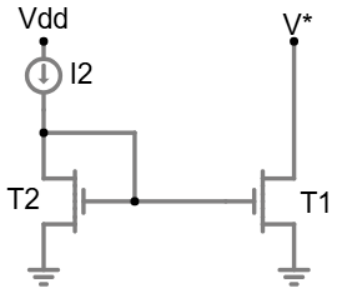


Figure 2.4: Current Mirror Circuit

In the configuration shown in Figure 2.4, the current present at I_2 is copied to transistor T_1. which can be calculated with Equation 2.12 [30].

$$I_1 = \frac{(W/L)_1}{(W/L)_2} I_2 \tag{2.12}$$

This demonstrates that the copied current is determined solely by the reference current and relative sizing of the transistors. To reduce overall current consumption, the transistors can be proportionally scaled such that the reference current, I_2, is a factor $\frac{(W/L)_2}{(W/L)_1}$ smaller than the desired output current. To ensure that even with system variation the ratio between the two transistors remains the same, it is common practice to use a unit transistor with fixed width and length. To achieve the desired scaling, these unity transistors can be placed in parallel or series, thereby effectively increasing the width or length of the overall device while preserving matching characteristics. If the channel-length modulation is taken into account then Equation 2.12 is changed to Equation 2.13.

$$I_1 = \frac{(W/L)_2}{(W/L)_1} \frac{1 + \lambda V_{DS2}}{1 + \lambda V_{DS1}} I_2 \tag{2.13}$$

Due to the channel-length modulation the current trough transistor T_1 wont be equal to the reference, unless $V_{DS1} = V_{DS2}$. Due to fluctuations in V^* this condition cannot always be met. Therefore, some techniques have been created to mitigate this effect [30, pp. 140-145]. As described earlier both drain-source voltages need to be equal to each other, which can be forced by the usage of cascoding transistors. Figure 2.5 illustrates both solutions.

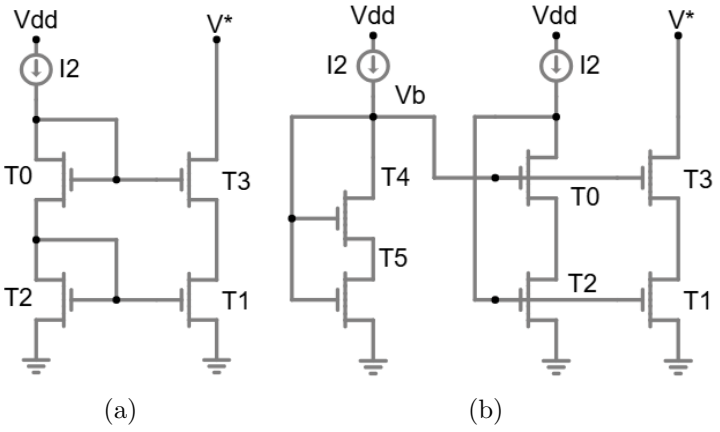


Figure 2.5: Cascoding Current Mirror [30, p. 145]

To ensure that both drain-source voltages of transistor T_1 and T_2 are equal, V_{DS1} can be forced to be equal to V_{DS2}, or vice versa. A circuit which forces V_{DS2} to be equal V_{DS1} is shown in Figure 2.5 (a) and is know for having headroom problems, if V^* is lower than a given value. The lowest value that V^* can obtain is calculated starting from Equation 2.14.

$$V_{DS0} \geq V_{GS0} - V_{th} \tag{2.14}$$

Because both source voltages are equal, Equation 2.14 an be written as:

$$V_{D0} \geq V_{G0} - V_{th} \tag{2.15}$$

$$V_{G0} = V_{D0} = V_{DS0} + V_{DS2} = V_{GS0} + V_{GS2} \tag{2.16}$$

When Equation 2.16 is substituted into Equation 2.15 then:

$$V^* = V_{G0} - V_{th} = V_{GS0} + V_{GS2} - V_{th} \tag{2.17}$$

Which is the lowest value V^* can obtain to ensure that transistor T_3 and T_4 are not driven out of saturation. To avoid a part of this headroom issue the circuit in Figure 2.5 (b) is proposed, where V_{DS1} is forced to be equal to V_{DS2}. If assumed that $V_{GS0} = V_{GS3}$ then the following equations proves that $V_{DS1} = V_{DS2}$.

$$V_{S0} = V_b - V_{GS0} \tag{2.18}$$

$$V_{DS2} = V_{D2} - V_{S2} = V_{S0} - 0V = V_b - V_{GS0} = V_{DS1} \tag{2.19}$$

Now V_b needs to be chosen to ensure that transistor T_0 and T_2 are in saturation and can be calculated by Equation 2.20 [30, P. 144].

$$V_{GS0} + (V_{GS1} - V_{th}) \leq V_b \leq V_{GS1} - V_{th0} \tag{2.20}$$

The bias voltage V_b can be generated using transistors T_4 and T_5, where T_5 establishes the required overdrive voltage and T_4 sets the corresponding gate-source voltage V_{GS}. This ensures that V_b is equal to $V_{GS1} - V_{th}$.

2.4 Improving Gain

The gain of an OPAMP is influenced by several factors, including the supply voltage, bias current, output impedance, input impedance, and other circuit-level parameters. Therefore, numerous design techniques have been proposed to ensure stable gain performance over a broader frequency spectrum.

2.4.1 Bootstrapping

As mentioned before, the output impedance plays a crucial role in the gain of an OPAMP. One technique used to improve the output impedance is the bootstrapping circuit. It operates by maintaining a constant voltage across specific circuit elements, thereby ensuring a steady current through those elements even as the overall node voltage fluctuates. As a result, the circuit appears to exhibit a higher output impedance. A bootstrapping circuit to achieve this is shown in Figure 2.6.

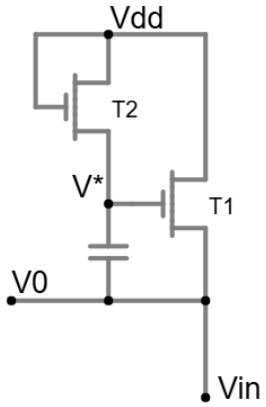


Figure 2.6: Bootstrapping Circuit

The bootstrapping circuit boosts the voltage at a given node to a value which exceeds the power supply voltage [30], utilizing positive feedback through a capacitor. It establishes a constant current by dynamical raising V^*. When the circuit shown in figure 2.6 starts up, the output voltage V_0 is initially zero, causing the capacitor to charge to $V_{dd} - V_{th}$. As V_0 increases to V_{dd}, the voltage at node V^* correspondingly rises to $V_{dd} + V_c$, where V_c represents the voltage contributed by the stored charge on the capacitor, which in this explanation is $V_{dd} - V_{th}$. As discussed before, Equation 2.1 describes the current through the drain of a transistor due to a voltage difference between the gate and source, where V_{GS} can be expressed as $V_G - V_S = V^* - V_0$, and since $V^* = V_0 + V_c$, substitution into the drain current equation yields the following expression:

$$I_D = \frac{g_m}{2} * V_C \tag{2.21}$$

This demonstrates that the current dependents solely on the voltage storred on the capacitor. If this voltage remains constant, then the current flowing through the transistor will also be constant.

2.4.2 Cascoding

The implementation of a cascoding stage will lower the effect of the Miller capacitor, which will be discussed later, and adds an extra output resistance, thereby increasing the gain and bandwidth. Such a stage can be realized by cascading a common-source (CS) with a common-gate (CG) transistor, where the CS transistor will convert a voltage into a current whilst the CG simply routes the signal through the system. The cascoding stage offers several advantages. However, it also presents certain drawbacks. Such an amplifier is presented in Figure 2.7.

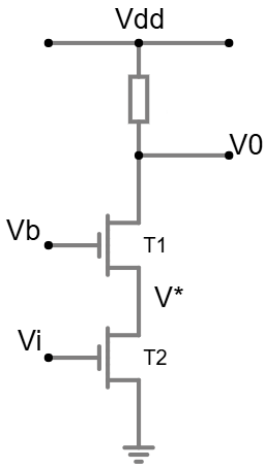


Figure 2.7: Cascoding Amplifier

One of the key advantages of the cascode amplifier is an increase in the output resistance, which results from the additional resistance and transconductance introduced by the added transistors [30]. he output resistance of the amplifier shown in Figure 2.7 can now be written as:

$$R_{out} = [1 + (g_{m1} + g_{mb1}) * R_{01}] * R_{02} + R_{01} \tag{2.22}$$

If $g_m * R_0 >> 1$, the output resistance R_{out} can be approximated as $(g_{m1} + g_{mb1})R_{01}R_{02}$, which indicates that the output impedance of transistor T_2 is effectively amplified by a factor of $(g_{m1} + g_{mb1})R_{01}$. To ensure complete signal transfer and proper operation of the circuit, it is essential that both transistors remain in the saturation region. Consequently, a cascode amplifier exhibits a minimum output voltage determined by the sum of the saturation voltages of the two transistors, which is approximately equal to twice the overdrive voltage. It is important to note that the body effect in a-IGZO can be ignored.

Before analysing how a cascode amplifier mitigates the Miller effect, it is essential to first develop a clear understanding of the effect itself. The Miller effect explains how the input capacitance can be increased due to the achieved amplification. Where the input impedance can be calculated by equation 2.23 [31, p. 725].

$$C_{in} = C_{GS} + C_{GD}(1 + A) \tag{2.23}$$

The voltage gain associated with transistor T_2 can be presented as $\Delta V^*/\Delta V_i$. The variation in current through a transistor is determined by Equation 2.24. Given that transistor T_1 and T_2 are connected in series, they share the same current flow. This relationship leads to the formation of Equation 2.25.

$$\Delta I = \frac{g_m}{2}(\Delta V_G - \Delta V_S) \tag{2.24}$$

$$g_{m1}(\Delta V_B - \Delta V^*) = g_{m2}(\Delta V_i - 0V) \tag{2.25}$$

Since V_b is a DC voltage, its small-signal variation ΔV_b is zero. When both sides of equation 2.25 is divided by ΔV_i, then the gain associated with transistor T_2 can be expressed as:

$$\frac{\Delta V^*}{\Delta V_i} = -\frac{g_{m2}}{g_{m1}} = A \tag{2.26}$$

This demonstrates that the voltage swing of node V^* is reduced relatively to V_0, leading to a corresponding reduction in the Miller effect.

2.5 Chopping

As discussed in Chapter 1, chopping is a signal modulation technique employed to shift the signal spectrum above the 1/f corner frequency, thereby mitigating the impact of low-frequency noise [32]. Figure 2.8 (a) shows a modulation circuit, called a chopper and 2.8 (b) shows the theoretical implementation.

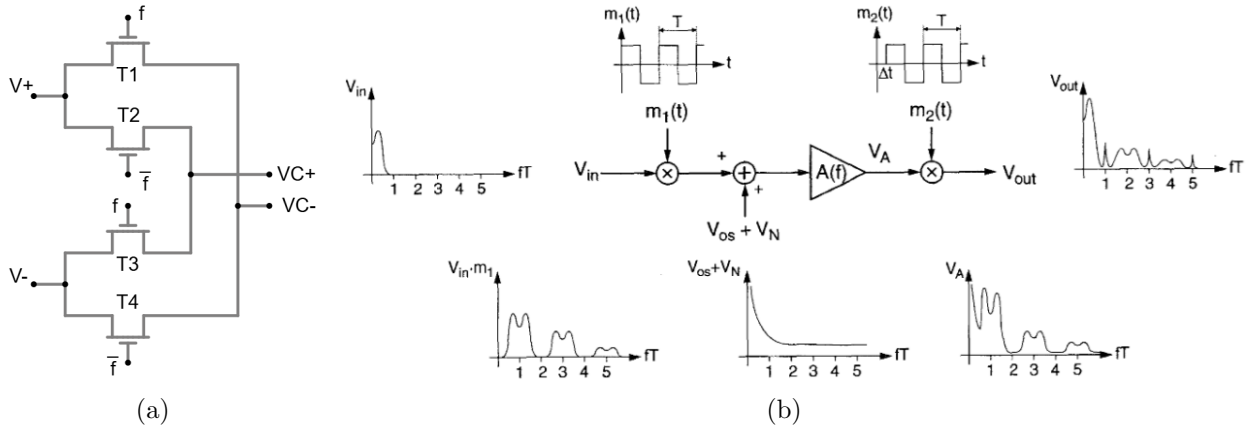


Figure 2.8: (a) Chopping Modulation Circuit (b) Theoretical Implementation [33, p. 1590]

In Figure 2.8 (a), the symbols f and $\bar{f}$ represent square waves with a frequency selected to exceed to 1/f noise corner and to prevent aliasing, where $\bar{f}$ is the digital complement inverse of f. This configuration enables the combination of transistor T_1 and T_3 as well as T_2 and T_4 to be active separately. This results in the periodic presence of V_+ and V_- at the outputs V_{C+} and V_{C-} [34], where the output signals can be mathematically write as:

$$V_{c-}(t) = (V_+(t) - V_-(t))\frac{4}{\pi}[cos(\omega_{CHOP}t) - \frac{1}{3}cos(3\omega_{CHOP}t) + \frac{1}{5}cos(5\omega_{CHOP}t) - \cdots] \tag{2.27}$$

$$V_{c+}(t) = (V_-(t) - V_+(t))\frac{4}{\pi}[cos(\omega_{CHOP}t) - \frac{1}{3}cos(3\omega_{CHOP}t) + \frac{1}{5}cos(5\omega_{CHOP}t) - \cdots] \tag{2.28}$$

Equation 2.27 demonstrates that chopping introduces harmonic frequency components, which can degrade the signal integrity. After demodulation, as illustrated if Figure 2.8 (b), the 1/f noise is translated to a frequency beyond the bandwidth of the input signal. These high-frequency components, including the shifted 1/f noise and harmonic frequencies, can subsequently be attenuated through the implementation of a low-pass filter.

It has to be noted that the implementation of chopping can itself introduce additional noise and variability into the system. This is primarily due to the capacitive coupling that exists between the various terminals in a transistors [33]. As the transistors switch at the chopping frequency f, the associated parasitic capacitances are periodically charged and discharged, leading to phenomena such as clock feedthrough. This effect can appear as an unwanted signal components at the output.

2.6 Feedback

Like many other electronic system differential amplifiers are subjected to system variability, which can arise due to manufacturing inaccuracies, temperature fluctuation, power supply variation and other environmental or process-related influences [30]. Therefore, feedback can be added to ensure an amplification which is not dependent on the transconductance of the system, but rather by a more stable component. There are two main feedback types, positive and negative feedback. With positive feedback the output signal is added in phase with the input signal, which can increase the gain, but pushes the system further to instability. With negative feedback, the output signal is added to the input signal with a 180° degree phase shift, effectively subtracting the output signal from the input. Such a negative feedback system is shown in Figure 2.9. The phase margin of a feedback system is defined as the difference between the phase shift introduced by the system and 180°, measured at the frequency where the loop gain magnitude equals unity. If the phase shift reaches 180°, negative feedback becomes positive feedback, potentially leading to instability.

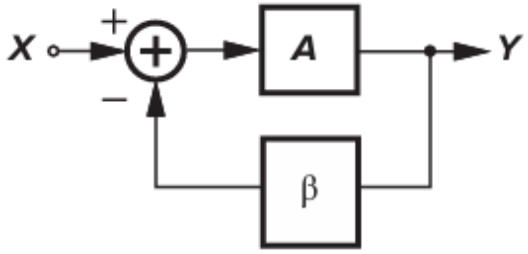


Figure 2.9: Negative Feedback System [30, p. 276]

In Figure 2.9, the symbol A represents the open-loop gain of the system and β the feedback factor. The systems amplification can be obtained with Equation 2.29 [30] and is called the closed loop-gain.

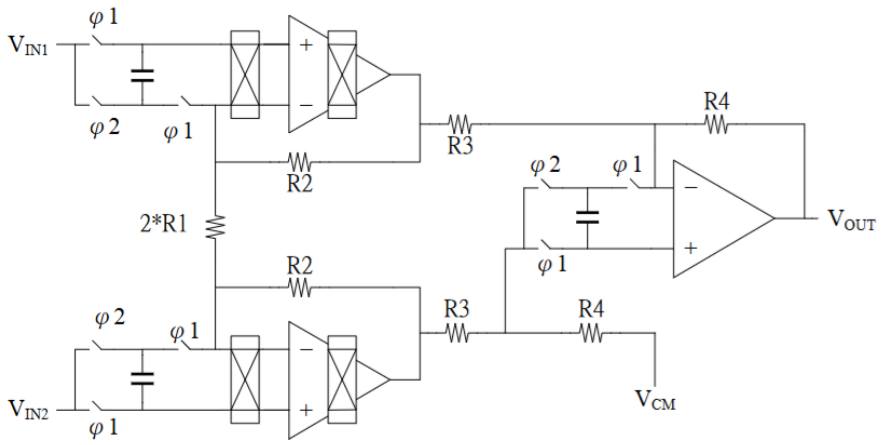
$$\frac{Y}{X} = \frac{A}{1 + \beta A} \tag{2.29}$$

It can be observed that increasing βA reduces the systems overall dependence on the open-loop gain. To further understand this topic, a system without feedback is considered, effectively changing the transfer function to $Y = A \cdot X$. In this open-loop amplification, any variation in A will effected the output by the same factor. However, when negative feedback is applied, this variation also appears in the denominator of the closed loop transfer function, effectively lowering its effect on the output.

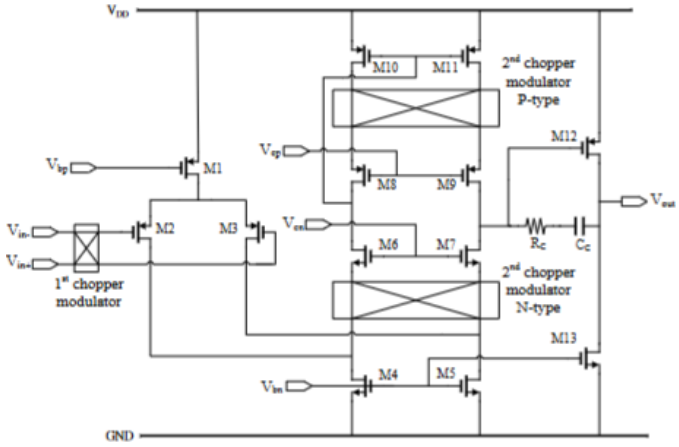
2.7 Bio-Potential Amplifiers

2.7.1 CMOS

Most OPAMPs fabricated in c-Si are single-ended outputs, meaning that the signal is amplified with respect to ground. [35] proposes the system presented in Figure 2.10 and shows that the AFE amplifier uses three OPAMPs, chopping, and auto-zeroing. Where auto-zeroing is used to mitigate the effect of white noise on the system [36].



(a) Three-OPAMP Design with Auto Zeroing and Chopping



(b) Chopping OPAMP Transistor Level

Figure 2.10: CMOS ECG Amplifier [35, p. 328]

The presented amplifier can be divided into two subsections, with each a specific purpose:

- **First stage:** which is represented by two OPAMPs with their feedback interconnected forming a fully differential amplifier. In this arrangement, each amplifier amplifies its input signal relative to the output of the other, effectively amplifying the voltage difference between the two inputs.

- **Second stage:** this stage amplifies the difference of both signal, thereby enhancing the CMRR while providing additional gain. The resistance R_6 can be used to normalize the output, ensuring that it remains within a specified voltage range.

This circuit operates with a 1.2 V power supply and consumes 1.32 mW of power. It achieves a voltage gain of 40.09 dB with a bandwidth of 69 kHZ, whilst having CMRR exceeding 60 dB. The chopping and auto-zeroing mechanisms require a external clock signal, operating at frequencies of 10 and 20 kHZ, respectively.

Certain circuit configurations have been engineered wherein a network of NMOS transistors are employed to emulate the operational characteristics of a PMOS transistor. [37] presents an OPAMP which employes pseudo-CMOS elements to implement feedback. The proposed OPAMP operates at a supply voltage of 5 V, achieving a voltage gain of 22.5 dB and consuming 160 µW of power.

2.7.2 Unipolar MOS

Due to the unavailability of PMOS transistors during the early development of OPAMPs, extensive research was conducted on circuits utilizing only NMOS transistors. Early studies report that a voltage gain of up to 50 dB can be achieved with a 30 V supply voltage [38]. For implementation in a-IGZO, a three stage amplifier architecture is proposed in [39], as illustrated in Figure 2.11.

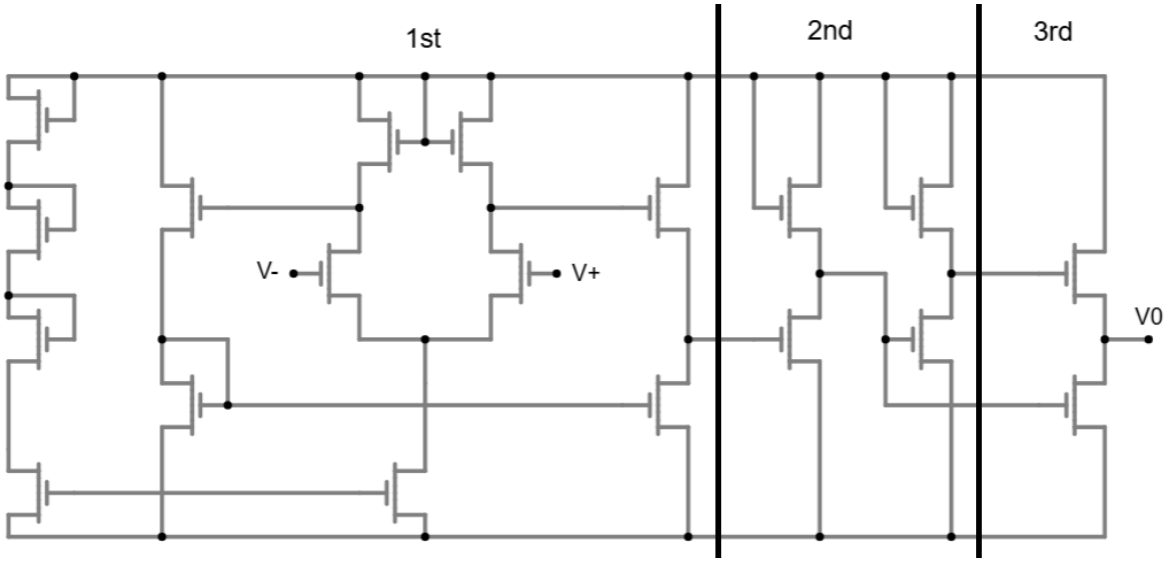


Figure 2.11: NMOS Only OPAMP Design [39, p. 657]

Figure 2.11 visually separates the three stages using bold black lines. The function of each stages is described as follows:

- **First stage:** uses a differential pair with a constant current source, to improve the CMRR of the OPAMP. The constant current source is configured as a current mirror, ensuring stable current flow that remains unaffected by variations in the system's load [40]. The output of the differential pair is connected to a differential-to-single-ended converter, where the current delivered to the second stage is determined by the output of the differential pair. It has to be mentioned that due to the use of NMOS transistors, the maximum output voltage swing is limited to $V_{dd} - V_{th}$ [30, P. 55].
- **Second stage:** is formed from a basic cascaded amplifier, ensuring the necessary amplification.

- **Third stage:** is used as a buffer, ensuring effective signal transfer by mitigating the effects of the output impedance [39], [41]. It is characterized by a high input and a low output impedance, which facilitates impedance matching and prevents signal degradation [42],[43].

The paper reports a voltage gain of 23.52 dB, achieved with a supply voltage of 20 V and a power consumption of 51 mW. The amplifier demonstrates that the unity-gain bandwidth is achieved at 2.37 MHz, with a phase margin of 102°.

[44] proposes a fully differential amplifier, characterized by the presence of two complementary output signals. Although the differential amplifier is intended to be used for EMG signals, its architecture may serve as a valuable reference for the amplification of ECG signals as well. One notable feature of the proposed differential amplifier is the implementation of chopping at multiple frequencies, which enables the usage of a single output lead to serve an array of amplifiers. Figure 2.12 shows the proposed differential amplifier at transistor level.

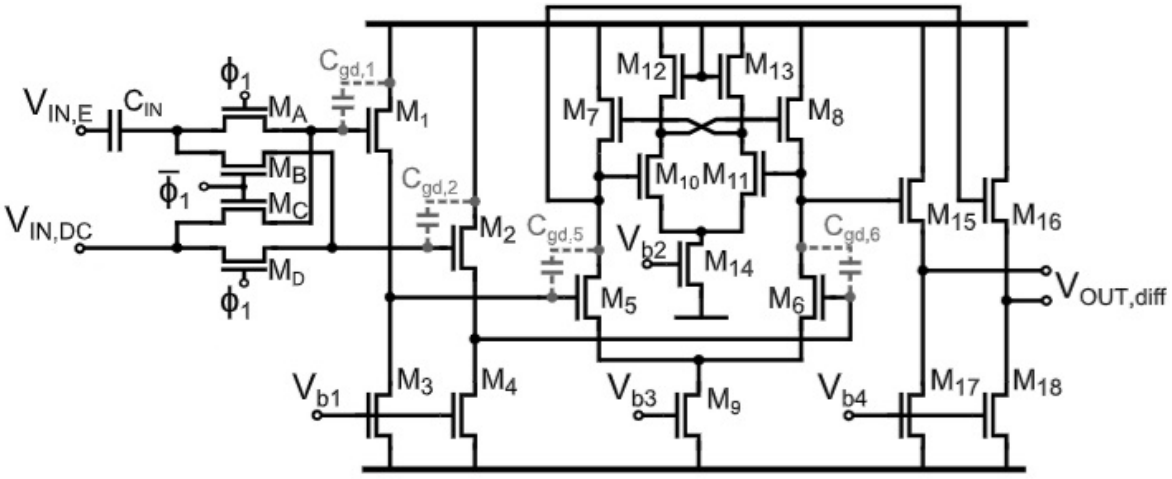


Figure 2.12: Fully Differential OPAMP with Input Chopping [44, p. 144]

Figure 2.12 shows a differential amplifier with multiple embedded stage:

- $\boldsymbol{M_A - M_D}$**:** are used to modulate the signal to a designated chopping frequency, effectively shifting it above the 1/f noise region to enhance signal integrity. In this implementation, chopping is also used to modulate individual EMG signals to distinct frequencies, allowing multiple signals to be transmitted over a single lead.
- $\boldsymbol{M_1 - M_4}$ **and** $\boldsymbol{M_{15} - M_{18}}$**:** are used as a buffer to ensure accurate signal transfer and to shift the signal to a preferred DC operating level.
- $\boldsymbol{M_5 - M_{14}}$**:** uses 2 separate differential pairs, with internal feedback. Transistors M_{10} to M_{14} are used as a auxiliary amplifier, which improves the output resistance of M_7 and M_8 by reducing the small-signal swing.

The differential amplifier operates with a 26 V power supply and achieves a maximum voltage gain of 24.9 dB. It provides a bandwidth of 5.4 kHZ whilst maintaining a power consumption of 1.3 mW.

2.8 Analogue Front-End

An AFE is used to increase the amplitude and current of an analogue signal to a value which can be transferred into a digital signal by the use of an analogue-to-digital converter (ADC). A visual representation is provided in Figure 2.13.

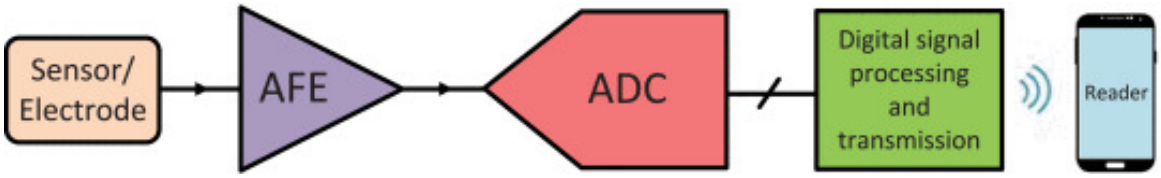


Figure 2.13: Visual Representation of a Analogue Front-end [45, p. 746]

The input resolution determines the gain required from the AFE to ensure accurate analogue-to-digital conversion without signal information loss. The equation to define the minimum input voltage to achieve a bit change is defined in [46], and is shown in Equation 2.30.

$$V_{lsb} = \frac{V_{fullscale}}{2^N} \tag{2.30}$$

In this context, V_{LSB} represents the lowest input value, $V_{fullscale}$ denotes the maximum analogue voltage value and N the resolution in bits at the output. When $V_{fullscale}$ is equal to the supply voltage, values of V_{LSB} reported in the literature vary: [47] and [48], which use a 10 V power supply, report values of 4 mV and 19 mV, respectively. To use the the full output, the ECG signal, which has an output swing between 1.0 and 1.4 mV, needs to be amplified to a maximum value of 10 V. For these ADCs a gain of 77 dB has to be realised by the AFE.

A more recent study reports the design of an ADC operating with a 4 V power supply. Allowing the AFE to have a lower gain of approximately 66 dB [49].

In addition to providing amplification, the AFE must exhibit a sufficiently high input impedance to ensure proper low-current signal transfer. [50] specifically addresses this requirement and suggest a minimum input impedance of 1.9 $G\Omega$.

2.9 Conclusion

Some implementations have been discussed to increase the gain of the amplifier. However, these approaches often introduce added side effects. The state-of-the-art indicates that a-IGZO amplifiers exhibit relatively low amplification compared to Si counterparts, despite the operation at comparatively high supply voltages. These elevated supply voltages contribute to the increase in power consumption, which is undesirable for application in flexible patches, where low power operation is essential.

Chapter 3

Designed Circuits

3.1 Introduction

In this section of the master's thesis, various differential amplifier designs are developed and explained. Each differential amplifier discussed in this chapter shares a common current referencing circuit, which is depicted in Chapter 2, Figure 2.4. While the reference circuit remains consistent, the biasing current and size of the transistors are adjusted for each individual amplifier configuration. After covering differential amplifiers, the chopper design will be discussed.

The different transistor sizes can be obtained in one of two ways, the square-law or the g_m/I_d model. In the square-law approach, Equation 2.1 is used to calculate the current through each transistor in the system. These currents can be combined to achieve the amplification equation which is equal to V_{out}/V_{in}. With the g_m/I_d method a transistors transconductance is directly coupled to its drain current, which places a transistor in one of its three distinct regions [51]. Each region has its design trade-offs, which are shown in Table 3.1. It has to be noted that the g_m/I_d values are obtained from [52], which are measured for silicone based transistors.

Table 3.1: g_m/I_d Design Trade-offs

regions	Trade-off	g_m/I_d (V^{-1})
Weak Inversion	Low Power, High Gain	20 to 40
Moderate Inversion	Moderate Gain, Moderate Speed, Moderate Power	7 to 20
Strong Inversion	High Power, High Speed	3 to 7

Table 3.1 outlines the appropriate operating region for a transistor based on desired design trade-offs. In this master's thesis, the differential pairs are used in the moderate inversion region to balance the efficiency and speed, while the output stages are used in the strong inversion region to ensure high drive capability and improve linearity.

3.2 Simple Differential Amplifier

Due to the unipolar nature of the a-IGZO technology, which only supports NMOS transistors, the first amplifier design is relatively basic. The fundamental building blocks utilized in the circuit, shown in Figure 3.1, are based on the methodologies proposed in [30].

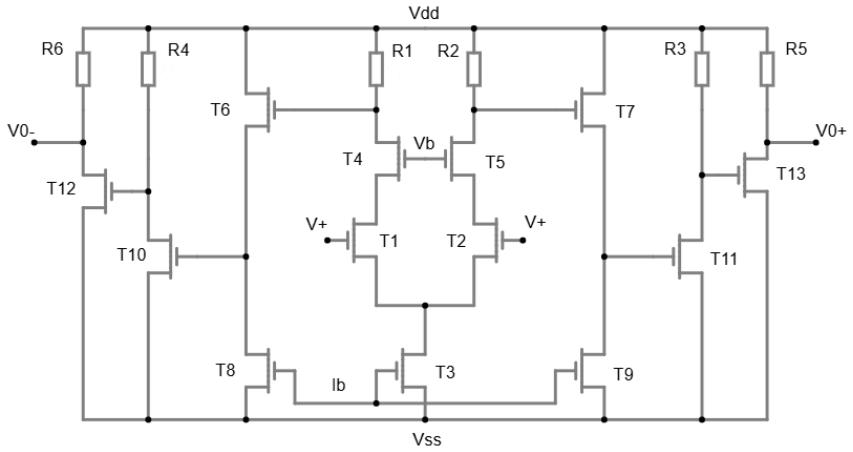


Figure 3.1: Three Stage Simple Differential Amplifier

Figure 3.1 shows a three stage differential amplifier with resistive loads, where each stage has its own purpose:

- **T1-T5**: ensure the common-mode functionality through the use of a shared and constant current source. Transistors T4 and T5 are configured in a cascode arrangement, as described in Chapter 2. This configuration mitigates the Miller effect, but increases the output common-mode voltage, which in turn reduces the available output swing. However, this also increases the output resistance, thereby enhancing the gain of the amplifier.

- **T6-T9**: lower the input voltage by V_{th}, thereby enabling a greater output voltage swing in the subsequent stages.

- **T10-T13**: create additional amplification. Resistors R4 and R3 are chosen to ensure that transistors T12 and T11 remain in the saturation region. Furthermore, resistor R6 and R5 are selected so that the input and output common-mode voltages are matched.

The proposed differential amplifier is designed to operate with a supply voltage of 3 V and utilizes a reference current of 3.1 µA. The bias voltage applied at the gates of transistors T4 and T5 is maintained at 2 V to ensure proper transistor operation. The different transistor sizes are shown in Table 3.2.

Table 3.2: Simple Differential Amplifier Sizes and Values

Transistor	W/L (µm/µm)	multiplier	Resistor	R (kΩ)
T1,T2,T4,T5	10/1.2	4	R1,R2	1000
T3,Tbias	5/1.2	7	R3,R4	330
T6,T7	1/0.6	1	R5,R6	150
T8,T9	5/1.2	1		
T10,T11	15/1.2	3		
T12, T13	15/1.2	1		

In Table 3.2 the transistor size of Tbias and T3 ensure that the current present at the bias transistor, within margins, is translated to the drain current of T3 without scaling.

3.3 Diode-Load Differential Amplifier

As discussed in Chapter 2, resistive loads can be replaced by diode-connected transistors. While this approach offers certain advantages, such as improved matching and area efficiency, it also has some design trade-offs. One of these trade-offs is the maximum allowable common-mode voltage, which in turn limits the overall output voltage swing. An example of a differential amplifier using diode-loads is illustrated in Figure 3.2.

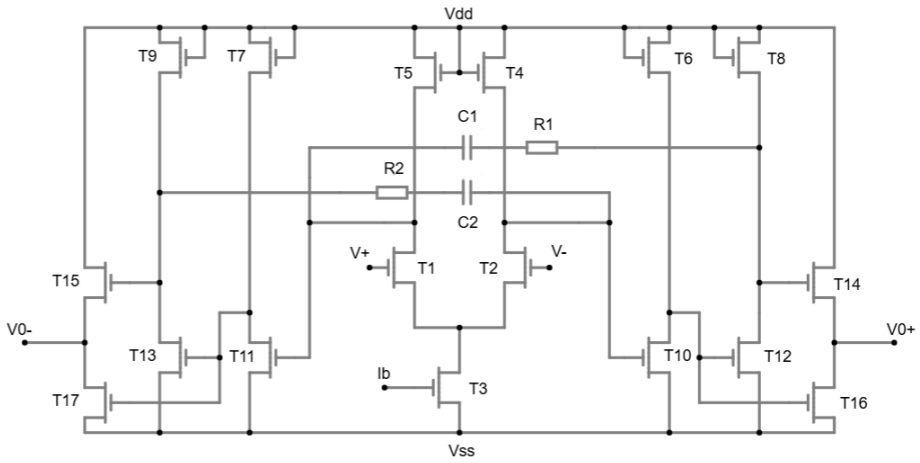


Figure 3.2: Three Stage Diode-Load Differential Amplifier

In Figure 3.2, a supply voltage of 5 V is used with a 21 µA biasing current. As explained before, the voltage drop is now created by a diode-connected transistor and not a resistive load. Although this circuit shares structural similarities with the previously discussed topology, it introduces several differences. One of the added elements is feedback by capacitive and resistive components. This technique, commonly referred to as Miller compensation, plays a role in increasing the stability of a system by shifting the dominant and non-dominant poles to a lower and higher frequency, respectively [53],[54]. A second key difference is the removal of the source-follower stage and the addition of a buffer stage at the output to ensure reliable signal transfer. To scale the different transistors, the transfer function is calculated with the transconductance of the different devices, which is shown in Appendix B. The different parameters for the components used in this circuit are presented in Table 3.3.

Table 3.3: Diode-Load Differential Amplifier Sizes and Values

Transistor	W/L (µm/µm)	multiplier	Resistor	R (kΩ)
T1,T2	200/1.2	4	R1, R2	70
T3,Tbias	180/1.2	7	Capacitor	C (pF)
T5,T4	1/1	1	C1,C2	8
T6,T7	80/1.2	1		
T8,T9	11.1/1.2	2		
T10, T11	70.8/1.2	8		
T12, T13	20/0.9	4		
T14, T15	40/1.2	2		
T16, T17	20/1.2	2		

For this circuit a layout is created using the PragmatIC Semiconductors 600nm technology node [55]. The resulting layout is illustrates in Figure 3.3. As previously discussed in the schematic analyses, the layout can be divided into three distinct substage, corresponding to the functional blocks of the amplifier.

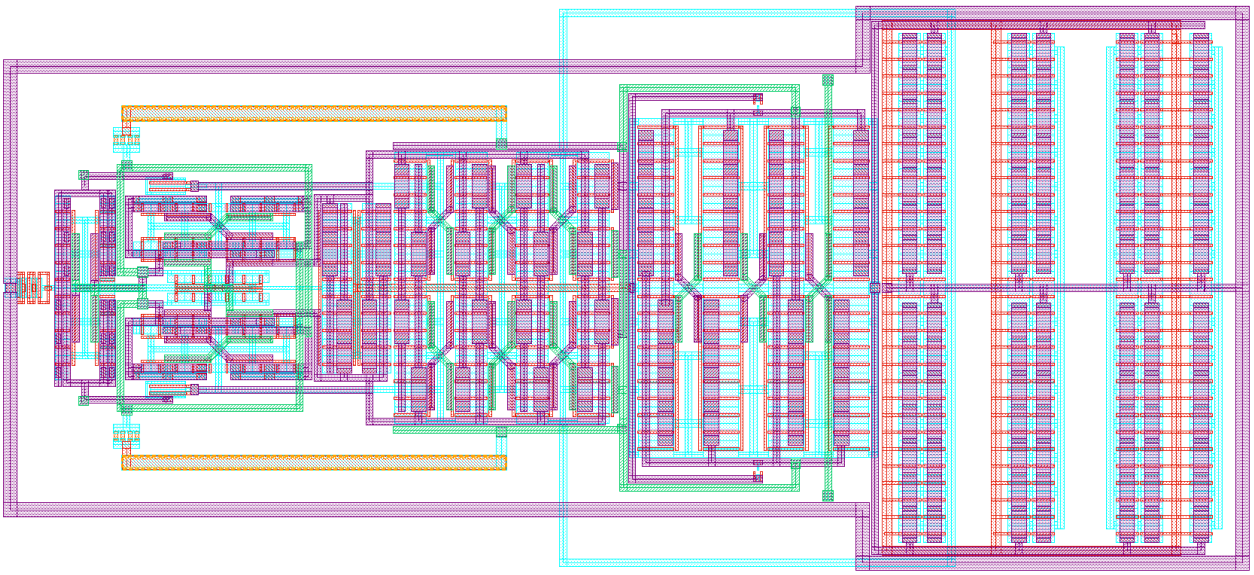


Figure 3.3: Diode-Load Differential Amplifier Layout

A more detailed representation of the layout is provided in Appendix A. The designed circuit employs a common-centroid layout technique, minimizing mismatch by ensuring that transistors operating in complementary roles are equally affected by coupling from aggressor signals [56],[57]. This layout strategy is evident in Figure A.4, where metal layers 1 and 2 are crossed to ensure connection between the different transistor stacks. To mitigate the impact of mechanical stress induced by overlying metal layers, these are extended across adjacent transistors to ensure uniform stress distribution. Metal layer 1 is primarily used to route signals within individual amplification stages. In the third amplification stage, diode-connected transistors are positioned between the input transistors to reduce layout area, as illustrated in Figure A.7.

3.4 Bootstrapped Differential Amplifier

The bootstrapping circuit is created out of two stages. The fundamental principle underlying bootstrapping is discussed in Chapter 2. By employing a feedback mechanism, it can assure, within certain limits, that the voltage present at the gate of a transistor is a predetermined amount greater then that of the source. This results in a constant gate-source voltage difference ΔV_{gs}, which in turn stabilizes the drain current I_d. The implementation of a bootstrapping circuit in a differential amplifier is illustrated in Figure 3.4, whilst Table 3.4 shows the different values for the used transistors, capacitors and resistors.

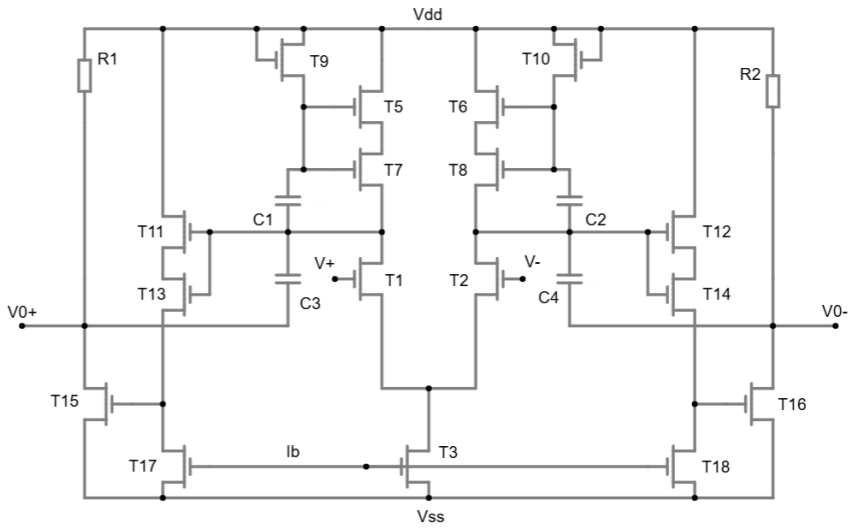


Figure 3.4: Two Stage Bootstrapped Differential Amplifier

Table 3.4: Bootstrapped Differential Amplifier Sizes and Values

Transistor	W/L (µm/µm)	multiplier	Resistor	R (kΩ)
T1,T2	30/1.2	4	R1, R2	100
T3	180/1.2	7	Capacitor	C (F)
Tbias	60/1.2	7	C1,C2	800µ
T5,T6,T7,T8	1/1.2	2	C3,C4	10p
T9,T10	20/0.6	1		
T11,T13,T12,T14	1.5/0.6	2		
T17, T18	60/1.2	7		
T15, T16	15/1.2	25		

The circuit illustrated in Figure 3.4 operates with a 3 V power supply and 1 µA biasing current. Transistors T1 to T3 form a differential pair configuration, as previously described. In this implementation, the traditional resistive loads are replaced with a bootstrapping circuit, which is represented by transistors T5 to T10 and capacitors C1 and C2. Transistors T7 and T8 function as cascoded devices, ensuring a lower common-mode voltage at the output of the differential stage. Transistors T9 and T10 are diode-connected to prevent current flow towards the power supply rail. Following the first stage, a level shifter circuit is employed to further lower the common-mode voltage, ensuring that transistors T15 and T16 remain in saturation region during operation. Capacitor C3 and C4 are used as Miller compensation, which is discussed before.

As shown in Table 3.4, transistor Tbias is sized to be three times smaller than T3. This sizing results in a biasing current that is approximately one-third of the current flowing through the differential pair, thereby contributing to a reduced overall power consumption in the circuit.

3.5 Transconductance Boosting Differential Amplifier

The final implemented circuit employs a feedback mechanism to enhance the transconductance of specific transistors. This technique, known as transconductance boosting, is similar to bootstrapping in that it stabilizes the current through the load of the differential pair. As a result, the load node presents a higher effective impedance, thereby improving the overall gain of the amplifier. In bootstrapping the feedback is of the capacitive kind, whilst in the Transconductance boosting a source sensing differential pair is used which increases the gate voltage relative to the source voltage, ensuring that V_{gs} of a transistor is stable [44], [58], [59].

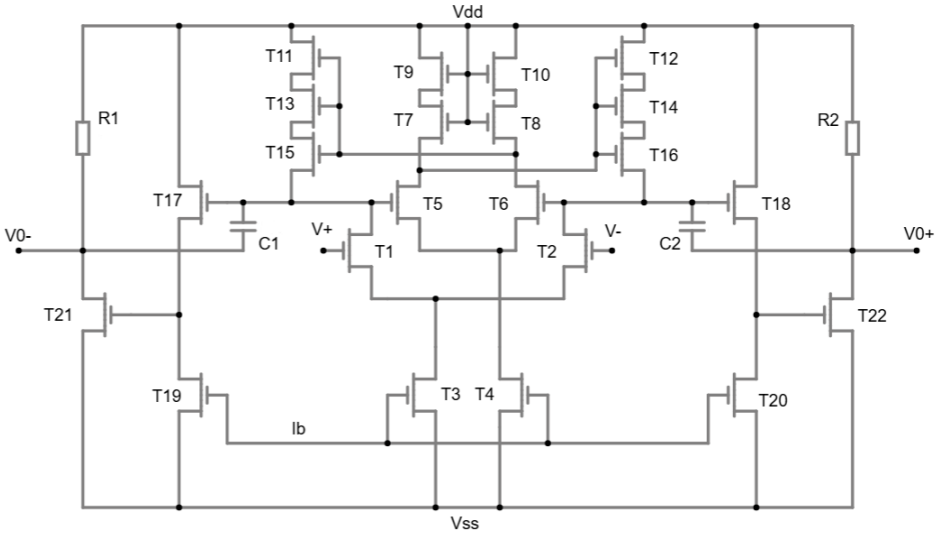


Figure 3.5: Two Stage Transconductance Boosting Differential Amplifier

The circuit in Figure 3.5 is implemented using a 3 V power supply and 1 µA biasing current. It uses two current reference transistors, T3 and T4, which are utilized to bias two separate differential pairs. One differential pair, with transistors T5 and T6, is responsible for sensing the source voltage of the load transistors T11 to T16. Transistors T1 and T2 operate as a conventional differential pair with their output connected to a source-follower and an additional amplification stage. The different used component values can be found in Table 3.5.

Table 3.5: Transconductance Boost Differential Amplifier Sizes and Values

Transistor	W/L (µm/µm)	multiplier	Resistor	R (kΩ)
T1, T2	24/0.6	3	R1, R2	180
T3, Tbias	6/1.2	2	Capacitor	C (pF)
T4	3/1.2	1	C1,C2	5
T5, T6	12/1.2	2		
T7, T8, T9, T10	15/1.2	5		
T11, T12, T13 T14, T15, T16	3/1.2	1		
T17, T18	3/0.6	1		
T19, T20	15/1.2	1		
T21, T22	10/1.2	11		

3.6 Implemented Feedback

As discussed in Chapter 2, negative feedback can mitigate the effects of system variability on the amplification. In this master's thesis, only capacitive feedback is applied to remove the DC offset from the skin electrode and to set the mid-band gain [60]. A visual representation of the feedback applied on the differential amplifiers can be found in Figure 3.6.

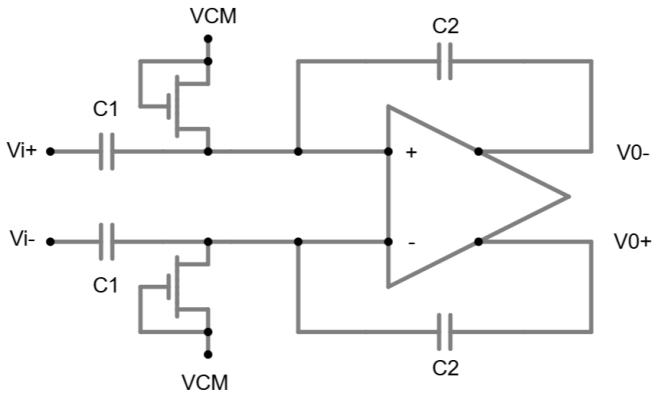


Figure 3.6: Capacitive Feedback on Differential Amplifier

Each amplifier designed in this master's thesis needs a certain DC offset at the input to ensure proper operation. Given that the input DC voltage may vary, an input capacitor C1 is employed to block the signal's DC component. Subsequently, a diode-connected transistor pulls the DC component of the signal up to the desired operating point. In this configuration, the gain of the amplifier is defined by the capacitor ratio C1/C2 instead of the transconductance of the internal components. However, the gain is ultimately limited by the maximum achievable open-loop gain. The used values for capacitors C1 and C2 in simulation are 10 nF and 5 pF, respectively, which should result in an amplification of 66 dB. Because 10 nF can have complications on flexible chip, due to area constraints, the capacitor sizes could be reduced to 2 nF and 1 pF.

3.7 Chopping Modulation Circuit

Chapter 2 explains why chopping is necessary and how it can be implemented. An illustration of the chopping modulating circuit can be found in Figure 3.7.

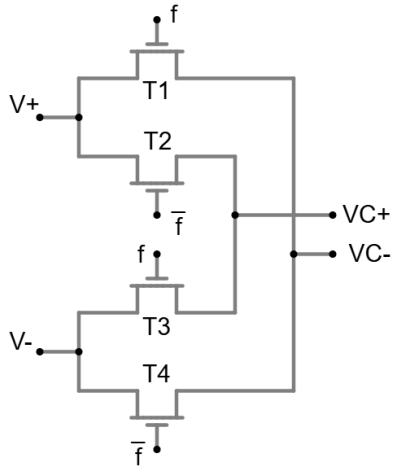


Figure 3.7: Chopping Modulator

To determine the appropriate sizing of the transistors used in Figure 3.7, several key transistor properties need be taken into consideration. One critical factor is device mismatch, which arises due to variations introduced during the fabrication process and can significantly affect signal integrity [61]. The degree of variation that can appear in a MOSFET is inversely proportional to the square root of its width and length, indicating that larger devices are generally less effected by process-induced variability. This relationship is studied in [62] and is mathematically expressed by Equation 3.1.

$$\sigma_{\Delta X} = \frac{A_X}{\sqrt{WL}} \tag{3.1}$$

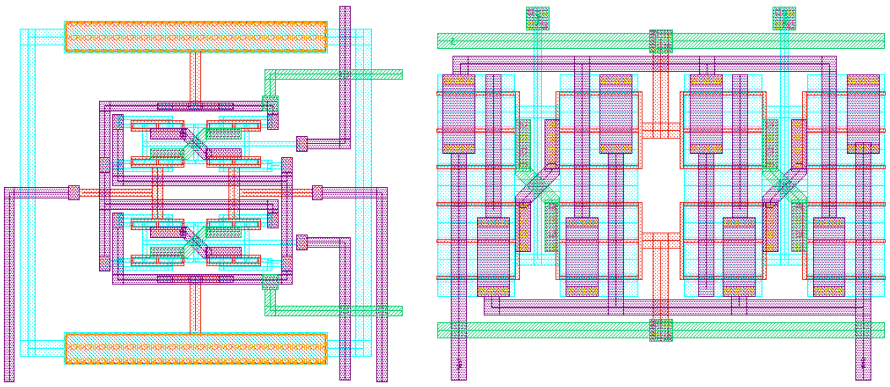
Where A_X is determined by the technology node.

As shown in Equation 3.1, larger transistors are less prone to process-induced variability. However, increasing transistor dimensions introduces trade-offs that must be considered. Specifically, larger transistors exhibit lower on-resistance, which lowers the voltage drop between drain and source when the transistor is conducting. Moreover, increased gate area leads to a higher parasitic capacitance, particularly the gate-to-source and gate-to-drain parts, which increase effects such as clock feedthrough. Therefore, transistor sizing must be optimized to reduce process-induced variability whilst decreasing clock feedthrough and transistor resistance. The selected transistor dimensions for the chopping modulation and demodulation circuits are presented in Table 3.6.

Table 3.6: Chopping Modulation Circuit Sizing

	Transistor	W/L (µm/µm)
chopping	T1, T2, T4, T5	3/0.6
dechopping	T1, T2, T4, T5	60/0.6

For the chopping circuit, layouts have been created, with the common-centroid technique in mind. The chopping modulator and demodulator layouts can be found in Figure 3.8. A full implementation with the layout created in Subsection 3.3 can be found in Appendix A Figure A.9



(a) (b)

Figure 3.8: (a) Chopping Modulator Layout (b) chopping Demodulator Layout

Chapter 4

Simulations and Analysis

4.1 Designed Test Benches

To evaluate the various designs, several test benches were developed. Each test bench targets a specific aspect of the evaluation process and will be examined in detail in this section.

4.1.1 Frequency Response

A Bode plot is used to observe the systems response to varying input frequencies. Such a plot illustrates the magnitude of the output signal relative to the input, while also presenting the phase margin between them. To obtain the frequency response, a 500 mV signal with a 180° phase shift is applied to each input, ensuring a unity voltage between them. To asses the stability of the system, the gain is first analysed in an open-loop configuration. If the system demonstrates stability under these conditions, feedback can subsequently be introduced, and its effects can be evaluated using the same test bench. For a system to become stable, an open-loop phase margin between 45° and 70° has to be obtained [24]. An illustration of the implemented test bench can be found in Figure 4.1.

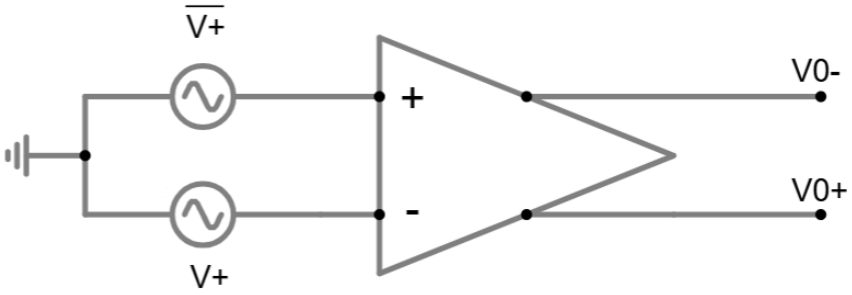


Figure 4.1: Frequency Response Test Bench

4.1.2 Transient Response

Since chopping introduces rapidly rising edges into the signal, the system must respond appropriately to such inputs. This behaviour can be evaluated by applying a square wave to the system. The implemented transient response test bench can be found in Figure 4.2.

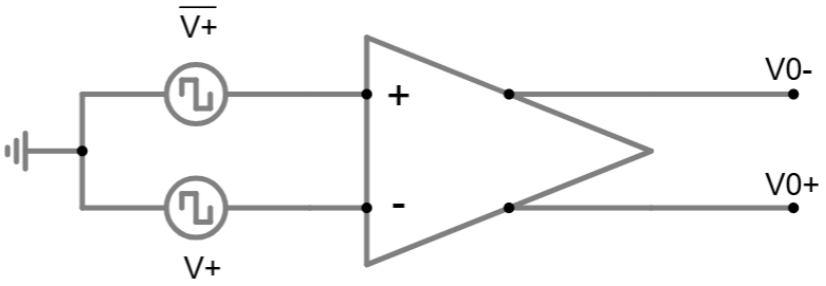


Figure 4.2: Square Wave Transient Response Test Bench

The square wave, as employed in Figure 4.2, is applied at frequencies of 1 kHz and 5 kHz, with an amplitude equal to 1 V. The output then illustrates the systems response to such stimuli and can be use to assess whether the system is suitable for operation with chopping. Replacing the square signal with with a sine wave allows for an estimation of the power consumption for each amplifier, which is a critical metric for application in flexible devices.

4.1.3 Common-Mode Rejection Ratio

The Common-Mode Rejection Ratio (CMRR), as defined in [30], is a measure of the extent to which the common-mode voltage appears at the output relative to the desired differential signal. Equation 4.1, obtained from [30], can be used to calculate the CMRR.

$$CMRR = \left| \frac{A}{A_{CM}} \right| \tag{4.1}$$

The value for the differential gain is already obtained in Subsection 4.1.1. To measure the common-mode present at the output, a new test bench is introduced, which applies a 1 V amplitude sine wave with zero phase shift to both inputs. This test bench is illustrated in Figure 4.3.

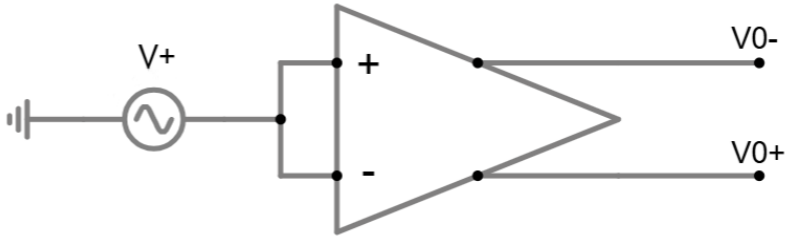


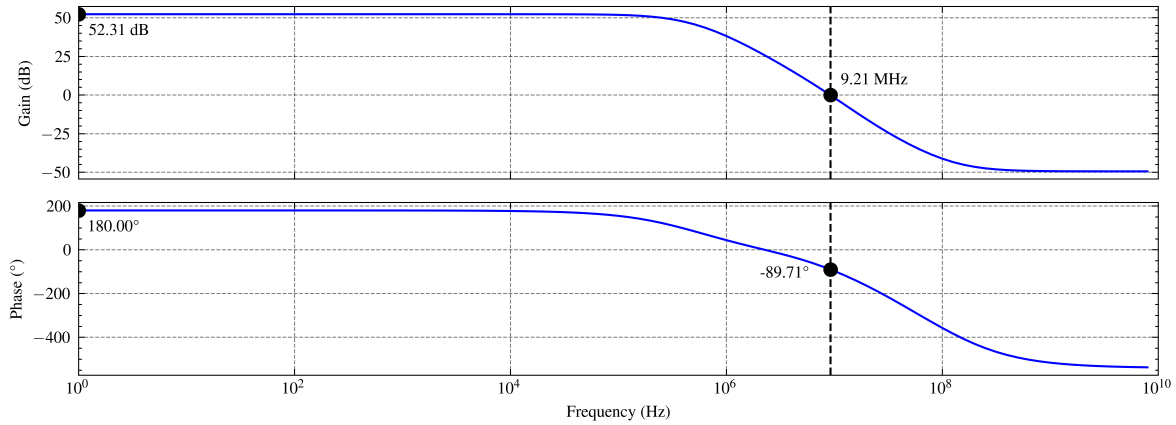
Figure 4.3: Common-Mode Test Bench

4.2 Differential Amplifier Simulation Results

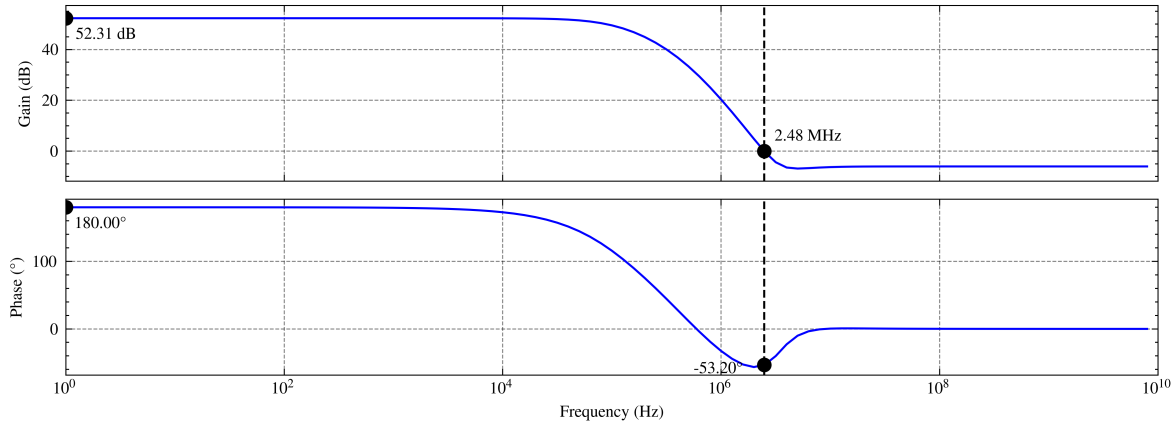
4.2.1 Simple Differential Amplifier

Bode Plot:

Figure 4.4 shows the Bode plot obtained from the Simple Differential Amplifier (SDA) with and without feedback. Each figure has a graph displaying the gain and phase, which are connected by the frequency present at the bottom. The Bode plot is simulated for frequencies up to 10 GHz.



(a)



(b)

Figure 4.4: Bode Plot Simple Differential Amplifier (a) Without Feedback (b) With Feedback

Figure 4.4 shows that the SDA has a gain equal to 52.31 dB, with a unity gain bandwidth (UGBW) of 9.21 MHz. Without feedback, the system has a phase margin (PM) of 90.29°. This indicates that the system is highly stable, and damps any oscillation that may occur [30, PP. 410-455]. One downside to an increased phase margin is a slower response to variations at the input.

Introducing feedback into the system decreases the UGBW, whilst also decreasing the frequency at which the gain drops by 3 dB, which is called the -3 dB point, and can be found at approximately 100 kHz. The gain of the system with feedback does not change, which is as expected because the closed-loop gain is limited by the achievable open-loop gain. One notable observation is the increase in phase margin, making the system more stable then it already was, and has a value of 126.8°.

Transient Response:

The transient response of the square wave, is simulated for 1 ms. The output of the SDA can be found in Figure 4.5, where the green and red lines represent the different outputs.

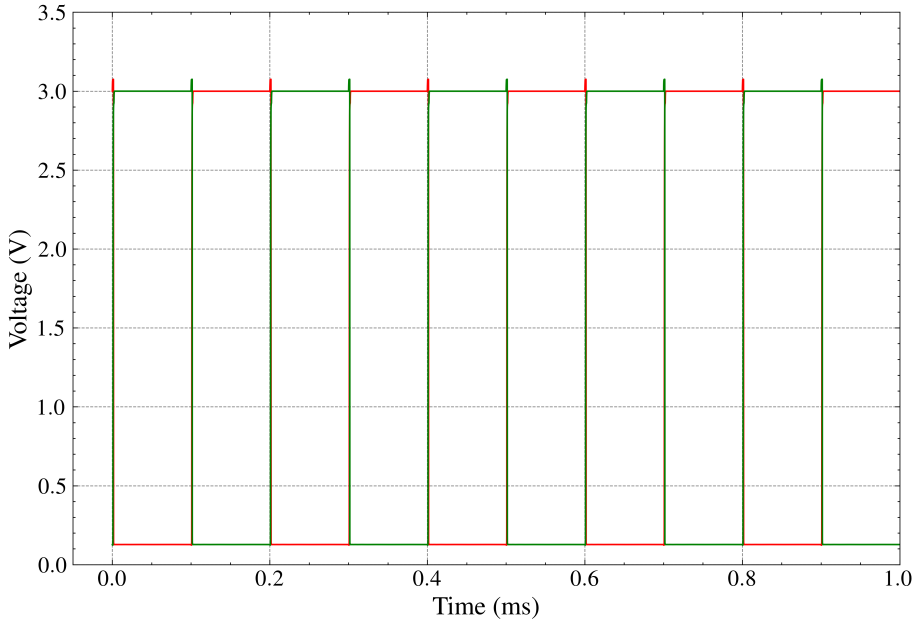


Figure 4.5: Square Wave Response of the Simple Differential Amplifier Closed-Loop

In the square wave shown in Figure 4.5, a slight overshoot can be observed prior to the signal being pulled down. The attained amplitude indicates that the system reaches full saturation, suggesting that the maximum output voltage has been achieved. This behaviour can be attributed to the systems gain, which amplifies a 1 V input signal to a level exceeding 3 V.

Results:

The Bode plot for the CMRR can be found in the Appendix C (Figure C.1), which has a maxim value of 38.49 dB. Its -3 dB point is reached at around 136 kHz, whereafter it reaches 0 dB at approximately 2.55 MHz. As discussed before, the square wave of the transient test bench can be replaced by a sinus source, which gives a power consumption estimate of the system when its maximum usable gain is reached. Its important to note that this system uses a 1.5 V DC offset at the input. The different values obtained are summarized in Table 4.1.

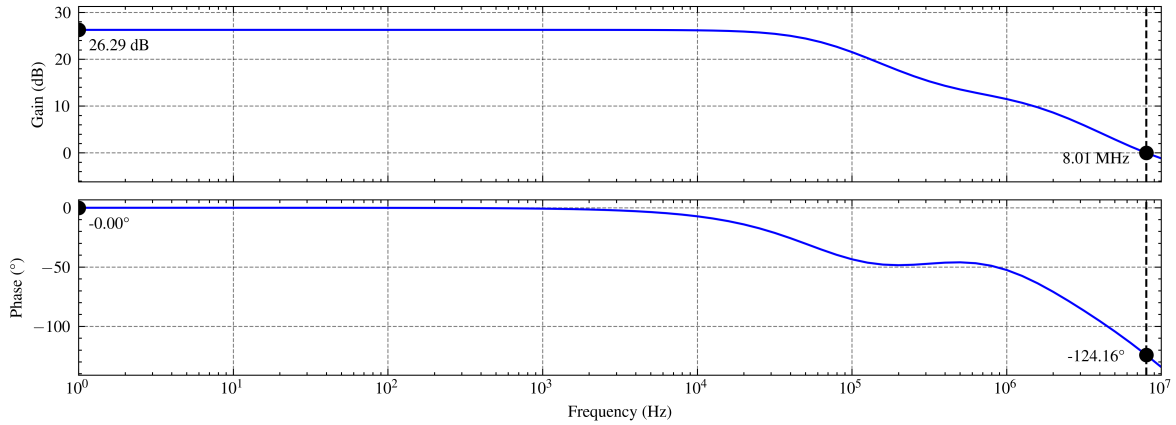
Table 4.1: Simple Differential Amplifier Obtained Values

	No Feedback	Feedback
Input Common-Mode (V)	1.5	1.5
Maximum Gain (dB)	52.31	52.31
-3 dB (kHz)	290	136
UGBW (MHZ)	9.21	2.55
PM (°)	90.29	126.8
Power (µW)	110.5	110.5

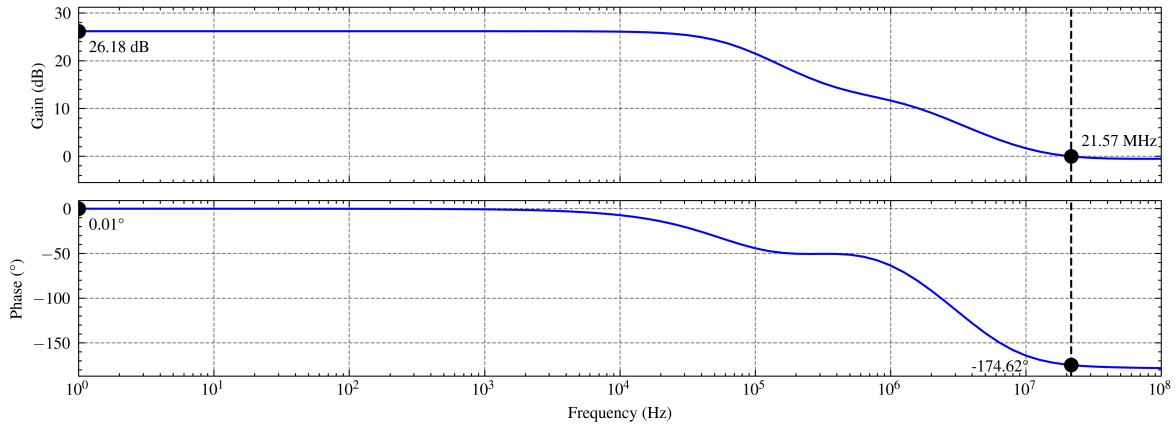
4.2.2 Diode-Load Differential Amplifier

Bode Plot:

Figure 4.6 show the Bode plot of the differential amplifier which uses diode-connected loads, also called the Diode-Load Differential Amplifier (DLDA). The systems without and with feedback are simulated to a frequency of 10 and 100 MHz, respectively.



(a)



(b)

Figure 4.6: Bode Plot Diode-Load Differential Amplifier (a) Without Feedback (b) With Feedback

The maximum gain reached by the DLDA is illustrated in Figure 4.6 and has a value of 26.29 dB, with the -3 dB point at a frequency of approximately 62 kHz. The system reaches the unity gain at a frequency of 8.01 MHz. At this frequency the system has a phase shift of -124.16°, resulting in a PM of 55.84°. This illustrates that the system is stable enough to be tested with feedback [30, PP. 410-455].

The added capacitive feedback decreases the amplification of the system whilst increasing the unity gain frequency to 21.57 MHz. At this frequency, the phase shift has a value of -174.62°, which is lower then the system without feedback. This decreases the PM to a value of 5.58°, and results in an unstable system. Negative feedback subtracts a portion of the output from the input, by giving the output a phase shift of 180°. However, if the overall loop phase shift approaches 180° at a frequency where the loop gain is still ≥ 1, the negative feedback effectively becomes positive feedback, which can cause oscillations to occur [30].

In Appendix D (Figure D.1) the Bode plot of the DLDA without Miller compensation can be observed. It shows that the unity gain frequency is reached at 9.45 MHz, which is 1.44 MHz higher then with Miller compensation. This shows that a decrease in the UGBW is traded for an increase in the PM.

Transient Response:

The transient response of the DLDA to a square wave can be found in Figure 4.5, and is simulated for 1 ms.

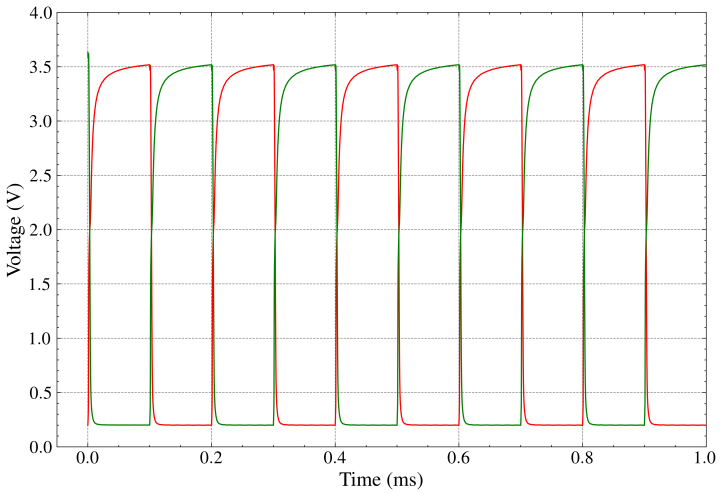


Figure 4.7: Square Wave Response of the Diode-Load Amplifier Open-Loop

As illustrated in Figure 4.7, the system exhibits a charging characteristic at both the positive and negative flanks. This can be explained by a low slew rate, which will be explained later in this chapter. Due to the use of a 5 V power supply and a relatively low amplification, the amplifier does not reach saturation.

Results:

The Bode plot of the CMRR is presented in Appendix C (Figure C.2). As shown, the CMRR reaches a value of 55.79 dB, with the first pole appearing at approximately 20 kHZ. after which, the CMRR gradually decreases, approaching 0 dB at a frequency beyond the simulation range. This improved CMRR can be attributed to the use of larger transistor sizes, which enhances device matching and reduces susceptibility to system variability. However, a key drawback of using larger transistors is the increased current requirement to maintain the same g_m/I_d ratio. A summary of the obtained values from various plots and simulations is provided in Table 4.2.

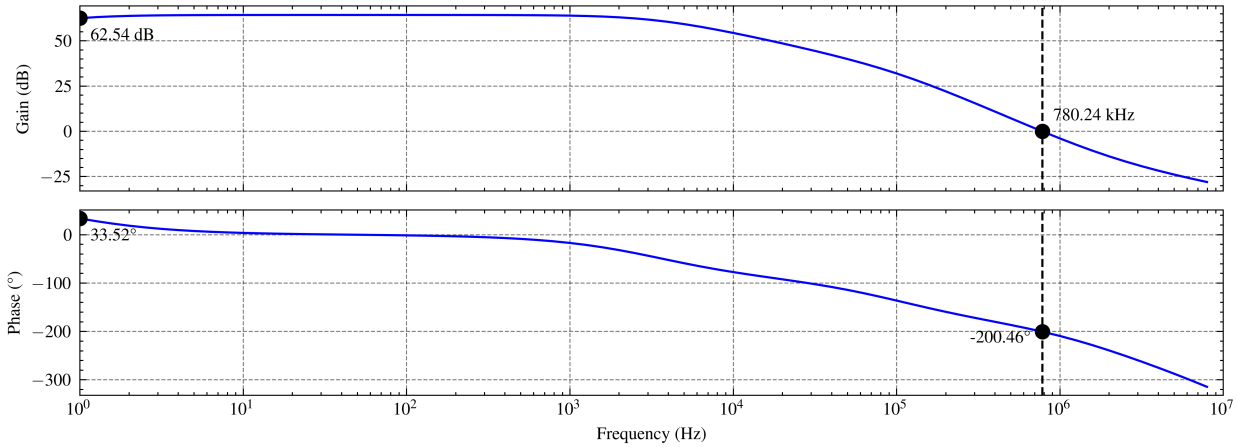
Table 4.2: Diode-Load Differential Amplifier Obtained Values

	No Feedback	Feedback
Input Common-Mode (V)	2.5	2.5
Maximum Gain (dB)	26.29	26.18
-3 dB (kHZ)	62	67
UGBW (MHZ)	8.01	21.57
PM (°)	55.84	5.58
Power (mW)	58.9	39.46

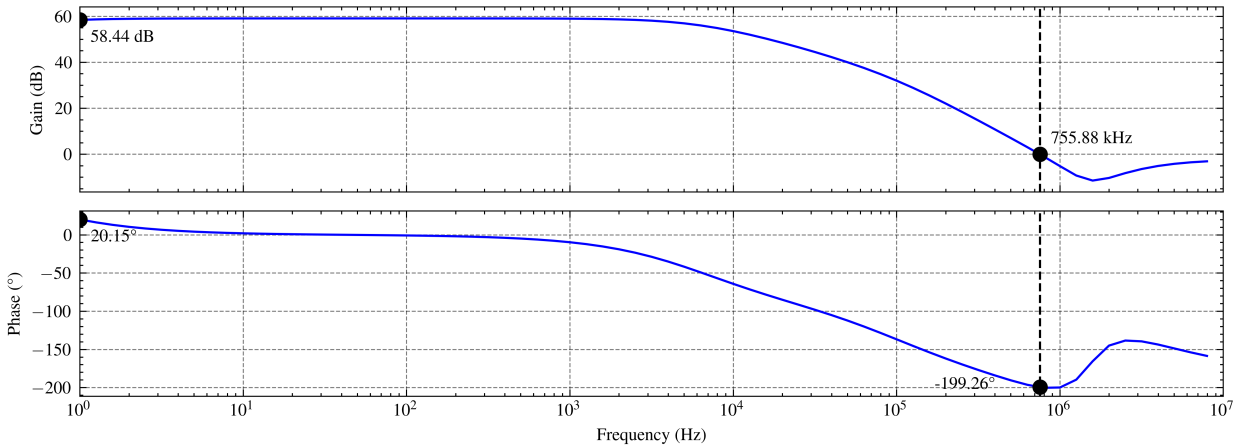
4.2.3 Bootstrapped Differential Amplifier

Bode Plot:

The Bode plot for the Bootstrapped Differential Amplifier (BDA) is simulated untill a frequency of 80 MHz, and can be found in Figure 4.8.



(a)



(b)

Figure 4.8: Bode Plot Bootstrapped Differential Amplifier (a) Without Feedback (b) With Feedback

The Bode plot of both the open- and closed-loop configuration of the BDA indicates that the system is unstable, as evidenced by a negative PM. The stability could be improved by increasing the capacity of the Miller compensation. However, this adjustment introduces a design trade-off, as it would further reduce the gain at 5 kHZ.

The open-loop system does reach an amplification of 62.54 dB with a -3 dB point at approximately 3 kHz. The system crosses the unity gain at a frequency of 780.24 kHz with a phase shift of -200.46°. In the feedback system this cross over appears earlier at a frequency of 755.88 kHz, where a phase shift of -199.26° can be observed.

Transient Response:

The transient response of BDA can be found in Figure 4.9, and has a simulation window of 1 ms which shows the full transient response.

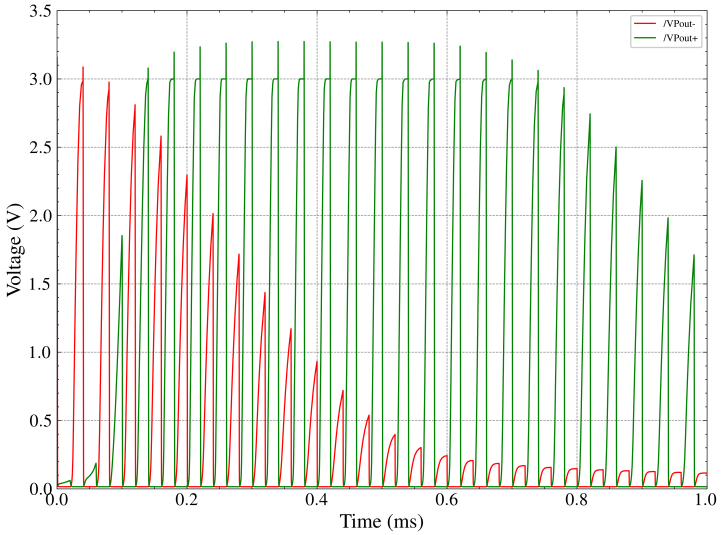


Figure 4.9: Square Wave Response of the Bootstrapped Differential Amplifier Open-Loop

It can be observed in Figure 4.9 that the BDA has a poor transient response to a square wave input. One of the output signals is suppressed, whilst the amplitude of the other increases. This indicates an imbalance in the differential output, and can be cause by the instability observed in the Bode plot. Figure 4.10 shows that the suppression of the output can be mitigated by the use of feedback.

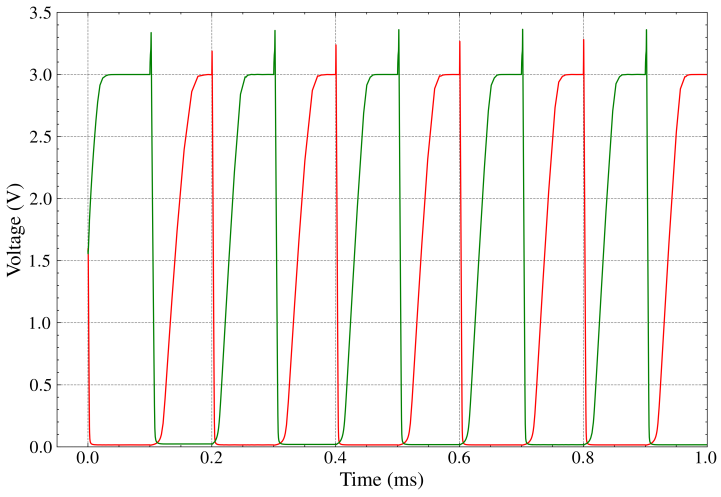


Figure 4.10: Square Wave Response of the Bootstrapped Differential Amplifier Closed-Loop

Results:

The CMRR has a maximum value of 49.41 dB, and can be found in Appendix C (Figure C.3). Its -3 dB point is observed at approximately 5 kHz, whereafter it reaches 0 dB at around 1 MHz. Table 4.3 summarises the different values obtained for the BDA, which shows that there is a slight difference in power consumption between the open- and closed-loop implementations.

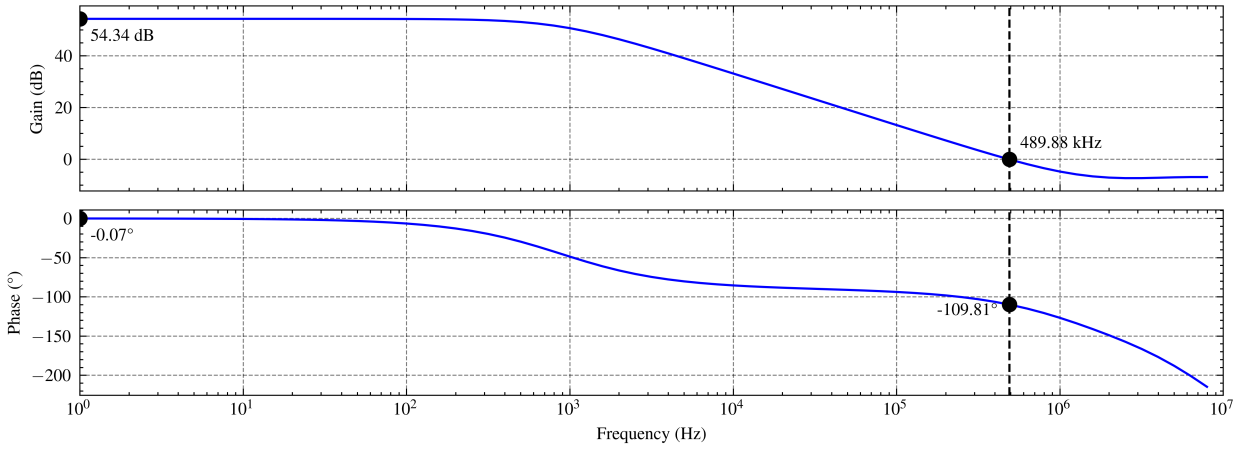
Table 4.3: Bootstrapped Differential Amplifier Obtained Values

	No Feedback	Feedback
Input Common-Mode (V)	1	1
Maximum Gain (dB)	62.54	58.44
-3 dB (kHz)	3	6
UGBW (kHZ)	780.24	755.88
PM (°)	-20.46	-19.26
Power (µW)	104.37	101.9

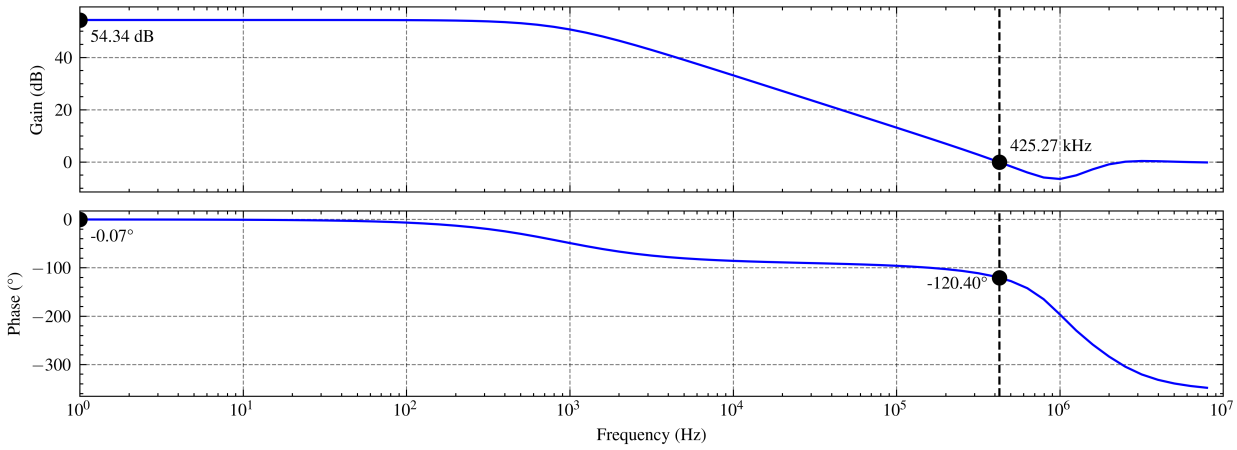
4.2.4 Transconductance Boosting Differential Amplifier

Bode Plot:

Figure 4.11 shows the Bode plot for the implemented Transconductance Boosting Differential Amplifier (TBDA), with a maximum simulation frequency of 80 MHz.



(a)



(b)

Figure 4.11: Bode Plot Transconductance Boosting Differential Amplifier (a) Without Feedback (b) With Feedback

The Bode plot in Figure 4.11 shows that the system remains stable with and without feedback. This stability can be attributed to implementation of Miller compensation. As shown in Appendix D (Figure D.3), the system without it is unstable with a PM of -8°. By introducing Miller compensation, the PM is significantly improved, although this comes at the cost of a reduced UGBW. The obtained PM for the open- and closed-loop systems are 70.12° and 59.6°.

The TBDA reaches a maximum amplification of 54.34 dB for both systems. The -3 dB point can be observed at 1 kHz, and the unity gain bandwidth at 489.88 kHz and 425.27 kHz for the open- and closed-loop systems, respectively.

Transient Response:

The transient square wave response of the TBDA can be observed in Figure 4.12

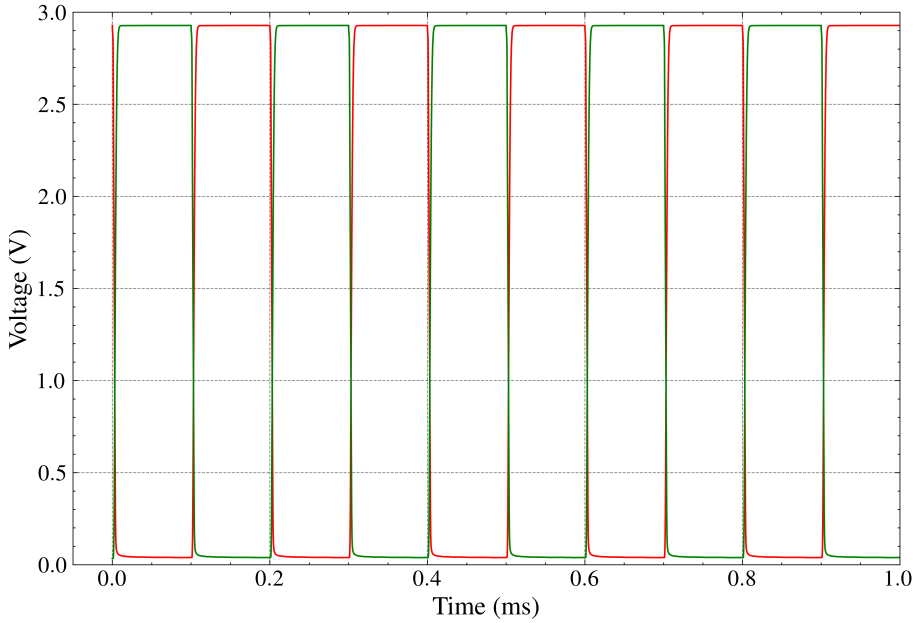


Figure 4.12: Square Wave Response of the Transconductance Boosting Differential Amplifier Closed-Loop

The square wave signal at the output exhibits a slight charging characteristic, which may lead to performance issues when higher frequencies are applied to the system. Additionally, the system reaches saturation at a lower amplitude compared to the previous designs. This behaviour can be attributed to the reduced voltage headroom caused by the use of NMOS transistors as impedance loads in the differential pair.

Results:

The system shows a maximum CMRR of 57.15 dB, and reaches 0 dB at around 2.6 MHz. The Bode plot of the CMRR is shown in Appendix C (Figure C.4). In this figure, a spike can be observed at a frequency of 125.4 kHz, which reaches a value of 53.44 dB. The different obtained values are summarized in Table 4.4.

Table 4.4: Transconductance Boosting Differential Amplifier Obtained Values

	No Feedback	Feedback
Input Common-Mode (V)	1	1
Maximum Gain (dB)	54.34	54.34
-3 dB (kHz)	1	1
UGBW (kHZ)	489.88	425.27
PM (°)	70.12	59.60
Power (µW)	105.6	105.6

4.3 Electrocardiogram Test Bench

To simulate the transient response of the implemented systems to a chopped electrocardiogram (ECG) signal, a test bench is designed to apply this signal, obtained from a two-lead measurement. In this configuration, the heart can be modelled as a low-current voltage source, with the two leads connected to the inverting and non-inverting outputs of that source. This representation is illustrated in Figure 4.13, and shows that the V_{in-} lead is an exact inverse of V_{in+}, indicating ideal differential signal conditions. The test bench itself is illustrated in Figure 4.14.

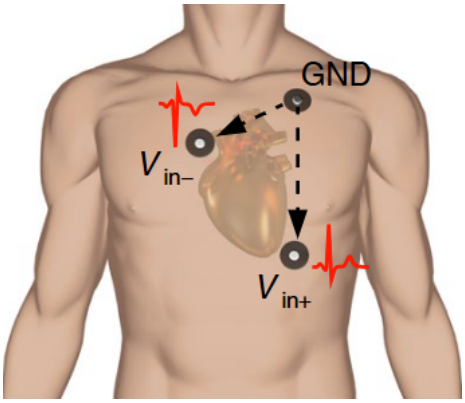


Figure 4.13: Visual Representation Of An ECG Signal Source [63, p. 358]

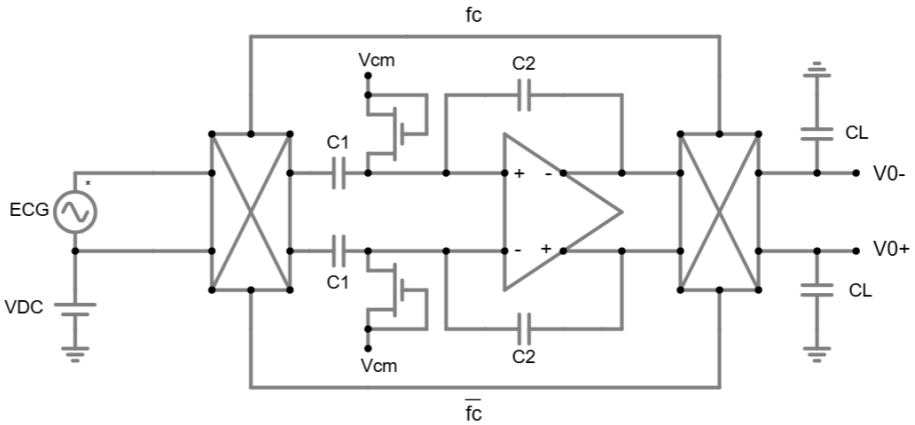


Figure 4.14: Designed Test Bench for ECG Signal Simulation

In Figure 4.14, the applied signal is sourced form [64], which is a medical study focused on the detection of sleep apnea using an ECG. A transient illustration of this signal can be found in Figure 4.15, with a 1.5 V DC offset. The load capacitors C_L at the outputs are used as a low-pass filter to remove the added 1/f noise and other parasitic signals added by the system.

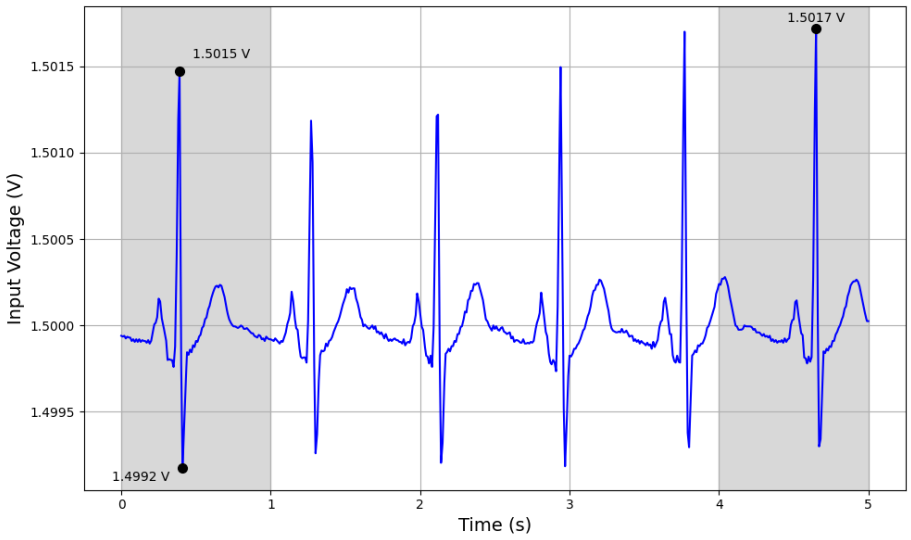


Figure 4.15: Transient Representation of the ECG Signal

4.4 Electrocardiogram Simulation Results

In Subsection 4.2, two promising differential amplifiers were identified: the SDA and TBDA, due to thier high amplification and stability. These amplifiers will be evaluated using the ECG test bench with chopping frequencies of 1 and 5 kHz. An output load capacitance of 20 nF is used to refine the simulations, although such a value is difficult to realize on-chip. The output of the chopping modulator, without a connected differential amplifier, can be found in Figure 4.16. This figure reveals the presence of small spike following each transition, which may degrade signal quality.

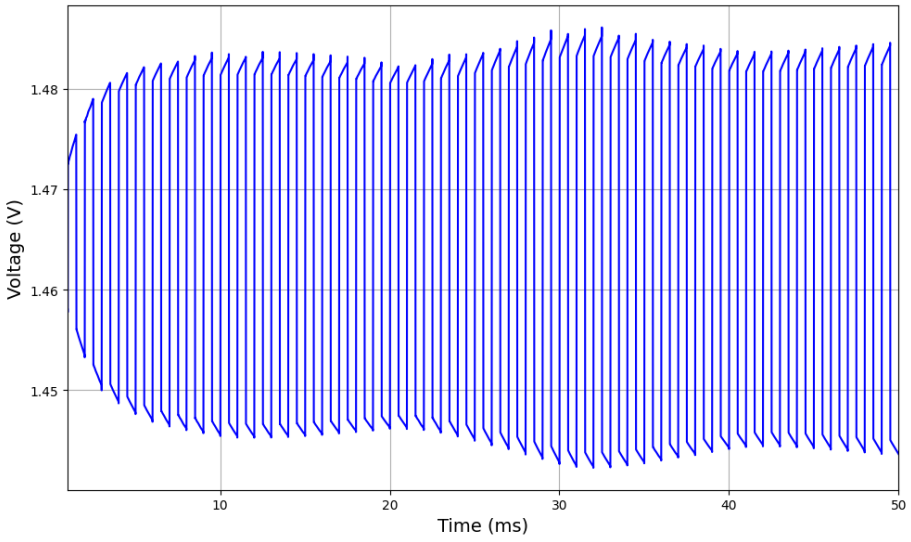


Figure 4.16: Chopped Electrocardiogram

4.4.1 Simple Differential Amplifier

Chopping at 1 kHz:

Observed from the Bode plot, shown in Figure 4.4, a gain of 52 dB can be reached for a 1 kHz frequency. When the chopped ECG signal is applied to the SDA, Figure 4.17 can be observed.

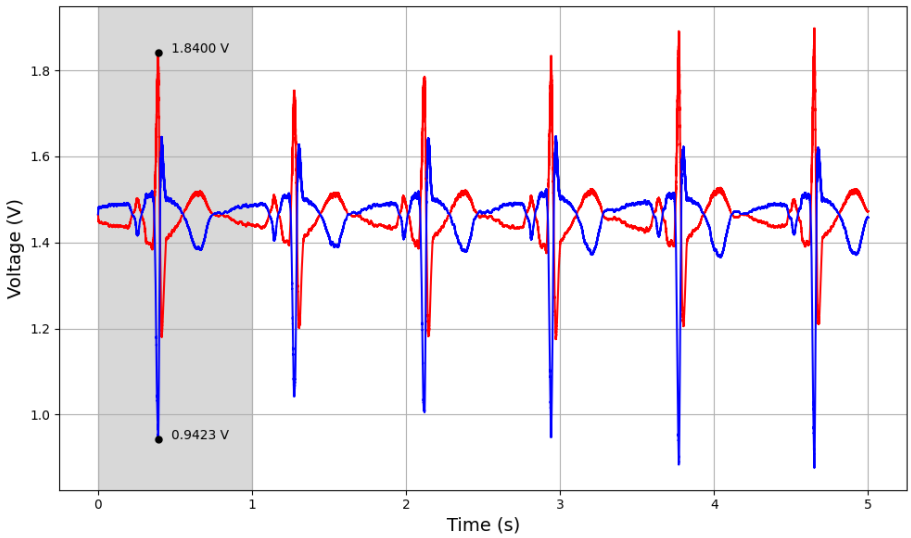


Figure 4.17: Simple Differential Amplifier Output f_{chop}=1 kHz

In Figure 4.17, a peak-to-peak voltage of 898 mV, between the outputs V_{0+} and V_{0-}, can be observed during the first simulation second, indicated by the grey-shaded region. The obtained signal has a small ripple effect attributed to the charging characteristic observed in Figure 4.5. Despite this ripple, the ECG signal is clearly visible. To verify whether the output is a clean, amplified version of the input signal, a single-ended representation is derived by subtracting V_{0+} from V_{0-}, as shown in Figure 4.18. The linearity of the system can be assessed by comparing the gain obtained between two distinct points, which in a linear system, should be equal.

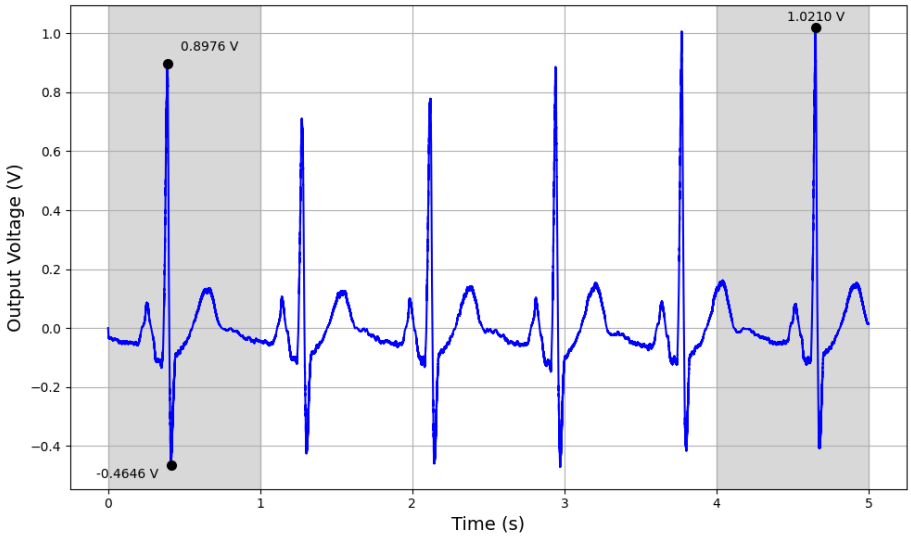


Figure 4.18: Single-Ended Output Simple Differential Amplifier f_{chop}=1 kHz

The single-ended representation in Figure 4.18 shows a voltage difference of 1.36 V. When compared to the input signal in Figure 4.15, corresponds to an approximate gain of 55.4 dB.

The gain calculated between the positive peaks in the first and last second is 55.81 dB. Although a ripple is present at the output, most of the characteristic ECG features are retained, indicating high signal integrity. This ripple can be examined in greater detail in Appendix E (Figure E.1).

Chopping at 5 kHz:

Because the first pole of the SDA is observed after 5 kHz, an amplification of 52 dB should be achievable. The transient response of the SDA with 5 kHz chopping is illustrated in Figure 4.19.

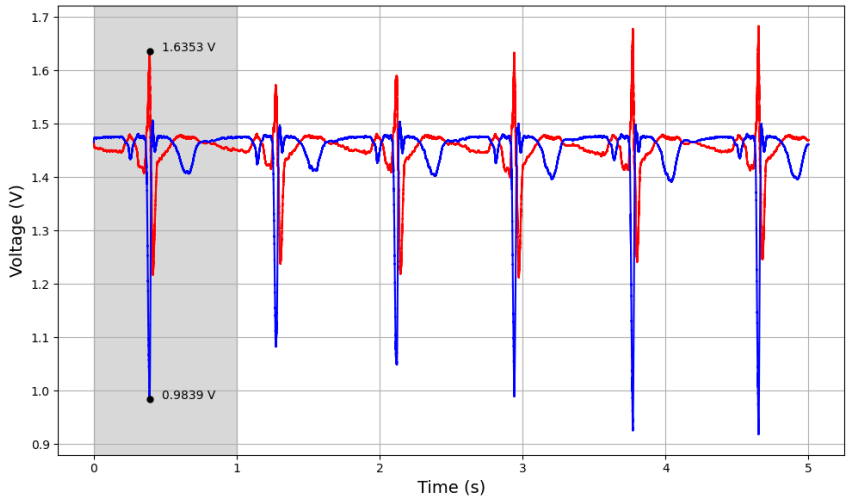


Figure 4.19: Simple Differential Amplifier Output f=5 kHz

The voltage difference between the outputs V_{0+} and V_{0-} has a value of 651 mV, which is 241 mV lower then the value observed with 1 kHz chopping. This can be explained by the slew rate, which is the maximum rate of change at the output voltage per unit time [30], which becomes critical at higher frequencies. As the chopping frequency increases, the amplifier may not have sufficient time to reach its full output swing before the modulation switches, resulting in a reduced output amplitude. This limitation likely accounts for the observed decrease in output voltage between 1 and 5 kHz chopping. To observe the signal integrity at this chopping frequency, Figure 4.20 presents the single-ended output response at 5 kHz.

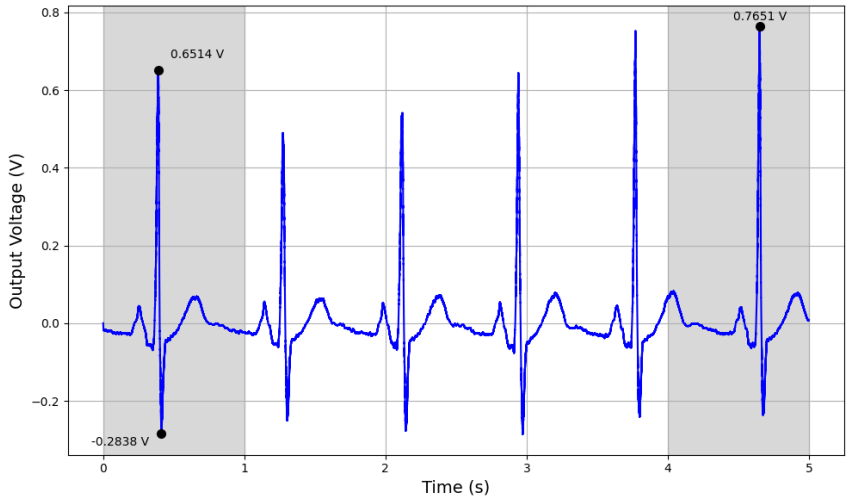


Figure 4.20: Single-Ended Output Simple Differential Amplifier f_{chop}=5 kHz

Although the amplification is lower, the system demonstrates a relatively good single integrity. It should be noted, however, that a ripple effect remains present at the output. The voltage difference corresponds to a gain of 52.20 dB, whilst the gain between the peaks in the first and last second, compared to the input, has a value of 55.10 dB.

4.4.2 Transconductance Boosting Differential Amplifier

Chopping at 1 kHz:

Applying a 1 kHz chopped ECG signal to the TBDA circuit, an amplification of 54.34 dB can be achieved, as indicated by the Bode plot in Figure 4.11. The transient response of the amplifier to this signal can be found in Figure 4.21.

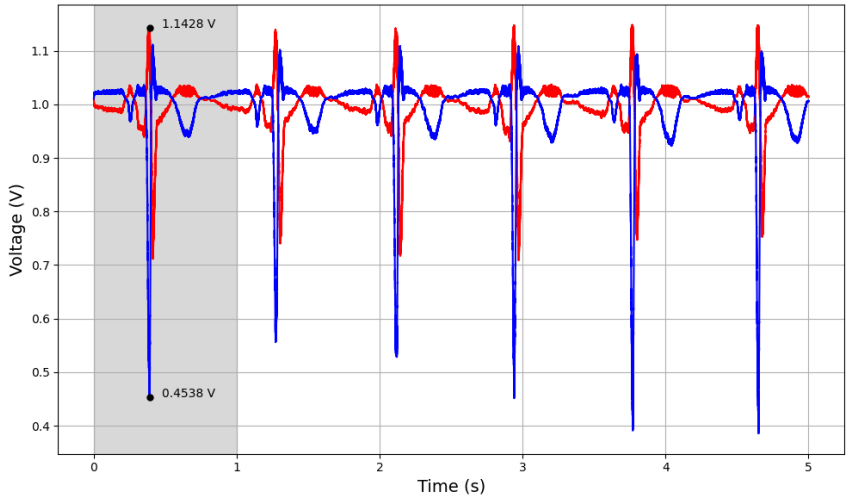


Figure 4.21: Transconductance Boosting Differential Amplifier Output f_{chop}=1 kHz

As shown in Figure 4.21, a peak-to-peak voltage of 689 mV is obtained. The linearity of the output is reduced due to a disparity in amplification between the upwards and downwards voltage swings. This behaviour could be explained by an incorrect common-mode voltage, which potentially drives certain transistors out of the saturation region. To determine if the linearity of the single-ended signal is effected, Figure 4.22 is used.

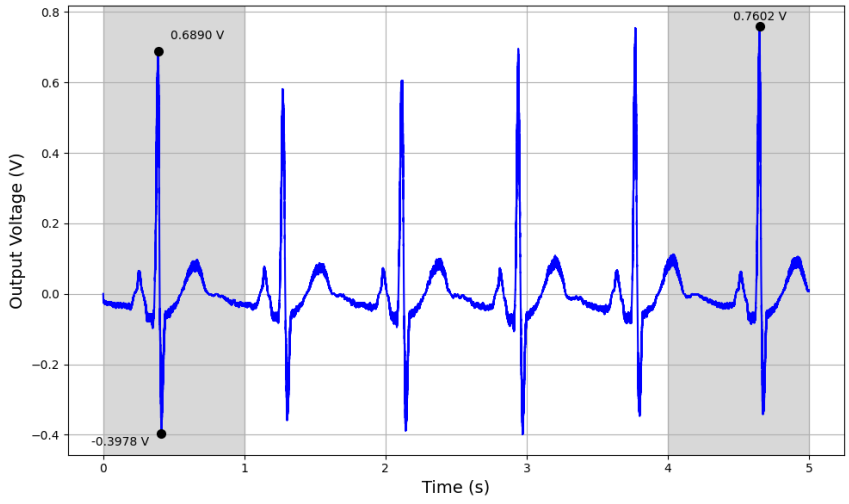


Figure 4.22: Single-Ended Output Transconductance Boosting Differential Amplifier f_{chop}=1 kHz

Although the ECG signal is present at the output, it is accompanied by an increased ripple element, which may lead to improper patient diagnosis. At a chopping frequency of 1 kHz, the figure reports a peak-to-peak voltage of 1.09 V, corresponding to an amplification of 53.5 dB relative to the reference shown in Figure 4.15. Furthermore, the gain calculated from the peak values observed during the first and last second, relative to the input, is 51.03 dB

Chopping at 5 kHz:

The Bode plot in Figure 4.11 reports a -3 dB point lower than 5 kHz, resulting in a decreased amplification at this frequency. The Transient response to a 5 kHz chopped input can be found in Figure 4.23.

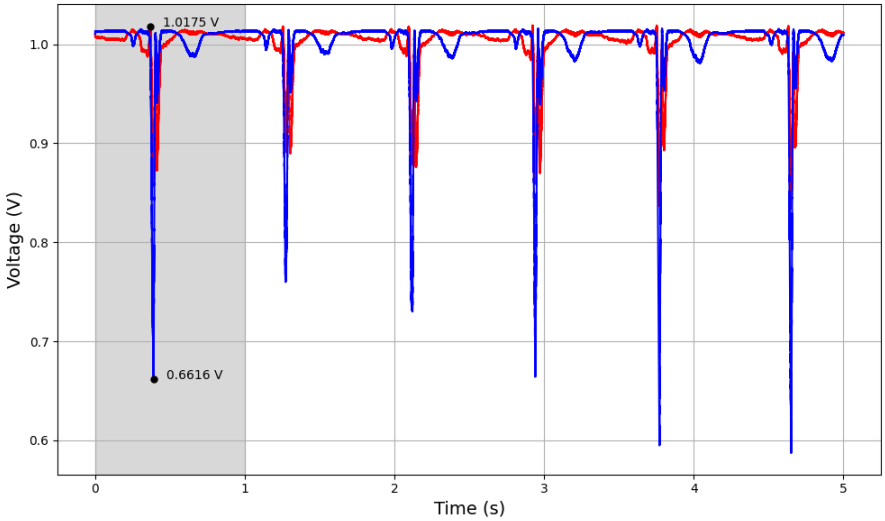


Figure 4.23: Transconductance Boosting Differential Amplifier Output f_{chop}=5 kHz

As previously discussed, the differential output shown in Figure 4.23 exhibits a reduced positive voltage swing compared to the negative swing. The simulated differential voltage is 356 mV, which is significantly lower than the value observed when a chopping frequency of 1 kHz is applied. The single-ended representation of the signal can be found in Figure 4.24.

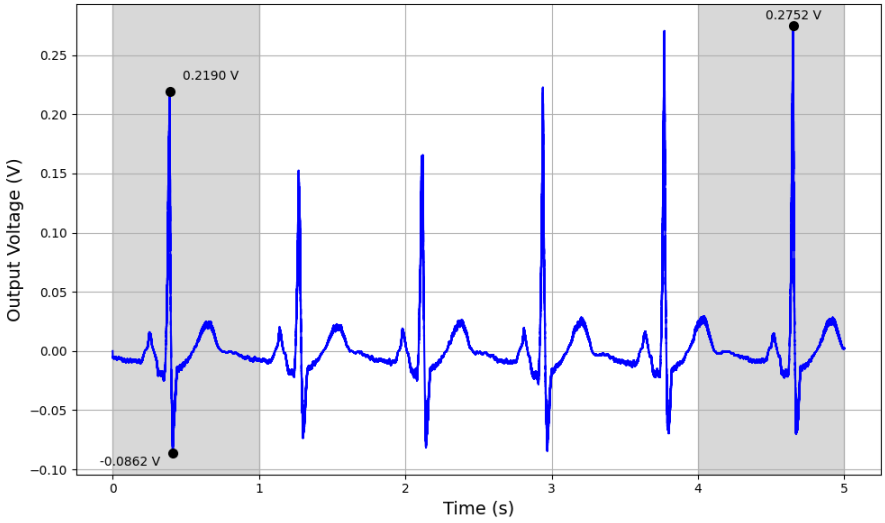


Figure 4.24: Single-ended Output Transconductance Boosting Differential Amplifier f_{chop}=5 kHz

At a chopping frequency of 5 kHz, the systems nonlinearity becomes more pronounced, resulting in a decrease of the signal integrity. The peak-to-peak voltage observed during the first second correspond to a gain of 42 dB. This value does not scale proportionally when compared to the difference between the maximum peak voltages in the first and last seconds of the simulation, which indicates a gain of 48.97 dB.

4.5 Conclusion

In this chapter, four differential amplifier topologies were evaluated. Among these, two demonstrated promising results for application in an AFE for ECG acquisition. These selected amplifiers were subsequently tested using an ECG signal, and their response was analysed.

The Simple Differential Amplifier (SDA), is stable enough and can be used with feedback, as illustrated in its Bode plot (Figure 4.4). The SDA has a maximum obtained gain of 52.31 dB, with a power consumption of 110.5 µW. The -3 dB point of the differential amplifier was reached at a frequency of 136 kHz, and the unity gain at 2.55 MHz. The CMRR has a value of 38.49 dB.

Afterwards, the SDA was subjected to a chopped ECG signal. Gains of 55.40 and 52.20 dB were observed for a chopping frequency of 1 and 5 kHz, respectively. To evaluate the linearity, the voltage difference between the positive peaks in the first and last seconds of the simulation were analysed. In a linear system, the gain calculated from this peak difference should match the gain derived from the peak-to-peak voltage. The simulated gains based on the positive peak difference were 55.81 and 55.10 dB for 1 and 5 kHz. These results suggest that the SDA exhibits more linear amplification at a chopping frequency of 1 kHz.

The Transconductance Boosting Differential Amplifier (TBDA) also demonstrated promising results, achieving a maximum gain of 54.34 dB. The system maintained stability with and without feedback, as illustrated in the Bode plot (Figure 4.11). The frequency where the gain drop with -3 dB is observed at 1 kHz, with the gain reaching 0 dB at approximately 425.27 kHz. These frequency characteristics are lower than those observed for the SDA. However, a notable advantage of the TBDA is its lower power consumption, simulated at 105.6 µW, and the increased CMRR.

When applying an ECG to the TBDA at chopping frequencies of 1 and 5 kHz, gains of 53.5 and 42 dB were observed, which are consistent with the expectations based on the Bode plot. In terms of linearity, the gain calculated from the difference between the positive peaks was 51.03 dB for 1 kHz and 48.97 dB for 5 kHz. These results indicate that the TBDA exhibits lower linearity compared to the SDA.

Although the SDA demonstrates an improved linearity and higher amplification over a wider frequency range, it consumes 4.4% more power then the TBDA, making it less suitable for low-power applications. Additionally, the TBDA exhibits a higher rejection against common-mode inputs. The comparison of these differential amplifiers with the state of the art, can be found in Table 4.5.

Table 4.5: Comparison with State-of-the-Art Designs

	this work		[65]			[44]	[66]	[67]	[68]	[58]	[69]
	SDA	**TBDA**	III.A	III.B	III.C						
Signal Type	ECG	ECG	ECG	ECG	ECG	EMG	N.A.	ECG	N.A.	N.A.	N.A.
Output Type	Fully-diff	Fully-diff	Fully-diff	Fully-diff	Fully-diff	Fully-diff	Single	Single	Single	Single	Single
Open Loop Gain (dB)	52.31	54.34	14	21.5	30	24.9 - 23.1	52	43.5	31.43	19	26.1
CMRR (dB)	38.49	57.15	N.A.	N.A.	N.A.	N.A.	N.A.	61.2	N.A.	N.A.	31.3
-3 dB (kHz)	290	1	2	0.4	0.150	5.2	± 1	2.1	9.33	25	8
UGBW (kHZ)	9210	489.88	4	2.5	5.5	N.A.	1190	290	180.2	330	89.1
PM (°)	90.29	70.12	N.A.	N.A.	N.A.	N.A.	64	58	-82	70	21
Amount of Stages	3	2	1	1	1	1	3	3	1	1	2
Supply Voltage (V)	3	3	± 10	± 10	± 10	± 13	3	15	15	6	10
Power (µW)	110.5	105.6	2.5	0.1	0.02	1300	186	200	5070	6780	960

Chapter 5

Conclusion and Discussion

5.1 Conclusion

This master's thesis investigated analogue circuits implemented using a-IGZO TFT technology, which demonstrates significant potential for application in flexible chips for ECG acquisition. To ensure effective implementation, a broader exploration of different amplifier topologies was undertaken. This research provided insight into the different suitable topologies and identified techniques that enable reliable amplification while minimizing noise contribution.

Afterwards, the different suitable topologies where designed and implemented in a feedback system. The transistor sizes where determined by the g_m/I_d method, which shows the correlation between the drain current, size and operation region of a transistor. For the diode-load differential amplifier and chopping circuits a layout was created.

The differential amplifiers were evaluated using a series of test benches to characterize their amplification, power consumption, single integrity, frequency, and square wave response. Among the examined topologies, the simple and transconductance boosting designs demonstrated the most promising performance, which were tested using an ECG test bench.

Based on these test results, it was concluded that the simple differential amplifier exhibited higher amplification over a broader frequency range, along with superior linearity. However, this performance comes at the cost of increased power consumption, which is approximately 4.4% higher than the transconductance boosting differential amplifier. Additionally, the transconductance boosting differential amplifier exhibits a higher common-mode rejection ratio.

The literature study indicated that a minimum amplification of 66 dB is required for compatibility with current ADCs implemented in a-IGZO technology. Although this target was not fully achieved in this master's thesis, the results represent an improvement over existing state-of-the-art designs.

5.2 Limitations of the Differential Amplifier and Potential Improvements

Due to the presence of a ripple effect at the the output of the differential amplifiers, a load capacitor was employed to mitigate its impact. However, implementing such a capacitor on a flexible chip poses significant challenges. A capacitor of the same size was used at the input of the differential amplifier, which presents a similar integration difficulty and additionally results in a reduction of the input impedance.

In future work, the systems presented in this study could be further evaluated using alternative feedback topologies aimed to increase input impedance. To address the ripple observed at the output, switched capacitor circuits or other filtering techniques could be employed. Since the ripple originates from the limited slew rate of the differential amplifier, exploring alternative amplifier topologies with improved slew rate performance could also prove beneficial.

5.3 Limitations of the Study and Future Work

To ensure reliable functionality in real-world implementation, the differential amplifiers could be subjected to Monte Carlo simulations to evaluate their performance under process and device variability. Successful results from these simulations would strengthen the case for further validation such as connecting the differential amplifier to a real-world ECG signal from a human subject.

Due to the unavailability of noise parameters for the used transistors, the noise performance of the system, particularly the effectiveness of the chopping technique, could not be evaluated. Future work could involve simulating noise contributions within the system to asses the impact of chopping and guide further optimization of the designs.

Acknowledgment

In this master's thesis, an OpenAI large language model was used to preform grammatical checks and improve text clarity, more preciously the GPT-4o model [70].

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Appendix A

Appendix - Layout Images

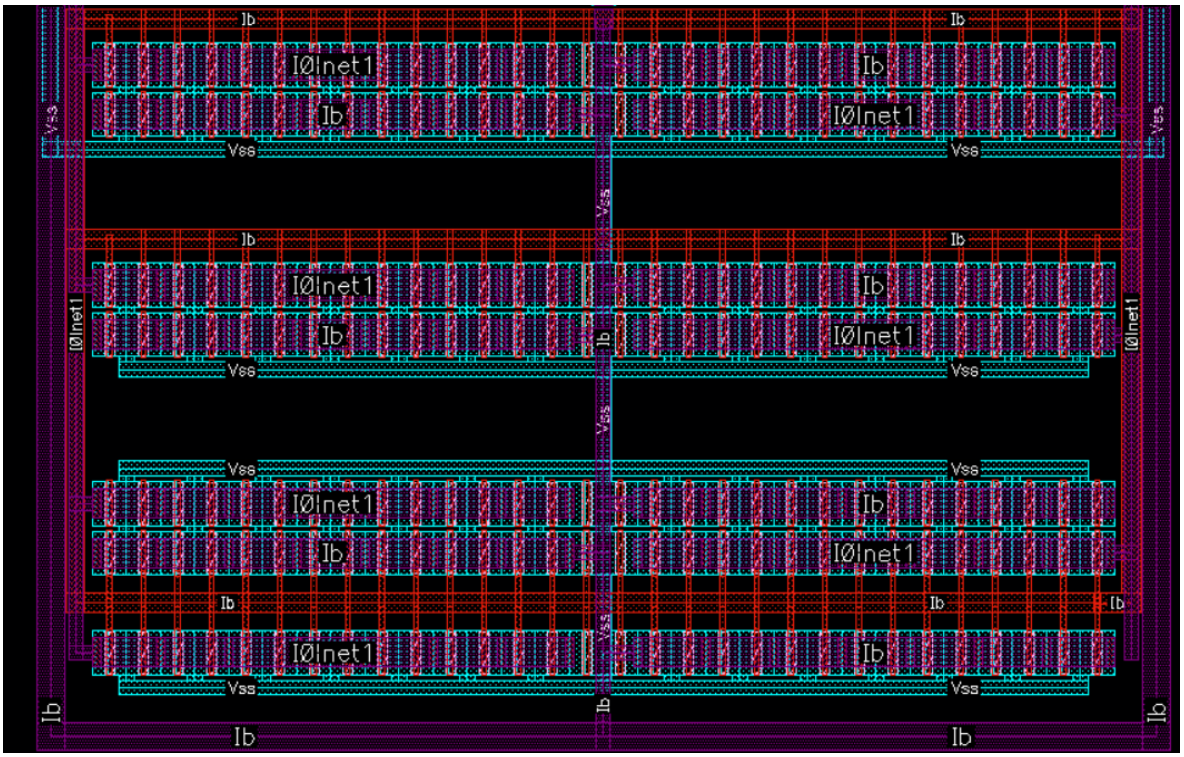


Figure A.1: Layout Current Mirror

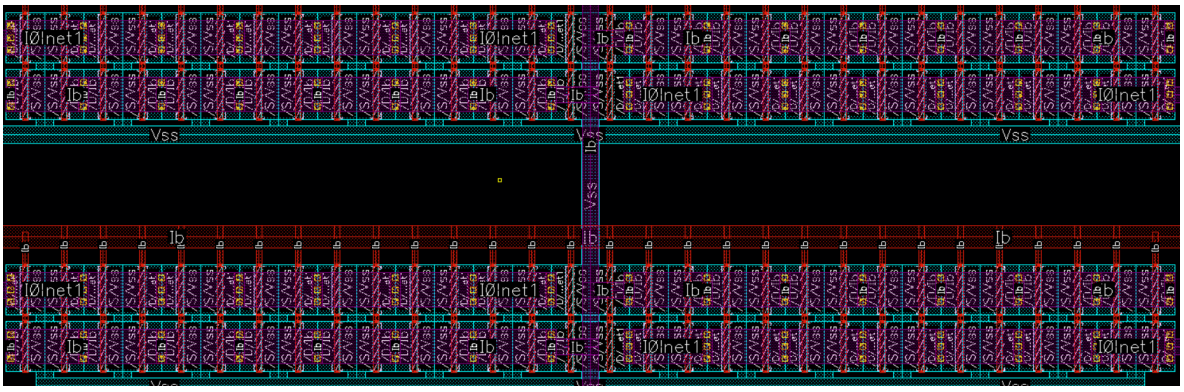


Figure A.2: Layout Current Mirror Magnified Transistor Stack

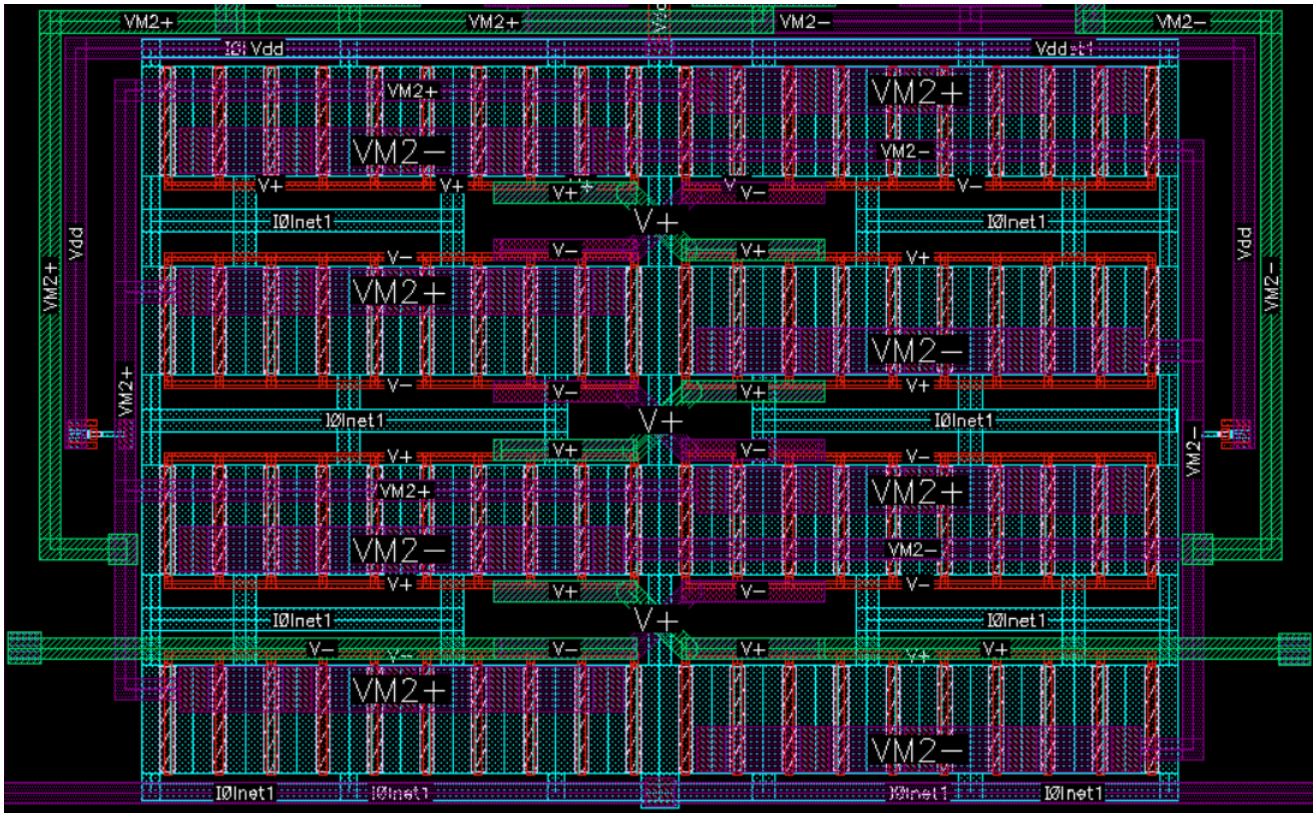


Figure A.3: Layout Differential Pair

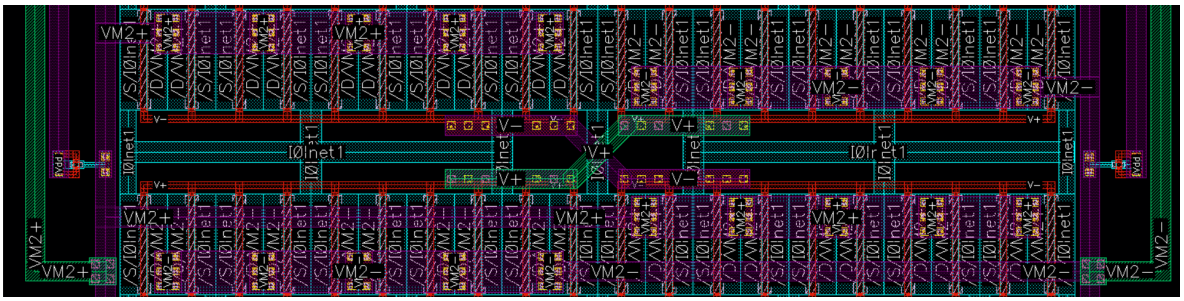


Figure A.4: Layout Differential Pair Magnified

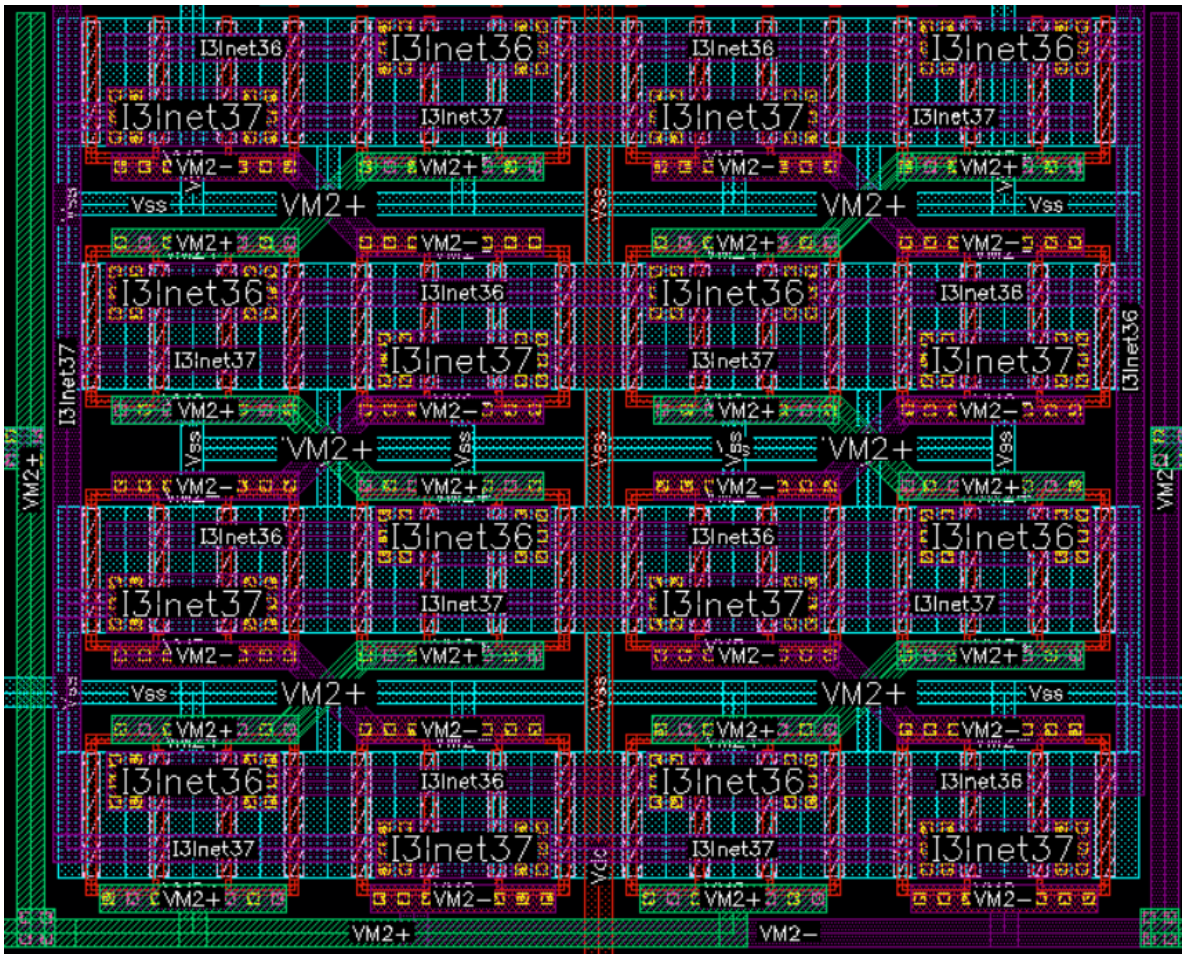


Figure A.5: Layout First Amplification Stage

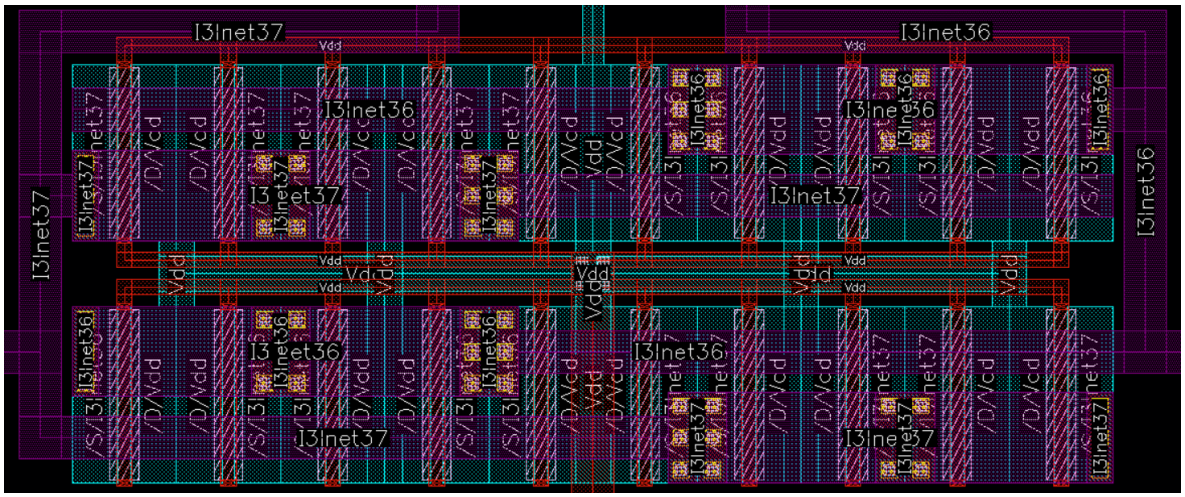


Figure A.6: Layout First Amplification Stage Diode-Connected Transistors

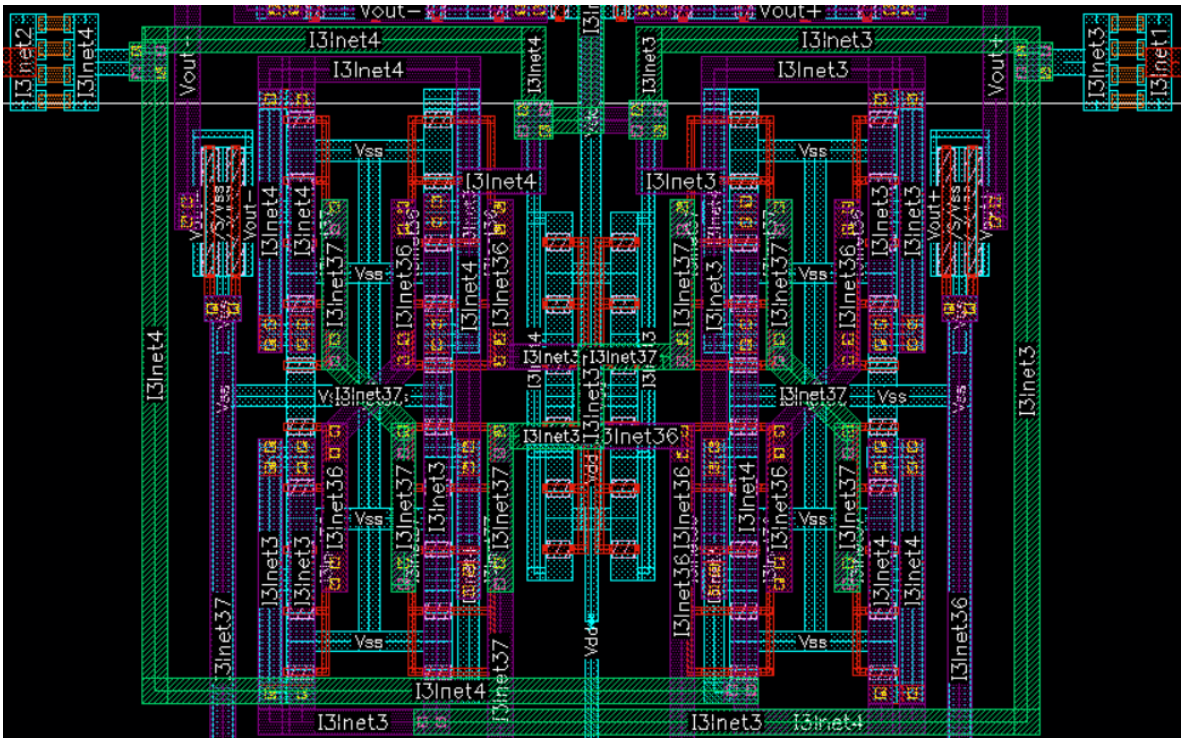


Figure A.7: Layout Last Amplification Stage

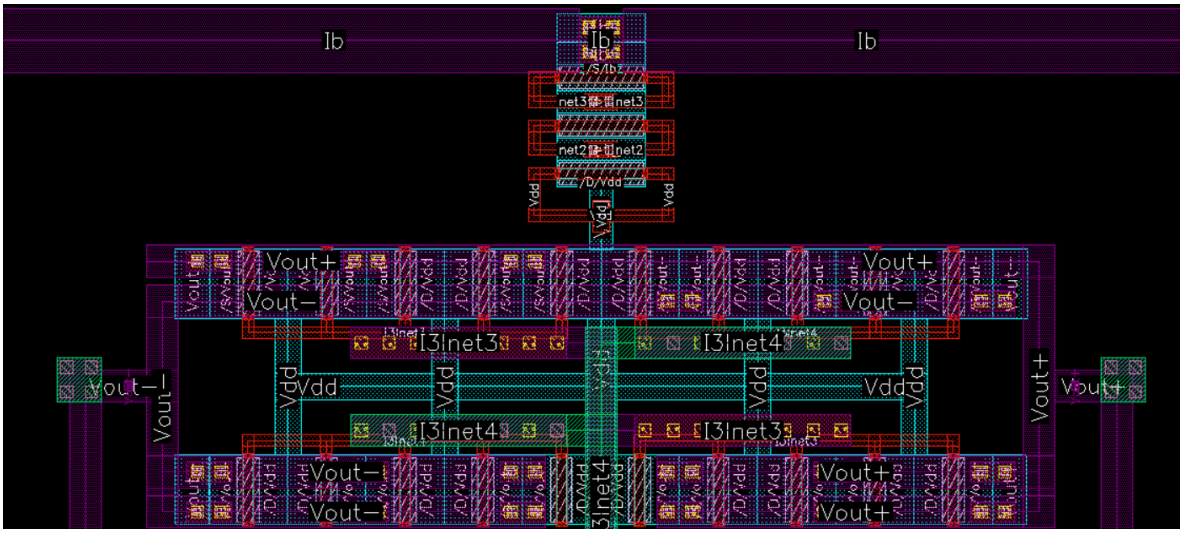


Figure A.8: Layout Bias Current Generation and Output Buffer

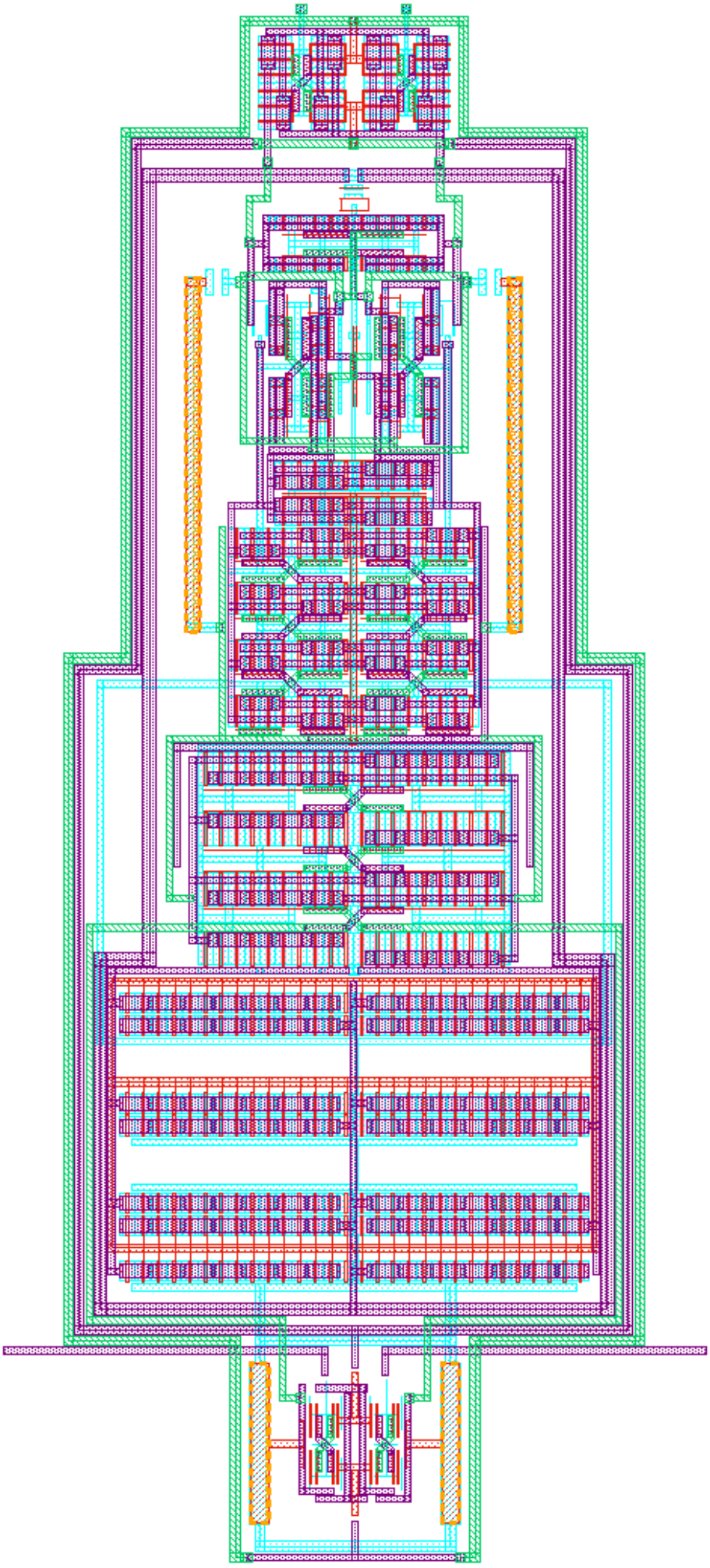
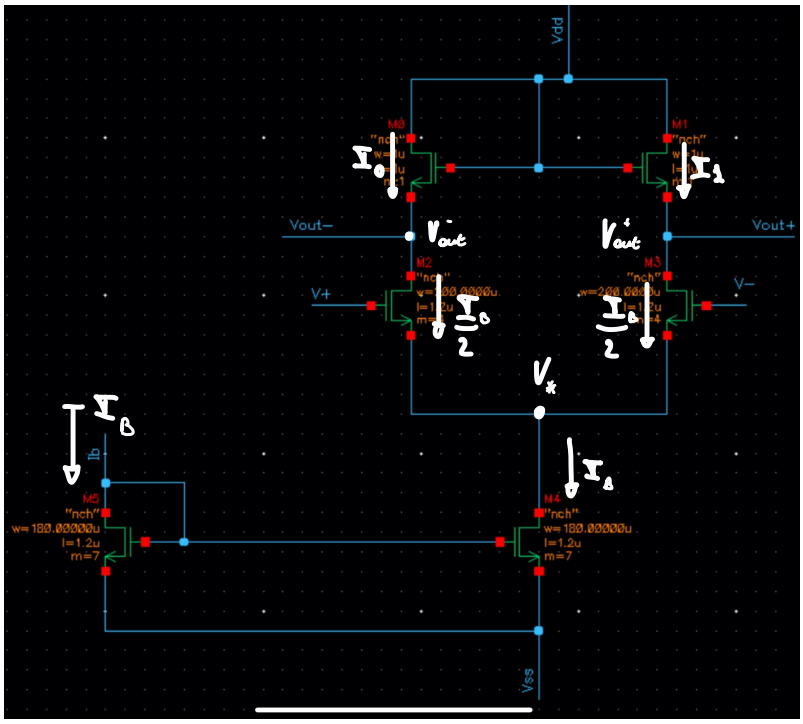


Figure A.9: Chopping Amplifier Layout

Appendix B

Appendix - Calculations



* M_4: no effect!

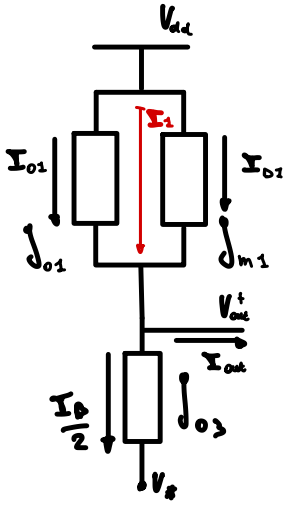
* M_2: $\frac{I_D}{2} = \frac{g_m}{2} \cdot (V_G - V_S)$

$\Rightarrow \frac{I_D}{2} = g_{m2} \cdot (V^+ - V_x)$

* M_3: $\frac{I_D}{2} = \frac{g_{m3}}{2} \cdot (V^- - V_x)$

* Gain $A = \frac{V_{out}^+ - V_{out}^-}{V_{in}^+ - V_{in}^-}$

* for V_{out}^+:



* $I_{D1} = \frac{g_{m1}}{2} \cdot (V_{dd} - V_{out}^+)$

* $I_{O1} = \Delta V \cdot g_{O1}$

$I_1 = I_{D1} + I_{O1}$

$= \frac{g_{m1}}{2} \cdot (V_{dd} - V_{out}^+) + g_{O1} (V_{dd} - V_{out}^+)$

* $g_{t1} = g_{O1} + g_{m1}$

* $g_{out} = g_{O3} + g_{O1} + g_{m1}$

$\rightarrow r_1 // r_3$

$\rightarrow V_{out}^+ = \frac{I_{out}}{g_{out}} = \frac{I_1 - \frac{I_D}{2}}{g_{out}}$

$g = \frac{I}{V} \Rightarrow V = \frac{I}{g}$

$$V_{out}^+ = \frac{\frac{g_{m1}}{2} \cdot (V_{dd} - V_{out}^+) + g_{O1} (V_{dd} - V_{out}^+) - g_{m3} \cdot (V^- - V_x)}{g_{O3} + g_{O1} + g_{m1}}$$

$$\Rightarrow V_{out}^+ + \frac{\frac{g_{m1}}{2} \cdot V_{out}^+ + g_{O1} \cdot V_{out}^+}{g_{O3} + g_{O1} + g_{m1}} = \frac{\frac{g_{m1}}{2} \cdot V_{dd} + g_{O1} \cdot V_{dd} - g_{m3} \cdot (V^- - V_x)}{g_{O3} + g_{O1} + g_{m1}}$$

$$\Rightarrow V_{out}^+ \left(1 + \frac{\frac{g_{m1}}{2} + g_{O1}}{g_{O3} + g_{O1} + g_{m1}} \right) = \frac{\frac{g_{m1}}{2} \cdot V_{dd} + g_{O1} \cdot V_{dd} - g_{m3} \cdot (V^- - V_x)}{g_{O3} + g_{O1} + g_{m1}}$$

$$\Rightarrow \quad V_{out}^{+} = \frac{\frac{g_{m1}}{2} \cdot V_{dd} + g_{o1} \cdot V_{dd} - g_{m3} \cdot (V^{-} - V_x)}{g_{o3} + g_{o2} + g_{m1}} \cdot \frac{1}{\left(1 + \frac{\frac{g_{m1}}{2} + g_{o1}}{g_{o3} + g_{o2} + g_{m1}}\right)}$$

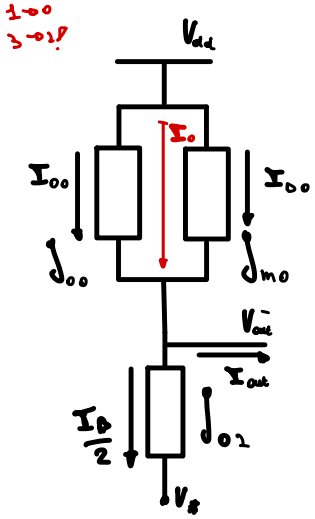
$$\frac{1}{\frac{g_{o3} + g_{o2} + g_{m1} + \frac{g_{m1}}{2} + g_{o1}}{g_{o3} + g_{o2} + g_{m1}}} = \frac{g_{o3} + g_{o2} + g_{m1}}{g_{o3} + g_{o2} + g_{m1} + \frac{g_{m1}}{2} + g_{o1}}$$

$$\Rightarrow \quad V_{out}^{+} = \frac{\frac{g_{m1}}{2} \cdot V_{dd} + g_{o1} \cdot V_{dd} - g_{m3} \cdot (V^{-} - V_x)}{\cancel{g_{o3} + g_{o2} + g_{m1}}} \cdot \frac{\cancel{g_{o3} + g_{o2} + g_{m1}}}{g_{o3} + g_{o2} + g_{m1} + \frac{g_{m1}}{2} + g_{o1}}$$

0V → AC GND

$$\Rightarrow \quad V_{out}^{+} = \frac{\frac{g_{m1}}{2} \cdot V_{dd} + g_{o1} \cdot V_{dd} - g_{m3} \cdot (V^{-} - V_x)}{g_{o3} + g_{o2} + g_{m1} + \frac{g_{m1}}{2} + g_{o1}} = \frac{\frac{g_{m1}}{2} \cdot V_{dd} + g_{o1} \cdot V_{dd} - g_{m3} \cdot (V^{-} - V_x)}{g_{o3} + 2 \cdot g_{o2} + \frac{3}{2} \cdot g_{m1}}$$

* for V_{out}^{-} :



* $I_{D0} = \frac{g_{m0}}{2} \cdot |V_{dd} - V_{out}^{+}|$

* $I_{oo} = \Delta V \cdot g_{oo}$

$\Big\} \; I_o = I_{D0} + I_{oo} = \frac{g_{m0}}{2} \cdot (V_{dd} - V_{out}^{+}) + g_{oo}(V_{dd} - V_{out}^{+})$

* $g_{to} = g_{oo} + g_{m0}$

* $g_{out} = g_{o2} + g_{oo} + g_{m0}$

* $V_{out}^{-} = \frac{\frac{g_{m0}}{2} \cdot V_{dd} + g_{oo} \cdot V_{dd} - g_{m2} \cdot (V^{+} - V_x)}{g_{o2} + 2 \cdot g_{oo} + \frac{3}{2} \cdot g_{m0}}$

* together ⟶ assume remety : $g_{m1} \; i \; g_{m3}$

↳ $g_{m1} = g_{m3}$ i $g_{m0} = g_{m1}$; $g_{oo} = g_{o1}$ i $g_{o2} = g_{o3}$

→ $A = \frac{V_{out}^{+} - V_{out}^{-}}{V^{+} - V^{-}}$

$$\Rightarrow V_{out}^{+} - V_{out}^{-} = \frac{\frac{g_{m1}}{2} \cdot V_{dd} + g_{o1} \cdot V_{dd} - g_{m3} \cdot (V^{-} - V_x)}{g_{o3} + 2 \cdot g_{o2} + \frac{3}{2} \cdot g_{m1}} - \frac{\frac{g_{m0}}{2} \cdot V_{dd} + g_{o0} \cdot V_{dd} - g_{m2} \cdot (V^{+} - V_x)}{g_{o2} + 2 \cdot g_{o0} + \frac{3}{2} \cdot g_{m0}}$$

$$= \frac{\frac{g_{m1}}{2} \cdot V_{dd} + g_{o1} \cdot V_{dd} - g_{m3} \cdot (V^{-} - V_x)}{g_{o3} + 2 \cdot g_{o2} + \frac{3}{2} \cdot g_{m1}} - \frac{\frac{g_{m0}}{2} \cdot V_{dd} + g_{o0} \cdot V_{dd} - g_{m2} \cdot (V^{+} - V_x)}{g_{o2} + 2 \cdot g_{o0} + \frac{3}{2} \cdot g_{m0}} \cdot \frac{g_{o2} + 2 \cdot g_{o0} + \frac{3}{2} \cdot g_{m0}}{g_{o3} + 2 \cdot g_{o2} + \frac{3}{2} \cdot g_{m1}}$$

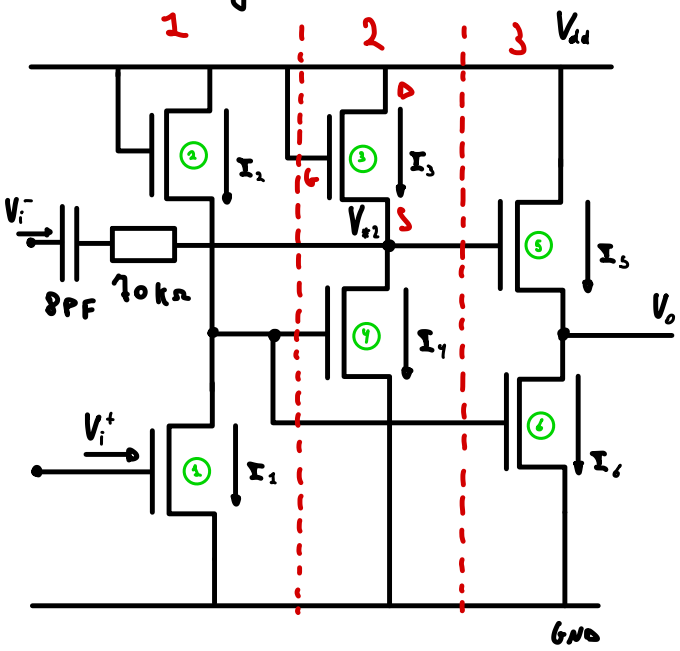
$$= \frac{\frac{g_{m1}}{2} \cdot V_{dd} + g_{o1} \cdot V_{dd} - g_{m3} \cdot (V^{-} - V_x) - \left(\frac{g_{m1}}{2} \cdot V_{dd} + g_{o1} \cdot V_{dd} - g_{m3} \cdot (V^{+} - V_x) \right)}{g_{o3} + 2 \cdot g_{o2} + \frac{3}{2} \cdot g_{m1}}$$

$V_x \approx 0V$

$$= \frac{-g_{m3} \cdot V^{-} + g_{m3} \cdot V^{+}}{g_{o3} + 2 \cdot g_{o2} + \frac{3}{2} \cdot g_{m1}} = \frac{g_{m3} \cdot (V^{+} - V^{-})}{g_{o3} + 2 \cdot g_{o2} + \frac{3}{2} \cdot g_{m1}}$$

$$\Rightarrow A = \frac{g_{m3}}{g_{o3} + 2 \cdot g_{o2} + \frac{3}{2} \cdot g_{m1}} = \frac{2 \cdot g_{m3}}{2 \cdot g_{o3} + 4 \cdot g_{o2} + 3 \cdot g_{m1}}$$

* second stage:



$$*1: \quad I_1 = \frac{g_{m1}}{2} \cdot (V_G - V_S)$$

$$\Rightarrow I_1 = \frac{g_{m1}}{2} \cdot (V_i - 0V) = \frac{g_{m1}}{2} \cdot V_i$$

$$I_1 = \frac{g_{m1}}{2} \cdot (V_{dd} - V_*) + g_{o2} \cdot (V_{dd} - V_*)$$

$$\rightarrow V_* = \frac{(I_2 - I_1)}{g_t}$$

$$\rightarrow g_t = g_{o2} + g_{m2} + g_{o1}$$

$$\Rightarrow V_* = \frac{-\frac{g_{m1}}{2} \cdot V_i + \frac{g_{m1}}{2} \cdot (V_{dd} - V_*) + g_{o2} \cdot (V_{dd} - V_*)}{g_{o2} + g_{m2} + g_{o1}}$$

$$\Rightarrow \quad V_* = \frac{-\frac{g_{m1}}{2} \cdot V_i + (\frac{g_{m1}}{2} V_{dd} - \frac{g_{m1}}{2} V_*) + (g_{o2} V_{dd} - g_{o2} \cdot V_*)}{g_{o2} + g_{m2} + g_{o1}}$$

$$= \frac{-\frac{g_{m1}}{2} \cdot V_i + \frac{g_{m1}}{2} V_{dd} + g_{o2} V_{dd}}{g_{o2} + g_{m2} + g_{o1}} - \frac{\frac{g_{m1}}{2} V_* - g_{o2} \cdot V_*}{g_{o2} + g_{m2} + g_{o1}}$$

$$\Rightarrow \left(1 + \frac{\frac{g_{m1}}{2} - g_{o2}}{g_{o2} + g_{m2} + g_{o1}}\right) \cdot V_* = \frac{-\frac{g_{m1}}{2} \cdot V_i + \frac{g_{m1}}{2} V_{dd} + g_{o2} V_{dd}}{g_{o2} + g_{m2} + g_{o1}}$$

$$\frac{1}{\left(1 + \frac{\frac{g_{m1}}{2} - g_{o2}}{g_{o2} + g_{m2} + g_{o1}}\right)} = \frac{g_{o2} + g_{m2} + g_{o1}}{\cancel{g_{o2}} + g_{m2} + g_{o1} + \frac{g_{m1}}{2} - \cancel{g_{o2}}}$$

$$= \frac{g_{o2} + g_{m2} + g_{o1}}{g_{m2} + g_{o1} + \frac{g_{m1}}{2}} = \frac{g_{o2} + g_{m2} + g_{o1}}{g_{o1} + \frac{1 \cdot g_{m1}}{2}}$$

$$\Rightarrow V_{\#} = \frac{-\frac{g_{m1}}{2}\cdot V_i + \frac{g_{m2}}{2}V_{dd} + g_{o2}V_{dd}}{g_{o1}+g_{m2}+g_{o2}} \cdot \frac{g_{o1}+g_{m2}+g_{o2}}{g_{o2}+\frac{3\cdot g_{m2}}{2}}$$

$$= \frac{-\frac{g_{m1}}{2}\cdot V_i + \frac{g_{m2}}{2}V_{dd} + g_{o2}V_{dd}}{g_{o2}+\frac{3\cdot g_{m2}}{2}}$$

*2:

$$\rightarrow I_3 = \frac{g_{m3}}{2}\cdot(V_G - V_S) + g_{o3}\cdot(V_G - V_S) = \frac{g_{m3}}{2}\cdot(V_{dd} - V_{\#2}) + g_{o3}\cdot(V_{dd} - V_{\#2})$$

$$\rightarrow I_4 = \frac{g_{m4}}{2}\cdot(V_{\#} - 0V)$$

$$V_{\#2} = \frac{I_3 - I_4}{g_{o3}+g_{m4}+g_{o4}} = \frac{\frac{g_{m3}}{2}\cdot(V_{dd} - V_{\#2}) + g_{o3}\cdot(V_{dd} - V_{\#2}) - \frac{g_{m4}}{2}\cdot V_{\#}}{g_{o3}+g_{m4}+g_{o4}}$$

$$= \frac{\frac{g_{m3}}{2}\cdot V_{dd} - \frac{g_{m3}}{2}V_{\#2} + g_{o3}V_{dd} - g_{o3}V_{\#2} - \frac{g_{m4}}{2}\cdot V_{\#}}{g_{o3}+g_{m4}+g_{o4}}$$

$$= \frac{\frac{g_{m3}}{2}\cdot V_{dd} + g_{o3}V_{dd} - \frac{g_{m4}}{2}\cdot V_{\#}}{g_{o3}+g_{m4}+g_{o4}} - \frac{\frac{g_{m3}}{2}V_{\#2} - g_{o3}V_{\#2}}{g_{o3}+g_{m4}+g_{o4}}$$

$$\Rightarrow \left(1 + \frac{\frac{g_{m3}}{2} - g_{o3}}{g_{o3}+g_{m4}+g_{o4}}\right)\cdot V_{\#2} = \frac{\frac{g_{m3}}{2}\cdot V_{dd} + g_{o3}V_{dd} - \frac{g_{m4}}{2}\cdot V_{\#}}{g_{o3}+g_{m4}+g_{o4}}$$

$$\frac{g_{o3}+g_{m4}+g_{o4}}{g_{o3}+g_{m4}+g_{o4}+\frac{g_{m3}}{2}-g_{o3}} = \frac{g_{o3}+g_{m4}+g_{o4}}{g_{o4}+\frac{3\,g_{m3}}{2}}$$

$$\Rightarrow V_{\#2} = \frac{\frac{g_{m3}}{2}\cdot V_{dd} + g_{o3}V_{dd} - \frac{g_{m4}}{2}\cdot V_{\#}}{g_{o3}+g_{m4}+g_{o4}} \cdot \frac{g_{o3}+g_{m4}+g_{o4}}{g_{o4}+\frac{3\,g_{m3}}{2}}$$

$$= \frac{\frac{g_{m3}}{2} \cdot V_{dd} + g_{o3} V_{dd} - \frac{g_{m4}}{2} \cdot V_*}{g_{o4} + \frac{3 g_{m3}}{2}}$$

*3

$$V_0 = \frac{I_5 - I_6}{g_{out}}$$

$$g_{out} = g_{o5} + g_{o6} + g_{m5}$$

$$\rightarrow I_{D5} = \frac{g_{m5}}{2} \cdot (V_G - V_S) + g_{o5} \cdot (V_G - V_S) = \frac{g_{m5}}{2} \cdot (V_{B2} - V_0) + g_{o5} \cdot (V_{B2} - V_0)$$

$$\rightarrow I_{D6} = \frac{g_{m6}}{2} \cdot (V_G - V_S) = \frac{g_{m6}}{2} \cdot (V_* - 0V)$$

$$\Rightarrow V_0 = \frac{\frac{g_{m5}}{2} \cdot (V_{B2} - V_0) + g_{o5} \cdot (V_{B2} - V_0) - \frac{g_{m6}}{2} \cdot (V_*)}{g_{o5} + g_{o6} + g_{m5}}$$

$$= \frac{\frac{g_{m5}}{2} \cdot V_{B2} - V_0 \cdot \frac{g_{m5}}{2} + g_{o5} \cdot V_{B2} - V_0 \cdot g_{o5} - \frac{g_{m6}}{2} \cdot V_*}{g_{o5} + g_{o6} + g_{m5}}$$

$$= \frac{\frac{g_{m5}}{2} \cdot V_{B2} + g_{o5} \cdot V_{B2} - \frac{g_{m6}}{2} \cdot V_*}{g_{o5} + g_{o6} + g_{m5}} - \frac{V_0 \cdot \frac{g_{m5}}{2} - V_0 \cdot g_{o5}}{g_{o5} + g_{o6} + g_{m5}}$$

$$\Rightarrow \left(2 + \frac{\frac{g_{m5}}{2} - g_{o5}}{g_{o5} + g_{o6} + g_{m5}}\right) \cdot V_0 = \frac{\frac{g_{m5}}{2} \cdot V_{B2} + g_{o5} \cdot V_{B2} - \frac{g_{m6}}{2} \cdot V_*}{g_{o5} + g_{o6} + g_{m5}}$$

$$\frac{g_{o5} + g_{o6} + g_{m5}}{\frac{g_{m5}}{2} - g_{o5} + g_{o5} + g_{o6} + g_{m5}}$$

$$V_0 = \frac{\frac{g_{m5}}{2} \cdot V_{B2} + g_{o5} \cdot V_{B2} - \frac{g_{m6}}{2} \cdot V_*}{g_{o5} + g_{o6} + g_{m5}} \cdot \frac{g_{o5} + g_{o6} + g_{m5}}{\frac{g_{m5}}{2} + g_{o6} + g_{m5}}$$

$$V_O = \frac{\frac{g_{m3}}{2}\cdot V_{s1} + g_{o3}\cdot V_{s1} - \frac{g_{m6}}{2}\cdot V_{*}}{\frac{g_{m3}}{2} + g_{o6} + g_{m5}} \quad \begin{matrix} \rightarrow A_2 V_{*} \rightarrow A_2 \cdot A_1 \cdot V_{in} \\ \rightarrow A_1 \cdot V_{in} \end{matrix}$$

* A_1:

$$V_{*A} - V_{*B} = \frac{-\frac{g_{m1}}{2}\cdot V_{iA} + \frac{g_{m1}}{2}V_{dd} + g_{o2}V_{dd}}{g_{o1} + \frac{J\cdot g_{m1}}{2}} - \left(\frac{-\frac{g_{m1}}{2}\cdot V_{iB} + \frac{g_{m1}}{2}V_{dd} + g_{o2}V_{dd}}{g_{o1} + \frac{J\cdot g_{m1}}{2}}\right)$$

$$\Rightarrow V_{*A} - V_{*B} = \frac{-\frac{g_{m1}}{2}\cdot V_{iA} + \cancel{\frac{g_{m1}}{2}V_{dd}} + \cancel{g_{o2}V_{dd}}}{g_{o1} + \frac{J\cdot g_{m1}}{2}} + \left(\frac{+\frac{g_{m1}}{2}\cdot V_{iB} - \cancel{\frac{g_{m1}}{2}V_{dd}} - \cancel{g_{o2}V_{dd}}}{g_{o1} + \frac{J\cdot g_{m1}}{2}}\right)$$

$$\Rightarrow V_{*A} - V_{*B} = \frac{\frac{g_{m1}}{2}\cdot V_{iB} - \frac{g_{m1}}{2}\cdot V_{iA}}{g_{o1} + \frac{J\cdot g_{m1}}{2}} = \frac{\frac{g_{m1}}{2}\cdot (V_{iB} - V_{iA})}{g_{o1} + \frac{J\cdot g_{m1}}{2}} = -\frac{\frac{g_{m1}}{2}\cdot (V_{iA} - V_{iB})}{g_{o1} + \frac{J\cdot g_{m1}}{2}}$$

$$\Rightarrow \frac{V_{*A} - V_{*B}}{V_{iA} - V_{iB}} = -\frac{\frac{g_{m1}}{2}}{g_{o1} + \frac{J\cdot g_{m1}}{2}} = -\frac{\cancel{\frac{g_{m1}}{2}}}{\cancel{\frac{1}{2}}(2\cdot g_{o1} + J\cdot g_{m1})} = -\frac{g_{m1}}{2\cdot g_{o1} + J\cdot g_{m1}}$$

* A_2:

$$A_2 = -\frac{g_{m3}}{2\cdot g_{o3} + J\cdot g_{m4}}$$

$$V_O = \frac{\frac{g_{m3}}{2}\cdot V_{s1} + g_{o3}\cdot V_{s1} - \frac{g_{m6}}{2}\cdot V_{*}}{\frac{g_{m3}}{2} + g_{o6} + g_{m5}} \quad \begin{matrix} \rightarrow A_2 V_{*} \rightarrow A_2 \cdot A_1 \cdot V_{in} \\ \rightarrow A_1 \cdot V_{in} \end{matrix}$$

$$= \frac{\frac{g_{m3}}{2}\cdot A_2 + g_{o3}\cdot A_2 - \frac{g_{m6}}{2}}{\frac{g_{m3}}{2} + g_{o6} + g_{m5}} \cdot A_1 V_{in}$$

$$\Rightarrow V_{A,o} - V_{B,o} = \frac{\frac{g_{m3}}{2}\cdot A_2 + g_{o3}\cdot A_2 - \frac{g_{m6}}{2}}{\frac{g_{m3}}{2} + g_{o6} + g_{m5}} \cdot A_1 \cdot V_{in,A} - \frac{\frac{g_{m3}}{2}\cdot A_2 + g_{o3}\cdot A_2 - \frac{g_{m6}}{2}}{\frac{g_{m3}}{2} + g_{o6} + g_{m5}} \cdot A_1 \cdot V_{in,B}$$

$$= \frac{\frac{g_{m3}}{2}\cdot A_2 + g_{o3}\cdot A_2 - \frac{g_{m6}}{2}}{\frac{g_{m3}}{2} + g_{o6} + g_{m5}} \cdot A_1 \cdot (V_{in,A} - V_{in,B})$$

$$\Rightarrow \frac{V_{A,o} - V_{B,o}}{(V_{inA} - V_{inB})} = \frac{\frac{g_{m3}}{2} \cdot A_2 + g_{o3} \cdot A_2 - \frac{g_{m6}}{2}}{\frac{g_{m3}}{2} + g_{o6} + g_{ms}} \cdot A_1$$

$$= \frac{g_{m3} \cdot A_2 + 2 \cdot g_{o3} \cdot A_2 - g_{m6}}{g_{m3} + 2 \cdot g_{o6} + 2 \cdot g_{ms}} \cdot \left(- \frac{g_{m1}}{2 \cdot g_{o1} + 3 \cdot g_{m1}} \right)$$

$$= - \frac{g_{m3} \cdot \frac{g_{m3}}{2 \cdot g_{o3} + 3 \cdot g_{m4}} + 2 \cdot g_{o3} \cdot \frac{g_{m3}}{2 \cdot g_{o3} + 3 \cdot g_{m4}} + g_{m6}}{g_{m3} + 2 \cdot g_{o6} + 2 \cdot g_{ms}} \cdot \left(- \frac{g_{m1}}{2 \cdot g_{o1} + 3 \cdot g_{m1}} \right)$$

$$= \left(\underbrace{\frac{g_{m3} \cdot g_{m3}}{(2 \cdot g_{o3} + 3 \cdot g_{m4})(g_{m3} + 2 \cdot g_{o6} + 2 \cdot g_{ms})}}_{(2)} + \frac{2 \cdot g_{o3} \, g_{m3}}{(2 \cdot g_{o3} + 3 \cdot g_{m4})(g_{m3} + 2 \cdot g_{o6} + 2 \cdot g_{ms})} + \underbrace{\frac{g_{m6}}{g_{m3} + 2 \cdot g_{o6} + 2 \cdot g_{ms}}}_{(1)} \right) \cdot \frac{g_{m1}}{2 \cdot g_{o1} + 3 \cdot g_{m1}}$$

(1) →
$$\frac{\frac{g_{m3} \cdot g_{m3}}{2 \cdot g_{o3} + 3 \cdot g_{m4}} + \frac{2 \cdot g_{o3} \, g_{m3}}{2 \cdot g_{o3} + 3 \cdot g_{m4}}}{g_{m3} + 2 \cdot g_{o6} + 2 \cdot g_{ms}} = \frac{\frac{g_{m3}(g_{m3} + 2 \cdot g_{o3})}{2 \cdot g_{o3} + 3 \cdot g_{m4}}}{2 \cdot g_{o6} + 3 \cdot g_{ms}}$$

$$\Rightarrow \underbrace{\frac{V_{A,o} - V_{B,o}}{(V_{inA} - V_{inB})}}_{A_\epsilon} = \left(\frac{\frac{g_{m3}(g_{m3} + 2 \cdot g_{o3})}{2 \cdot g_{o3} + 3 \cdot g_{m4}}}{2 \cdot g_{o6} + 3 \cdot g_{ms}} + \frac{g_{m6}}{2 \cdot g_{o6} + 3 \cdot g_{ms}} \right) \cdot \frac{g_{m1}}{2 \cdot g_{o1} + 3 \cdot g_{m1}}$$

$$\Rightarrow A_\epsilon = \frac{\frac{g_{m3}(g_{m3} + 2 \cdot g_{o3})}{2 \cdot g_{o3} + 3 \cdot g_{m4}} + g_{m6}}{2 \cdot g_{o6} + 3 \cdot g_{ms}} \cdot \frac{g_{m1}}{2 \cdot g_{o1} + 3 \cdot g_{m1}}$$

$$= \frac{\frac{\gamma_{m3}\left(\beta_{m3} + 2\cdot\beta_{o3}\right) + \beta_{m6}\left(2\cdot\beta_{o3} + 3\cdot\beta_{m4}\right)}{2\cdot\beta_{o3} + 3\cdot\beta_{m4}}}{\frac{2\cdot\beta_{o6} + 3\cdot\beta_{m5}}{1}} \cdot \frac{\gamma_{m2}}{2\cdot\beta_{o2} + 3\cdot\beta_{m2}}$$

$$= \frac{\gamma_{m3}\left(\beta_{m3} + 2\cdot\beta_{o3}\right) + \beta_{m6}\left(2\cdot\beta_{o3} + 3\cdot\beta_{m4}\right)}{2\cdot\beta_{o3} + 3\cdot\beta_{m4}} \cdot \frac{1}{2\cdot\beta_{o6} + 3\cdot\beta_{m5}} \cdot \frac{\gamma_{m2}}{2\cdot\beta_{o2} + 3\cdot\beta_{m2}}$$

$$= \frac{\left(\gamma_{m3}\left(\beta_{m3} + 2\cdot\beta_{o3}\right) + \beta_{m6}\left(2\cdot\beta_{o3} + 3\cdot\beta_{m4}\right)\right)\cdot\gamma_{m2}}{\left(2\cdot\beta_{o3} + 3\cdot\beta_{m4}\right)\cdot\left(2\cdot\beta_{o6} + 3\cdot\beta_{m5}\right)\cdot\left(2\cdot\beta_{o2} + 3\cdot\beta_{m2}\right)}$$

Appendix C

Appendix - Bode Plot CMRR

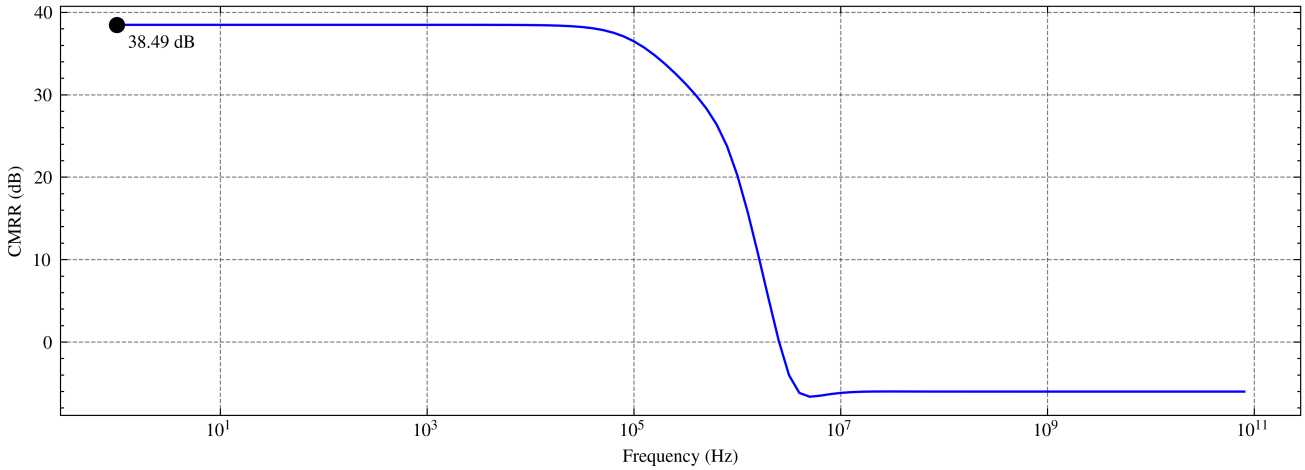


Figure C.1: CMRR Simple Differential Amplifier Closed-Loop

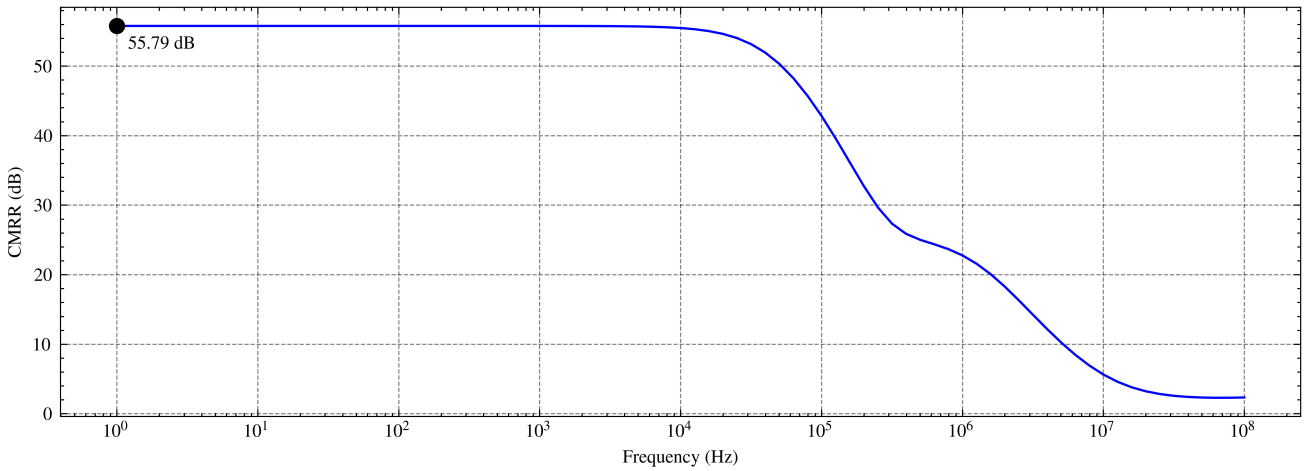


Figure C.2: CMRR Diode-Load Differential Amplifier Open-Loop

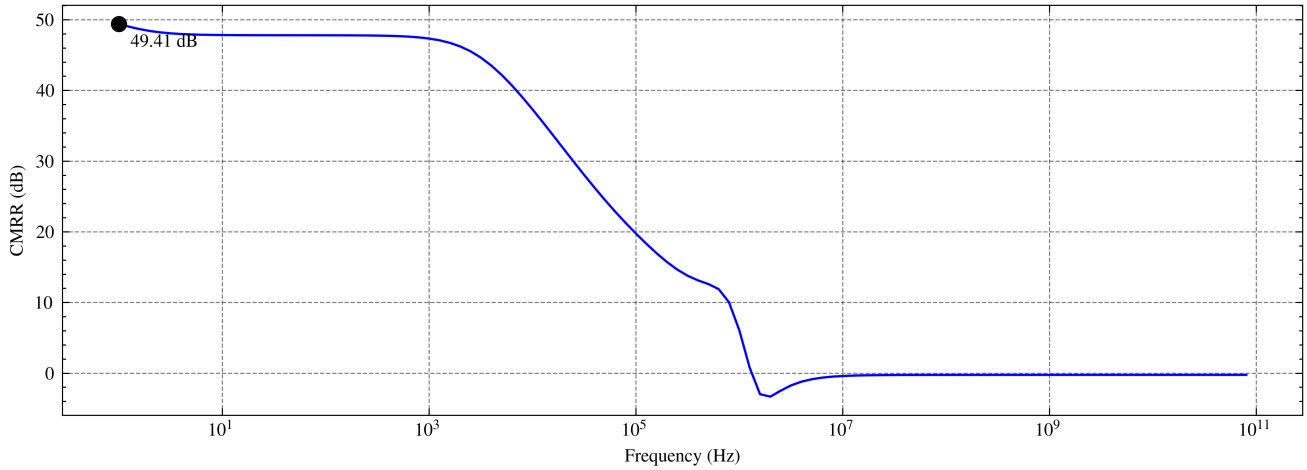


Figure C.3: CMRR Bootstrapped Differential Amplifier

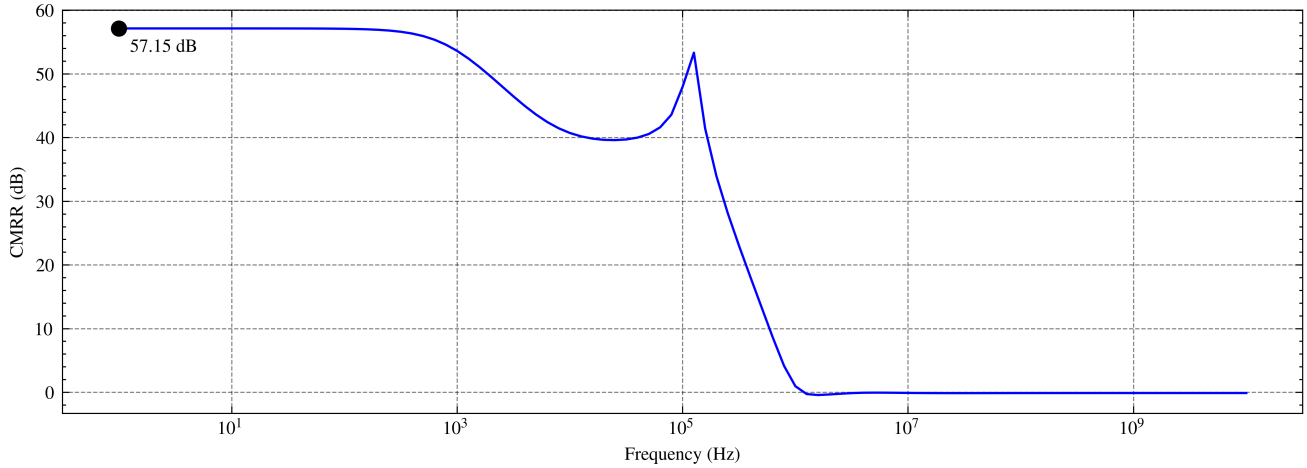


Figure C.4: CMRR Transconductance Boosting Differential Amplifier

Appendix D

Appendix - No Miller Compensation Bode Plot

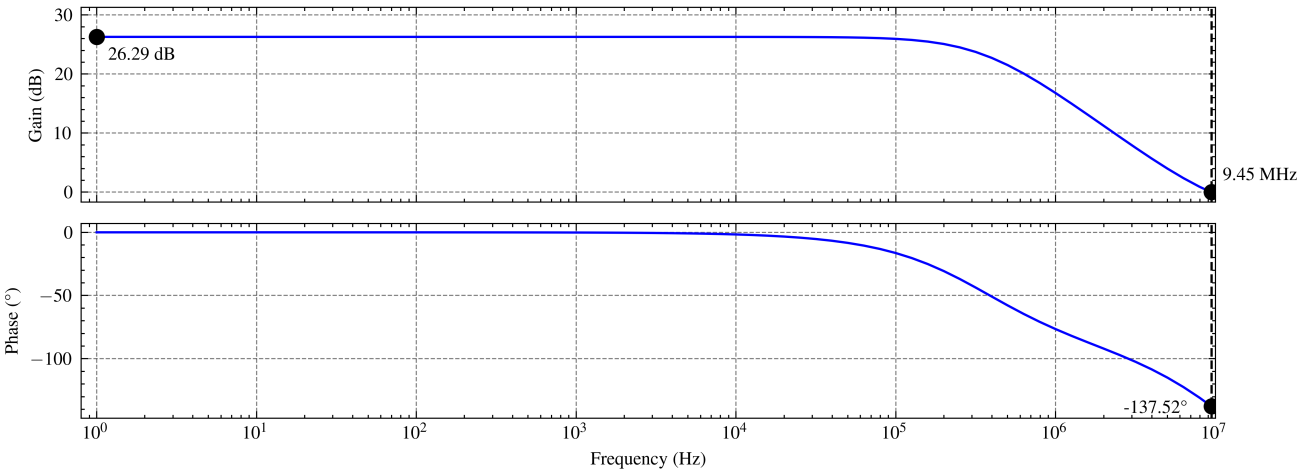


Figure D.1: Diode-Load Differential Amplifier Without Miller Compensation

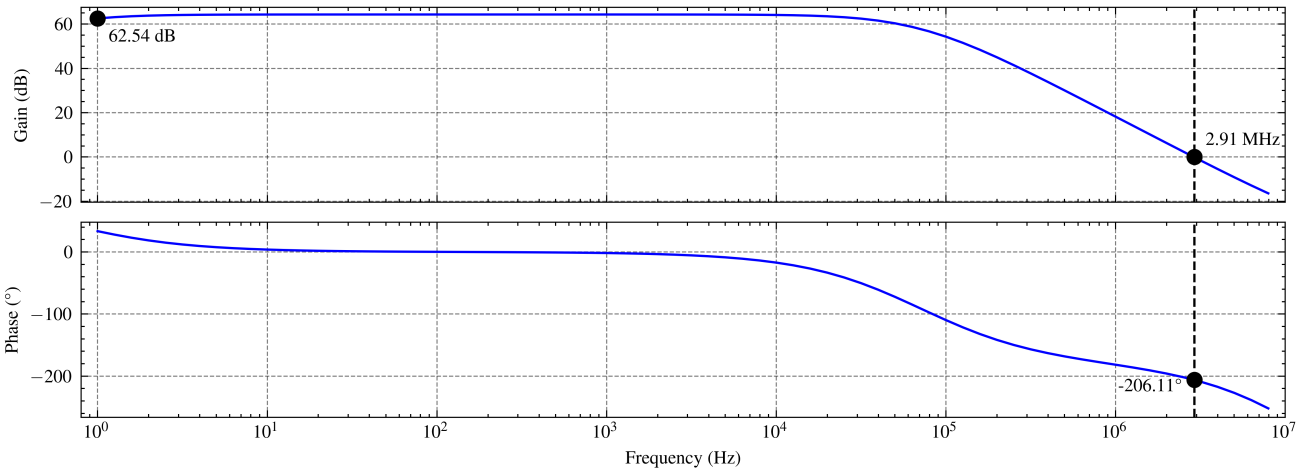


Figure D.2: Bootstrapped Differential Amplifier Without Miller Compensation

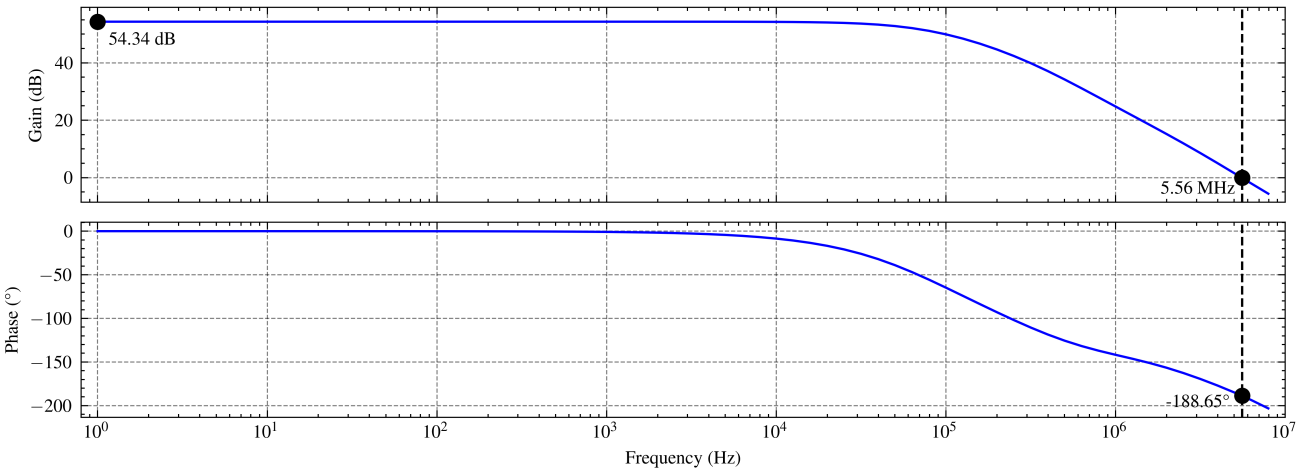


Figure D.3: Transconductance Boosting Differential Amplifier Without Miller Compensation

Appendix E

Appendix - Electrocardiogram Recordings

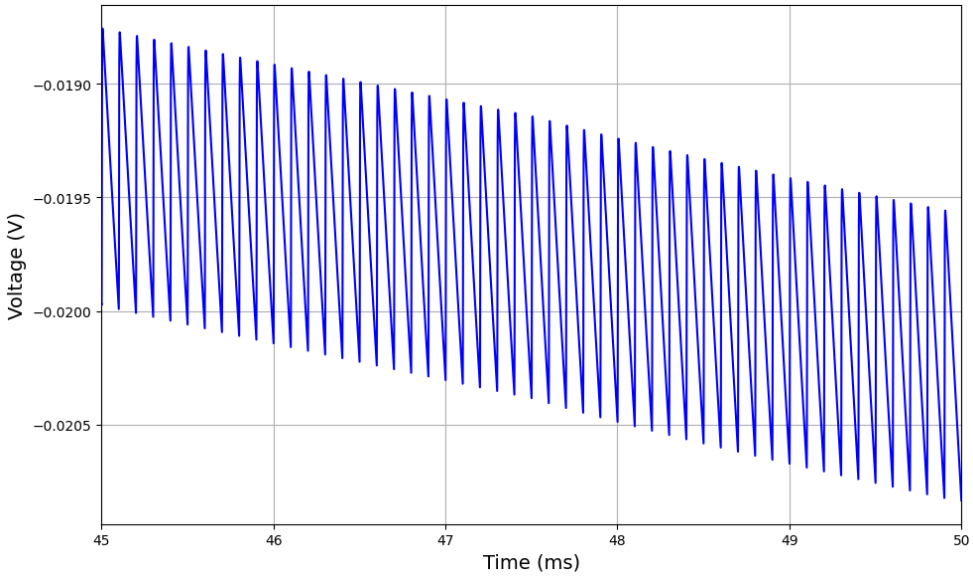


Figure E.1: Ripple on Output Differential Amplifier