Development of a Bio-Potential Chopping Amplifier for Flexible Electrocardiogram Systems

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Introduction

Technological advances have had a profound **impact** on the field of **human healthcare [1]**, with the two fields becoming increasingly **intertwined**, as evidenced by recent developments involving **Artificial Intelligence (AI)** and **wearable electronics**. The utilisation of **comprehensively trained AI models**, **combined** with **wearable electronics**, enables the **diagnosis** of patients form virtually **anywhere [2],[3]**.

The **biomedical information** utilised by the AI model is **measured** and stored on the **wearable electronic device**. The aforementioned information is measured by an **analogue front-end**, which is **amplifies** and **transform** the signal from **analogue to digital**. The **aim** of this thesis is to **develop** a **chopping Operational Amplifier (OPAMP)** utilising flexible **Indium Gallium Zinc Oxide (IGZO) technology** for application in **electrocardiogram (ECG)** systems. The **IGZO technology** is **incompatible** with **p-type transistors** due to the fundamental properties of the material itself. This **implies** that the **OPAMP** needs to be **designed** with **only N-type transistors**.

Methodology

To create the **OPAMP** the **PragmatIC** 600nm IGZO technology will be used in **Virtuoso Cadance**.
The OPAMP can be divided into four parts:

- **Chopping modulator** is used to modulate the signal to a higher frequency which is greater than the 1/f noise. This technique is used to mitigate the impact of 1/f noise on the system.
- **Chopping demodulator** reconstructs the chopped signal back into its original form, while maintaining the amplification.
- **Differential stage** is utilised to enhance the Common-Mode Rejection Ratio (CMRR) of the system by amplifying the difference between the two input signals.
- **Amplification stage** is used to further improve the gain of the system.

Chopping

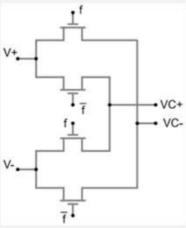

Fig. 1: Chopping Modulator

The design of the chopping modulator is illustrated in Figure 1.

A **square wave** with an **amplitude** of 3 V is **applied** to the f **gate** and the **inversed wave** at the $\overline{f}$ **gate**. The **transistors used** in the initial segment of the chopper are **small compared** to the **demodulator** at the output. This design choice is implemented to **increase** the **input impedance**, whilst **decreasing** the **output impedance**. The chopping frequency of this system is 1 KHz, which is near the 1/F corner frequency for IGZO transistors [8].

Differential

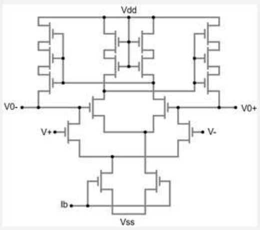

Fig. 2: Differential Stage

The design of the differential stage is shown in Figure 2.

This stage employs **feedback** as a **load** for the **differential stage**, which maintains a **constant current flow** through the load and effectively presents a **high output impedance**. This is achieved by **increasing** the **gate voltage** of the **load transistors relative to its source voltage**. The **transistors** positioned at the **bottom controls** the **common-mode rejection ratio** of the system. This circuit operates at a **3 V supply voltage**, with a **1 µA** current source.

Amplifier

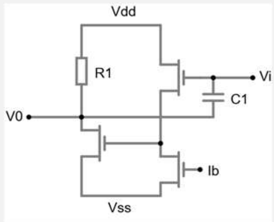

Fig. 3: Amplification Stage

The design of the amplification stage can be found in Figure 3.

This stage can be **subdivided** into a **voltage shifter** and **single stage amplifier**. The voltage shifter effectively **downshifts** the **DC offset** of the **input** to **ensure**, **together with R1**, that the **signal stage amplifier** operates in the **saturation** region. The **capacitance** C1 is **used** to **increase** the **phase margin** of the system by **moving** the **dominant pole** to a **lower frequency.**

Results and conclusion

Tbl. 1: Comparison with Literature Study

	[4]	[5]	[6]	this work
TFT Process	A-IGZO	A-SI	A-IGZO	A-IGZO
aplication	ECG	EEG	EMG	ECG
Amplification (dB)	43.5	20	25	53.5
Unity GainBand width (KHz)	290	2	-	489
CMRR (dB)	61.2 @ 100Hz	30 - 50	-	57.15
Vdd (V)	15	55	26	5
power (µW)	200	11000	1300	105.6

Figure 4 illustrates the **output voltage** of the **created amplifier**, which shows a **closed loop gain** of **53.5 dB** at a chopping frequency of 1KHz, when **capacitive feedback** is applied. The **system** has a **phase margin** of **59.60°** and **consumes 105.6 µW** of power. This amplifier is compared with the literature in Table 1.

Figure 4 demonstrates that the **ECG signal** can be **modulated** and **recovered** while **maintaining** an **amplification**. The **OPAMP utilises** a **3 V supply voltage**, indicating its suitability for **integration** into **flexible chips** where **power availability** is **limited**. However, the **output signal** exhibits a **ripple** which is **attributed** to the **charging behaviour** of the **OPAMP**. **Future work** could **explore** the use of **additional filtering techniques** to **mitigate** this **ripple**.

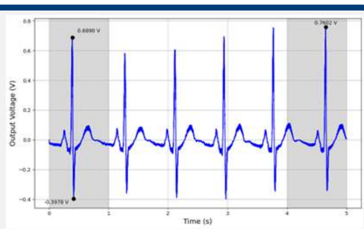

Fig. 4: Time-Domain Amplified Bio signal

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