Faculteit Industriële Ingenieurswetenschappen

master in de industriële wetenschappen: elektronica-ICT

Masterthesis

The Development of an Analog Front End in LTPO Technology

Bjorn Spauwen

Scriptie ingediend tot het behalen van de graad van master in de industriële wetenschappen: elektronica-ICT

PROMOTOR :
Prof. dr. ing. Kris MYNY

PROMOTOR :
dr. ir. Mohit DANDEKAR

BEGELEIDER :
De heer Yari NOWICKI

Gezamenlijke opleiding UHasselt en KU Leuven

UHASSELT KU LEUVEN

Universiteit Hasselt | Campus Diepenbeek | Faculteit Industriële Ingenieurswetenschappen | Agoralaan Gebouw H - Gebouw B | BE 3590 Diepenbeek

Universiteit Hasselt | Campus Diepenbeek | Agoralaan Gebouw D | BE 3590 Diepenbeek
Universiteit Hasselt | Campus Hasselt | Martelarenlaan 42 | BE 3500 Hasselt

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Preface

The conclusion of this master's thesis marks the end of my four-year studies at the Faculty of Engineering Technology of Hasselt University and KULeuven. I am leaving this period of my life behind not only with an engineering master's degree but also with many fond memories and personal growth. The writing of this thesis has taught me many new things about the link between electrical circuit design and healthcare, which will greatly help me towards my future career goals.

Firstly, I would like to show my gratitude to my co-advisor at ES&S ing. Yari Nowicki, for his guidance through this thesis. I would also like to thank Prof. dr. ing. Kris Myny for his unwavering commitment towards the Master's programme Electronics-ICT and its students. In addition, I would like to thank ing. Jelle Biesmans and Muhammad Dawood Asghar for their support.

Secondly, I would like to thank my family for always standing alongside me and providing a listening ear through the most stressful moments.

And finally, I would like to thank my peers and friends for their constant companionship and a healthy sense of competition that has kept me pushing to get the best version out of myself.

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List of Abbreviations

a-IGZO	amorphous Gallium-Indium-Zinc-Oxide
AC	Alternating Current
ADC	Analogue to Digital Converter
AFE	Analogue Front-End
ALU	Arithmetic Logic Unit
CLK	Clock
CMRR	Common Mode Rejection Ratio
DC	Direct Current
DSP	Digital Signal Processing
ECG	Electrocardiogram
HRV	Heart Rate Varation
LTPO	Low-Temperature Poly Oxide
LTPS	Low-Temperature Poly Silicon
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
SR	Slew Rate
TFT	Thin Film Transistor
VDD	Positive supply voltage
Vin	Input voltage
Vout	Output voltage
VSS	Negative supply voltage
W/L	Width to Length Ratio

Abstract

Thin-film transistors (TFTs) have gained increasing interest in specific applications due to their ability to bend and fold in any direction. One promising application is electrocardiogram (ECG) signal monitoring, where flexible chips could enable on-skin amplification and local processing of the heart's signals. A recent advancement in TFT technology is the emergence of Low-Temperature Polycrystalline Oxide (LTPO), which hybridises the p-type TFTs of Low-Temperature Poly Silicon and the n-type TFTs from Amorphous Indium Gallium Zinc Oxide. In this thesis, an analogue front end (AFE) for ECG is developed using LTPO technology. The AFE consists of an analogue amplifier, followed by a digital heartrate detection circuit.

The amplifier employs a two-stage fully differential architecture featuring cascaded transistors. The design achieves a closed-loop gain of 49.6 dB ($\approx$ 300x), with a -3 dB cut-off frequency of 8.5 kHz and a phase margin of 30°. This combination of high gain and appropriate bandwidth makes the amplifier suitable for ECG monitoring. Additionally, a digital heartbeat detector is designed based on the StrongARM latch topology, followed by an edge detector. The complete AFE provides three outputs: two amplified differential output signals and a digital heartbeat pulse. The system operates on a 3 V power supply, with an average power consumption of 6.8 µW. The results show significant improvement, especially in power consumption, compared to previous LTPO research.

Abstract in Dutch

Thin Film Transistors (TFT's) staan bekend om hun buigbaarheid in alle richtingen, wat hen bijzonder geschikt maakt voor flexibele toepassingen. Een interessante toepassing is het lokaal monitoren van elektrocardiografische (ECG) signalen, waarbij een volledig flexibele chip de elektrische hartsignalen ter plaatse kan versterken en verwerken. Een recente ontwikkeling in TFT-technologie is de opkomst van Low Temperature Polycrystalline Oxide (LTPO), dat een hybride is van de p-type TFT's van Low Temperature Poly Silicon en de n-type TFT's van Amorf Indium Gallium Zinc Oxide. In deze thesis werd een analoge front end (AFE) in LTPO ontworpen, specifiek voor ECG, bestaande uit een analoge signaalversterker en een digitaal hartslagdetectiecircuit.

De signaalversterker bestaat uit een tweetraps volledig differentiële architectuur met in cascade geschakelde transistors. Het ontwerp bereikt een geslotenlusversterking van 49,6 dB ($\approx$ 300x), met een -3 dB afsnijfrequentie van 8.5 kHz en een fasemarge van 30°, wat het geschikt maakt voor nauwkeurige ECG-verwerking. Daarnaast is er een digitale hartslagdetector ontworpen op basis van de StrongARM-latchtopologie, gevolgd door een flankdetector. De complete AFE levert drie uitgangen: twee versterkte differentiële uitgangssignalen en een digitale hartslagpuls. Het systeem werkt op een voeding van 3 V, met een gemiddeld stroomverbruik van 6,8 µW. Vergeleken met eerder LTPO-onderzoek tonen de resultaten een aanzienlijke verbetering, vooral in stroomverbruik.

Chapter 1

Introduction

1.1 Motivation

In the analogue circuit design sector, thin-film transistors (TFTs) are emerging as a complementary technology to the industry-standard silicon-based Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) technologies in specific applications because of their ability to fold and bend in any direction. TFTs are already widely used in displays on mobile devices, alongside some promising applications in other fields such as wearable healthcare devices [1], [2], [3], [4].

Recently, a new TFT technology has surfaced that hybridises the p-type TFTs of Low-Temperature Poly Silicon (LTPS) and the n-type TFTs from Amorphous Indium Gallium Zinc Oxide (a-IGZO), called Low-Temperature Polycrystalline Oxide (LTPO). This technology has found its use in high-end variable refresh rate displays [5], [6]. However, their integration into non-display analogue circuits remains largely unexplored. This thesis aims to develop an application for LTPO TFT technology, to be used in a low-power analogue front-end (AFE) circuit for electrocardiogram (ECG) signal measurement, thereby extending its application beyond conventional display use. Ultra-thin chips and sensors that can bend in any direction have a high potential as wearable health monitors [7]. A device like this can potentially be attached to the human skin like a plaster, unlocking the ability to passively monitor the patient's health in new ways without the presence of a qualified physician. To make such technology practical and accessible, it is crucial that these systems are both low-power and cost-effective. Minimising power consumption enables long-term continuous monitoring without frequent battery replacements or recharging, which is essential for real-world medical use. Likewise, keeping production costs low enables widespread deployment in both hospitals and home environments, helping to make healthcare more accessible and scalable.

1.2 Problem Statement

During a standard ECG measurement, electrodes are attached directly to the skin to record the electrical activity of the heart in a technique called analogue lead derivation (ALD) [8]. These analogue signals are then fed into an analogue-to-digital converter (ADC), or directly transferred via long cables to a processing unit for further analysis. In this latter configuration, weak ECG signals are susceptible to noise generated by external factors like the human body, electronic

equipment, or cables. This significantly reduces the integrity of very the low-power biological signals [9]. However, if the amplifier/AFE is connected directly to the electrodes on the skin, which are extremely close to the source of the signals, then the noise can easily be subtracted. This ensures that only the essential components of the ECG are transmitted with high signal integrity [10]. A typical AFE contains more than just an amplifier. It usually consists of a variety of components, such as operational amplifiers, active filters, and analogue to digital converters (ADCs) [11].

1.3 Objectives

The primary objective of this thesis is to explore the application potential of LTPO TFT technology and to evaluate its performance in comparison with other TFT technologies.

The research first focusses on the design of an analogue signal amplifier tailored for ECG signals. Given the characteristics of ECG waveforms, the amplifier will be optimised to deliver high gain at low frequencies while consuming minimal power, maintaining excellent signal integrity, and to drive large loads at the output without degradation in performance.

The second objective is to develop a digital signal processing (DSP) unit capable of receiving the amplified analogue signals, accurately detecting heartbeat events, and generating corresponding digital outputs for further analysis. This unit will be designed with an emphasis on low power consumption, making it suitable for continuous operation in wearable devices.

Together, these objectives aim to provide new research towards LTPO as a viable option in TFT technologies for integration in fully flexible and wearable devices, with a specific application in the healthcare sector.

1.4 Thesis outline

The rest of this thesis is divided into four more chapters:

Chapter 2 – Literature Study: Covers the fundamentals of LTPO TFT technology, ECG signal characteristics, and existing analogue front-end designs.

Chapter 3 – Analogue Design Methodology: Describes the design approach for the analogue amplifier, and the considerations made.

Chapter 4 – Results and Discussion: Presents the design, simulation results, and performance analysis of three proposed ECG amplifiers, and the digital signal processing unit. Additionally, a power consumption analysis is made on the complete AFE circuit and comparisons are made to other state-of-the-art TFT designs.

Chapter 5 – Conclusion and Discussion: Concludes the results of the thesis and suggests improvements and future follow-up work on this thesis.

Chapter 2

Literature study

2.1 Thin Film Transistors (TFTs)

TFTs are a type of Field Effect Transistor (FET) based on the deposition of thin layers of semiconductor, dielectric, and metallic contacts on an insulating substrate. Compared to the more commonly known Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs), TFTs are typically manufactured on top of a glass or plastic substrate in a relatively low-temperature process, allowing for extremely thin and flexible electronic applications. In addition, TFTs are cheap and easy to manufacture on a large scale [12]. So far, TFTs have mostly found their use in active matrix displays such as Liquid Crystal Displays (LCDs) [13] as on/off switches for all individual pixels and drivers in flat-panel displays due to their fast switching ability [14]. TFT is a collective name for multiple structure designs. Some of the most relevant are the following:

- Amorphous silicon (a-Si)
- Amorphous indium gallium zinc oxide (a-IGZO)
- Low temperature poly silicon (LTPS)
- Low temperature poly oxide (LTPO)

The most commonly used TFT in LCD displays is a-Si due to its simplicity and cheap manufacturing. However, its relatively low carrier mobility means slower switching. More high-end applications are therefore opting for different materials, such as a-IGZO or LTPS. LTPS TFTs, for example, achieve a much higher field-effect mobility (μ_{FE}) of approximately 100 cm^2/Vs compared to 1 cm^2/Vs for a-Si [15], [16]. However, LTPS technology is less suitable for lower frame rate displays due to its relatively high off-state currents (I_{FE}) [17]. In contrast, a-IGZO TFTs exhibit significantly lower leakage currents, making them much better suited for such applications. Nevertheless, their μ_{FE} of approximately 10 cm^2/Vs is comparatively lower and therefore less desirable for high-performance circuits. However, a-IGZO consists only of n-type transistors (contrary to the usual CMOS transistor topology, consisting of both n-type and p-type transistors) due to the high density of defect states above the valence band [18], [19]. To overcome the limitations of both technologies, LTPO was developed as a hybrid circuit architecture that combines p-type LTPS TFTs for driving elements with n-type a-IGZO TFTs for switching elements. This enables the implementation of complementary CMOS-like logic, offering advantages such as rail-to-rail output, reduced noise, and lower power consumption.

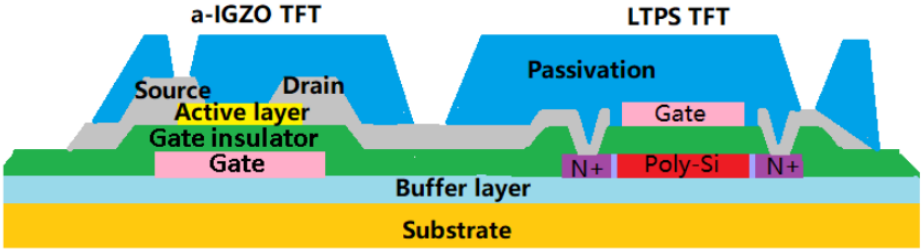


Figure 2.1: Typical device configuration of LTPO [21].

2.2 LTPO Fabrication and Applications

In 2017, the first hybrid integration of p-channel LTPS and n-channel a-IGZO on the same substrate was demonstrated [20]. Since then, LTPO has been commercially implemented primarily in variable refresh rate displays [5]. This section will go over the fabrication process of LTPO and explores and compares several other research efforts involving LTPO technology.

2.2.1 Fabrication Process

The typical cross-sectional structure of an LTPO inverter is illustrated in Figure 2.1 with the n-type a-IGZO TFT on the left and the p-type LTPS TFT on the right. The fabrication is done by building the p-channel TFTs in a top-gate, top-contact configuration, followed by the n-type TFT in a bottom-gate, top-contact configuration. First, the process starts by depositing a thick SiO_2 layer onto a substrate via plasma enhanced chemical vapour deposition (PECVD). The Poly-Si layer is grown by consequently treating an a-Si film placed on the buffer layer via PECVD. This newly formed Poly-Si layer is then photolithographically patterned and then etched via reactive ion etching (RIE) to form the isolated islands. The N+ source and drain regions are doped with boron ion implantation and followed up by a rapid thermal annealing (RTA) process. Both the n-type and the p-type gate are placed by direct current sputtering and wet etching of the metal oxide layer. The gate insulator layer also serves as an interlayer on the LTPS TFT between the gate and the Poly-Si layer and consists of another SiO_2 layer placed via PECVD. Note that source and drain contact holes are also formed in this stage by patterning. Next, the n-type a-IGZO active layer is deposited by reactive sputtering and placed with wet etching. The source and drain metal layers are formed by sputtering and patterning another metal oxide layer. As the last step, a thick passivation layer is deposited by PECVD, and via holes are formed at the source and drain. A more elaborate explanation of the fabrication process can be found in [13], [20], [17].

2.2.2 Pixel Circuit

The first commercial implementation of LTPO TFTs on the market was in the Apple Watch Series 4. Figure 2.2 represents the circuit that drives each pixel on the AMOLED screen. The circuit consists of one metal oxide (a-IGZO) TFT used as the switching transistor, five LTPS TFTs, and a storage capacitor. Using a-IGZO as the driving transistor instead of the standard LTPS results in a much lower off-state current compared to the standard LTPS AMOLED displays [5].

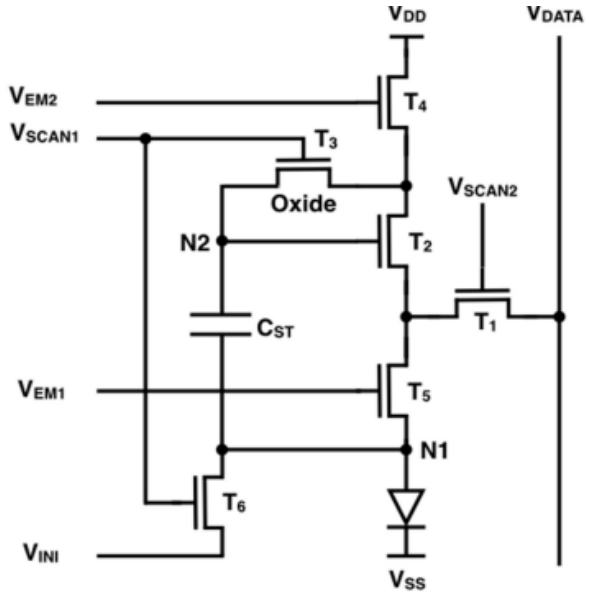


Figure 2.2: LTPO pixel circuit schematic [5].

2.2.3 Full Adder ALU

In 2022, researchers at the Chinese Academy of Sciences developed the first LTPO Arithmetic Logic Unit (ALU) [22]. The 1-bit ALU circuit contains the arithmetic operations ADD, SUB, logical operations AND and OR, and set less than (SLT). The proposed ALU circuit contains one AND gate, one OR gate, one full adder, one inverter, and two multiplexers as seen in Figure 2.3. The ALU operates on a 15 V supply voltage. The results show that the LTPO ALU has significantly lower rise and fall times (32 µs and 64 µs, respectively) and a smaller circuit area compared to other TFT-based ALUs.

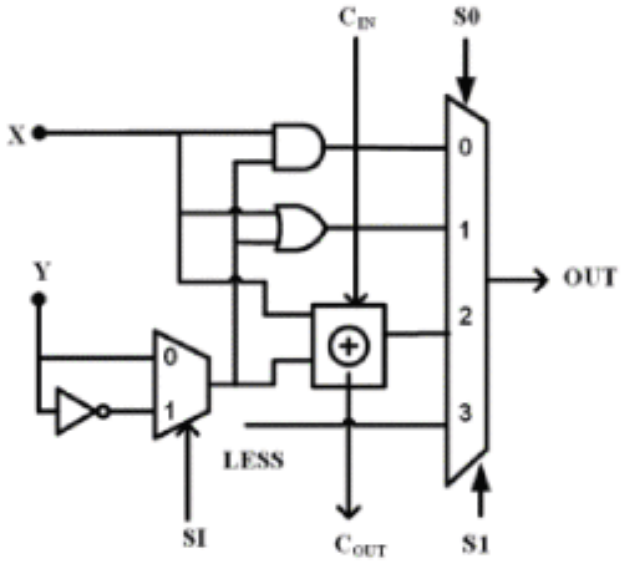


Figure 2.3: Circuit diagram of 1-bit LTPO ALU [22].

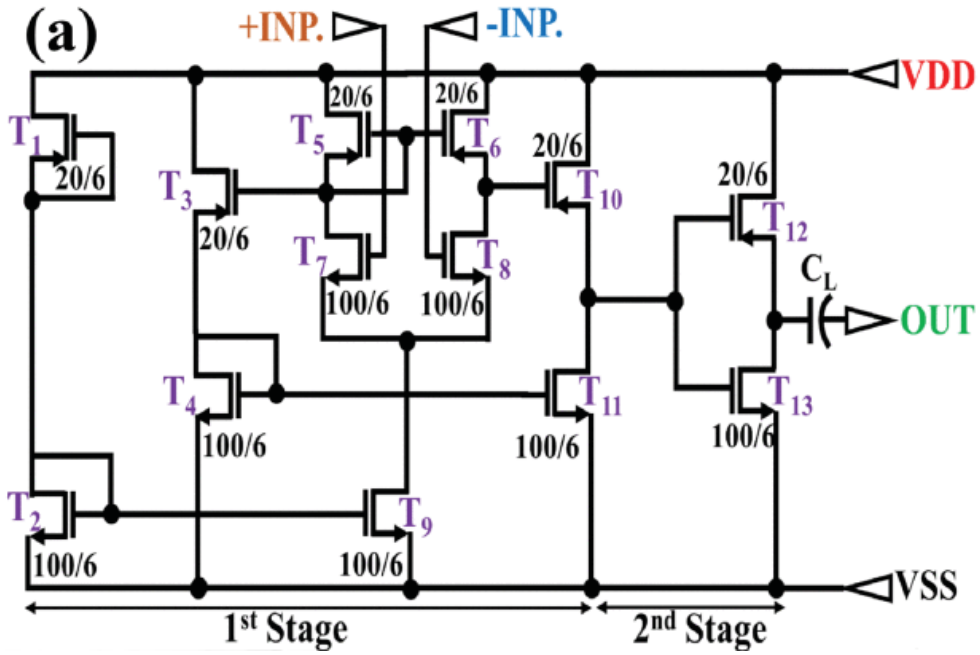


Figure 2.4: Schematic of the proposed two-stage LTPO op-amp, with the W/L ratio of each TFT in µm [13].

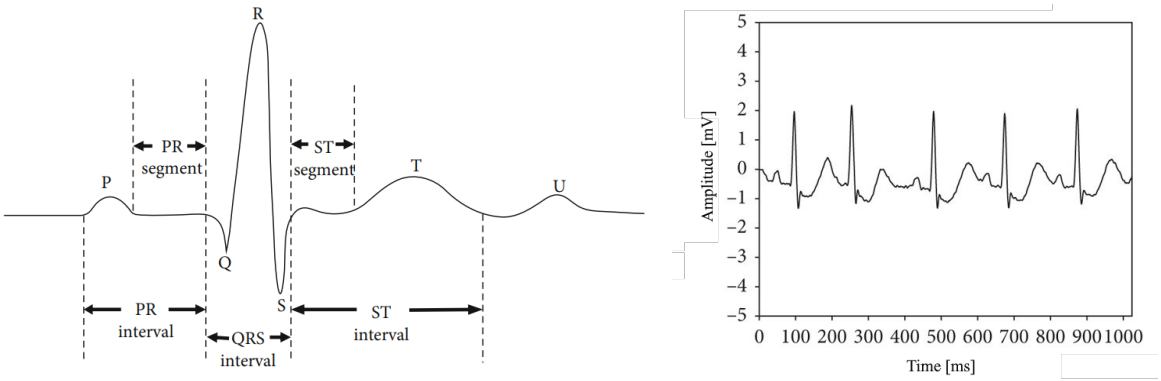
2.2.4 Operational Amplifier

Previous research on amplifiers based on LTPO TFT technology resulted in the two-stage single-ended operational amplifier (op-amp) shown in Figure 2.4. The circuit design consists of six p-type TFTs and seven n-type TFTs. The circuit can be divided into two stages. The first stage contains the input stage, current mirror, and the differential to single-ended converter stage. The second stage serves as an output buffer stage to improve the current drive capability.

This design achieves a voltage gain of 50.7 dB with a cut-off frequency of 200 kHz, and a unity gain bandwidth of 7 MHz. The op-amp operates on a ±20 V dual power supply and consumes 0.6 mW of power. The op-amp also exhibits a slew rate of 22.7 V/µs up and 6.4 V/µs down. These results prove that an LTPO TFT amplifier is capable of producing a high gain over a very large frequency range. However, this amplifier is not suitable for a wearable ECG AFE. The use of a high dual power supply is incompatible with typical wearable applications, which operate on a single, low-voltage supply (commonly 3 V or less) to ensure safety and energy efficiency [23]. Furthermore, both the amplifier's cut-off frequency and the slew rate far exceed the requirements for ECG signal processing. Reducing these specifications would lead to a more power-efficient and application-specific design without compromising the signal integrity.

2.3 AFE for ECG signals

ECG is the recording of electrical activity generated by the heart during each muscle contraction cycle. It is a widely used diagnostic tool for detecting and monitoring various cardiac conditions. With the increasing demand for smart healthcare solutions, significant research is already underway on developing a flexible wearable device to measure heart rate and ECG signals [4], [10], [24], [25].



(a) (b)

Figure 2.5: Typical ECG signal cycle. a) a single ECG cycle, and b) ECG over a 10-second period. [26].

2.3.1 Measurement

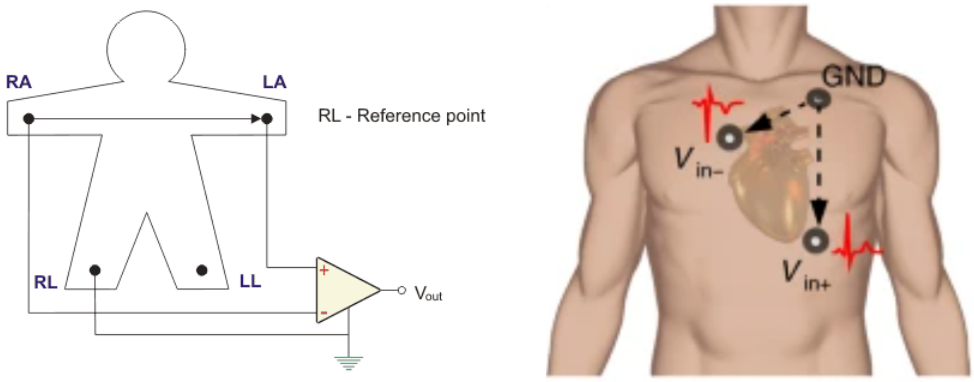
Figure 2.5a shows an illustration of a single heartbeat cycle of the ECG with all major waveform components highlighted. Figure 2.5b shows the waveform diagram of an ECG recording over a 10-second interval, demonstrating noticeable variations between consecutive cycles. A typical ECG signal consists of a common-mode voltage of $\sim$ 1.5 V, with an additional direct current (DC) component of $\pm$300 mV and an average voltage amplitude of 2.5 mV, with occasional peaks of up to 5 mV [11]. Due to their low amplitude and susceptibility to various sources of noise, raw ECG signals require careful amplification and filtering before further processing. This task is performed by the AFE, which amplifies the signal while preserving signal integrity and suppressing noise.

From an engineering standpoint, the heart functions as a source of bio-electrical signals, while the body serves as the conductive path through which these signals propagate. These potential differences can be measured by placing two or more electrodes on the surface of the skin. The resulting signals are known as leads. Each lead provides a different projection of the electrical activity of the heart. Figure 2.6 illustrates a simplified example of the lead I measurement method, which measures the potential difference between the right arm (RA) and the left arm (LA). The resulting ECG signal can be derived as follows:

$$\text{Lead I} = \text{LA} - \text{RA} \tag{2.1}$$

2.3.2 Amplification Stage

Considering the amplifier stage, the American Health Association (AHA) recommends a bandwidth of 125 Hz for measuring ECG on adults [27]. The guidelines further specify that the amplitude response should remain flat to within $\pm$0.5 dB across the 0.1-30 Hz range, with the -3 dB cut-off frequencies no higher than 0.67 Hz at the low end and no lower than 150 Hz at the high end. [28] has established a standard bandwidth of 250 Hz for measuring ECG signals on children up to 16 years old. Any frequencies higher than this can be considered as noise and should be filtered out in the AFE.



(a) (b)

Figure 2.6: Illustrations for a) the electrical signal of Lead I measurement and b) the placement of the electrodes in context for a smart plaster [10].

2.3.3 ADC

A typical AFE consists of a chain of instrumentation and/or operational amplifiers, followed by filtering stages and an ADC. The resulting output is a digital representation of the ECG waveform suitable for further interpretation and processing by an external system. All components preceding the ADC are designed to condition the signal to ensure it operates within its optimal range and captures the analogue signal as accurately as possible. An ADC's resolution refers to the smallest distinction in voltage it can detect. For example, on an 8-bit ADC, with a reference voltage (V_{ref}) of 3 V (usually equal to the power supply voltage), the resolution is as follows:

$$\text{Resolution} = \frac{V_{ref}}{2^N} \tag{2.2}$$

$$= \frac{3.00\ V}{2^8} = 11.7\ mV \tag{2.3}$$

Note that this value already exceeds more than twice the maximum amplitude typically observed in ECG signals. As a result, this ADC is not suitable for directly processing a raw ECG input. To ensure accurate digitisation, the ADC resolution must increase significantly, or the input signal must be appropriately amplified to utilise the full dynamic range of the ADC.

These results suggest two viable design approaches for an AFE. The first involves employing a high-gain, low-noise analogue circuit that sufficiently amplifies the signal before digitisation with a lower-resolution ADC. Alternatively, a low-gain amplifier can be used in conjunction with a high-resolution ADC to capture the signal accurately without extensive amplification. Texas Instruments recommends an amplification of approximately 500x for a 16-bit ADC, or a 24-bit ADC for an amplification of approximately 5x [11]. Assuming a reference voltage of 3.00 V for both cases, this results in the following effective voltage resolutions:

$$\text{Resolution}_{16-bit} = \frac{3.00\ V}{2^{16}} = 45.8\ \mu V \tag{2.4}$$

$$\text{Resolution}_{24-bit} = \frac{3.00\ V}{2^{24}} = 179\ pV \tag{2.5}$$

If we now assume average voltage peaks of 2.5 mV, the amount of different data points between the common-mode voltage and the peak voltage, for an amplifier with an amplification of 500x with a 16-bit ADC and an amplifier with an amplification of 5x with a 24-bit ADC respectively, can be approximated with the following equation:

$$\text{Data Points}_{16-bit} = \frac{2.5\ mV * 500}{45.8\ \mu V} = 27,300 \tag{2.6}$$

$$\text{Data Points}_{24-bit} = \frac{2.5\ mV * 5}{179\ pV} = 70,000 \tag{2.7}$$

Although the second hypothetical AFE yields nearly three times as many potential data points as the first, both can be considered to operate within the same order of magnitude. Each is capable of delivering a high-quality digital output suitable for ECG signal processing. Ultimately, the choice between these designs depends on the trade-offs the design engineer is willing to make between performance requirements, power constraints, and cost in order to achieve the most optimal AFE implementation.

Chapter 3

Analogue Design Methodology

This chapter discusses and justifies the design choices made in the analogue amplifiers presented in this thesis to meet the requirements of an AFE for ECG signals.

3.1 Fully Differential and Single-Ended amplifiers

An operational amplifier that provides a single output referenced to ground is referred to as single-ended, whereas one that produces two complementary outputs is known as fully differential. A differential signal consists of two voltages with equal magnitude and frequency but opposite polarity. These signals can be characterized by two components: the common-mode voltage (V_{CM}), which is the average of the two output voltages, and the differential-mode voltage (V_{DM}), which is the difference between them.

The primary advantage of a fully differential output is its immunity to external noise sources that affect both signals equally. Consider the example of an amplifier with a supply noise in Figure 3.1. The noise generated by the supply voltage V_{DD} affects both the single-ended output V_{out} and the fully differential output signals V_{X} and V_{Y}. However, since the V_{DD} noise appears as a common-mode component, it will be removed in V_{DM}, which is equal to $V_{\mathrm{X}} - V_{\mathrm{Y}}$. ECG signal measurements will contain many of these types of external noise, not only from the supply voltage but also at the input nodes caused by the human body. In addition, since this specific amplifier will likely be placed close to the human skin, it will constantly be influenced by these external signals. All of these influences can be eliminated by implementing a differential output over a single-ended output.

An additional advantage of fully differential amplifiers is their greater signal swing. A single-ended output signal can swing from $0V$ to V_{DD}, and a fully differential output allows each output node to swing over this same range in opposite directions. As a result, the total differential output swing can reach $2V_{\mathrm{DD}}$, doubling the available dynamic range.

3.2 Input differential pair

Figure 3.2 illustrates a basic common-source amplifier stage. It is referred to as "common-source" because the source terminal of the transistor serves as a shared reference point for both the input signal applied at the gate and the output signal taken from the drain. The amplification of a

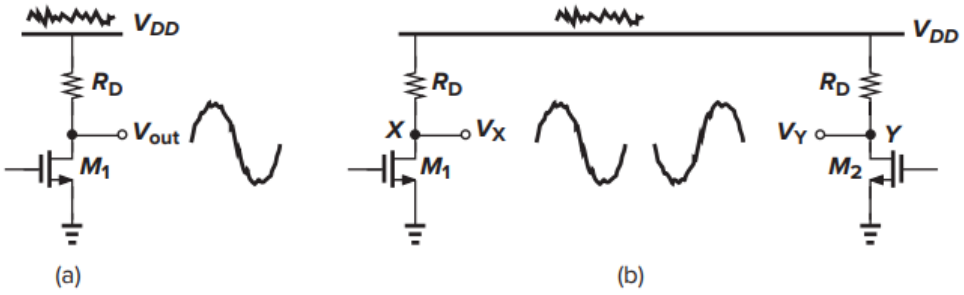


Figure 3.1: Effect of supply noise on (a) a single-ended circuit and (b) a differential circuit.

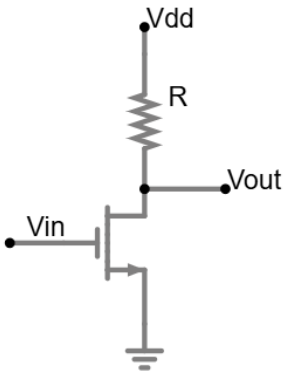


Figure 3.2: Common-source input pair.

signal A_v is defined by the ratio between the change in the output signal ∂V_{out} and based on a change in the input signal ∂V_{in}. For ease of analysis, it is assumed that all transistors operate in the saturation region. This means that the voltage between the drain and the source V_{DS} is always higher than the voltage difference between the gate and the source V_{GS} and the threshold voltage of the transistor V_T.

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = \frac{\partial V_{DS}}{\partial V_{GS}} \tag{3.1}$$

Assuming there is no change in input voltage, no current will flow to the output and $I_D = I_R$. This means that:

$$V_{out} = V_{DD} - V_R = V_{DD} - I_D R \tag{3.2}$$

The input signal V_{in} will be amplified to V_{out} by a factor of transconductance g_m of the transistor. This describes the change in current flowing through the transistor ∂I_D as a result of a change in gate-source voltage ∂V_{GS}.

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{3.3}$$

$$I_{D_{sat}} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \tag{3.4}$$

Based on the equation for the drain current in a transistor in saturation 3.4, the following equation can be derived:

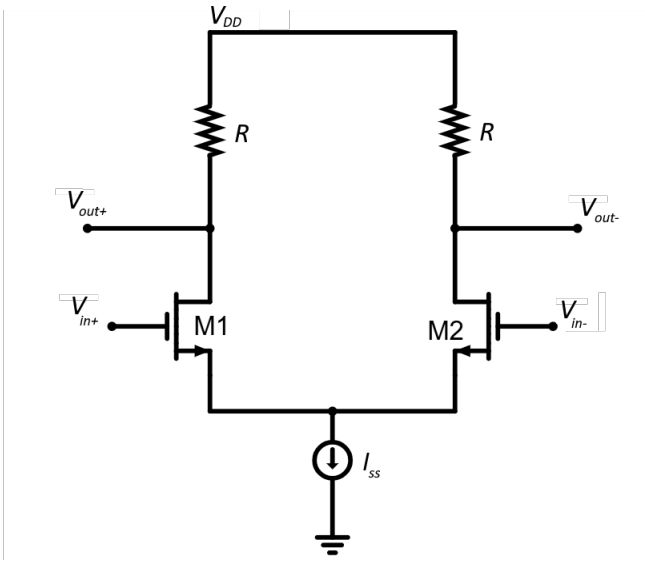


Figure 3.3: Input differential pair with resistive load.

$$g_m = \mu C_{ox} \frac{W}{L}(V_{GS} - V_T) \tag{3.5}$$

By inserting 3.4 into 3.2 we get:

$$V_{out} = V_{DD} - R\frac{1}{2}\mu C_{ox} \frac{W}{L}(V_{GS} - V_T)^2 \tag{3.6}$$

Now, inserting this into 3.1 we get the following equation for the amplification of a simple common-source stage:

$$A_v = -R\mu C_{ox} \frac{W}{L}(V_{GS} - V_T) \tag{3.7}$$

$$= -g_m R \tag{3.8}$$

Since the amplifier will contain a differential input signal and two output signals, the topology will need to have more than one input transistor. Figure 3.3 illustrates a typical input differential pair with a resistive load and a constant tail current source I_{SS}, which is always equal to $i_{D1}+i_{D2}$. This means that if $V_{in1} = V_{in2}$ then $i_{D1} = i_{D2} = i_{SS}/2$ and any change in $i_{D1} + \Delta i$ results in an equal change $i_{D1} - \Delta i$. The output common mode voltage V_{OCM} is as follows:

$$V_{OCM} = V_{DD} - \frac{RI_D}{2} \tag{3.9}$$

3.3 Positive Channel Load

The circuit in Figure 3.3 makes use of resistors as load devices in the circuit. These show up in equation 3.8 as a defining factor for the gain. Another way of greatly increasing this gain is by replacing them with p-type transistors with a constant bias voltage V_B at their gate, as

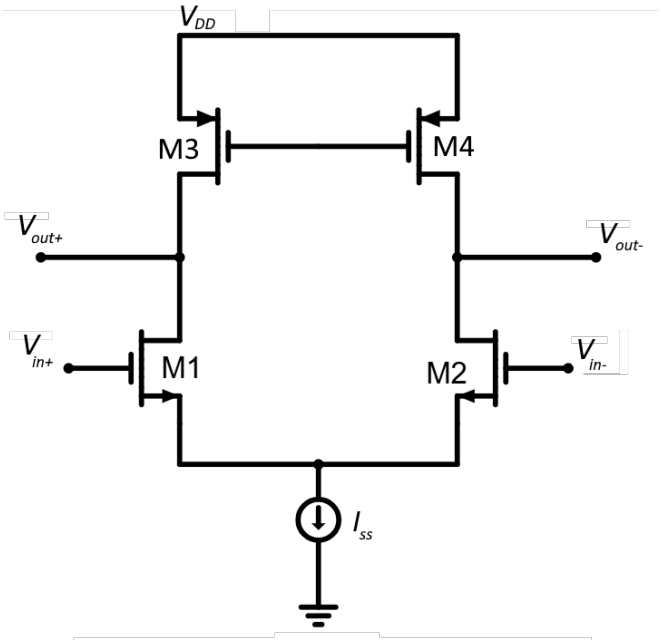


Figure 3.4: Differential pair circuit with p-type load.

illustrated in Figure 3.4. By substituting the resistance in equation 3.1 by the transconductance, the total resistance at the output node V_{out+} now becomes equal to $r_{O1}||r_{O3}$, and we get the following:

$$A_v = -\frac{g_m}{r_{o,1}||r_{o,3}} \tag{3.10}$$

With r_{O1} and r_{O3} the output impedance of the respective transistors. In a transistor, V_{DS} and r_O are not as strongly related as the value of a resistor to its voltage drop. This means that impedance (and, in turn, gain) can be increased while maintaining a low voltage drop [29].

3.4 Slew Rate and Tail Current

The slew rate (SR) of an amplifier is the maximum speed at which it can change the output signal, expressed in $V/\mu s$. It essentially defines how quickly the output voltage can change in response to a change in input voltage. When a fast or large input step is applied in a non-ideal amplifier, the output cannot immediately follow. This can cause performance limitations and lower the signal integrity. The slew rate can be defined as follows:

$$\mathrm{SR} = \max \left| \frac{dV_{\mathrm{out}}}{dt} \right| \tag{3.11}$$

To measure the slew rate of an amplifier, a signal with an infinitely high ΔV, also known as a step, is applied at the input (see Figure 3.5). The slew rate can be derived from $\Delta V_{out}/\Delta t$ in the linear part of the rise time.

In a simple differential pair amplifier, the slew rate is defined as follows:

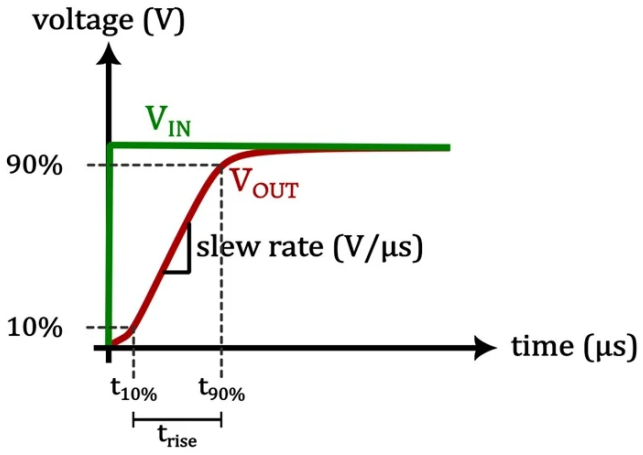


Figure 3.5: Slew rate example

$$\mathrm{SR} = \frac{I_{ss}}{C_L} \tag{3.12}$$

where I_{ss} is the tail current and C_L is the load capacitance [29].

In summary, the slew rate defines how quickly an amplifier can change its output voltage in response to an input change, and while this is crucial in high-speed applications, it is unnecessary for ECG processing. Designing for a high slew rate based on 3.12 results in a higher current through the input transistors, which in turn increases the overall power consumption. Since an ECG amplifier does not require fast switching due to the low-frequency nature of the signal, prioritising a high slew rate offers no practical advantage. Therefore, a low tail current is selected to support a low-power design that remains sufficient for the intended application. According to established guidelines, ECG AFEs should achieve a minimum slew rate of 400 µV/ms [30].

3.5 Cut-off frequency and phase margin

The cut-off frequency, f_c or $f_{-3\mathrm{dB}}$, of an amplifier is the point where its gain falls 3 dB below the low-frequency gain. It is essentially considered the highest frequency where the amplifier still provides an acceptable amplification compared to its low-frequency behaviour. As previously mentioned, standard ECG signals do not contain any significantly high frequency signals. This means the amplifier can be designed for a low cut-off frequency, and as a result also function as a low-pass filter.

When negative feedback is applied to an amplifier, the system's stability depends on maintaining a sufficient phase margin. If the phase shift φ reaches $-180°$ at a frequency where the gain is still above 0 dB, the negative feedback effectively becomes positive feedback with $0°$ phase shift, resulting in oscillation. Each pole in an amplifier introduces a $90°$ phase lag into the system [29]. Therefore, in systems with more than one pole, the total phase shift can approach or exceed $-180°$, especially at higher frequencies. In an ideal system without variability, it is sufficient to ensure that the amplifier phase surpasses $0°$ after the amplification drops below 0 dB. However, in real-world implementations, process variations and non-idealities can cause both the gain and phase to deviate from their ideal values. The phase margin represents the allowable deviation in phase before the system reaches instability, providing a buffer that ensures a stable operation

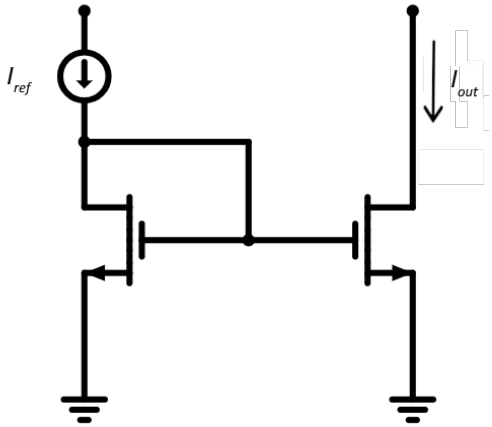


Figure 3.6: Simple NMOS current mirror.

under non-ideal conditions.

$$\mathrm{PM} = \varphi - (-180°) \tag{3.13}$$

Analogue design engineers usually opt for a phase margin of approximately 60°. However, any phase margin larger than 45° is generally acceptable [31]. If the phase margin falls below this value, the risk of oscillating on a negative feedback system will be too high.

3.6 Current Mirror Design

Referring back to Figure 3.3, the circuit contains a tail current source I_{SS} that keeps a constant current flowing between the sources of M1 and M2 and the ground. This constant current source is typically implemented using a current mirror that copies a constant independent reference current. In this context, a basic NMOS current mirror can be employed, as shown in Figure 3.6, where transistors M8 and M9 form a simple current mirror structure.

If both transistors operate in the saturation region, and by applying equation 3.4, the drain currents of the reference and output transistors can be expressed as:

$$I_{ref} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_1 (V_{GS} - V_T)^2 \tag{3.14}$$

$$I_{out} = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS} - V_T)^2 \tag{3.15}$$

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{ref} \tag{3.16}$$

This shows that the output current is a scaled version of the reference current, where the scaling factor is determined by the ratio of the channel dimensions (W/L). Thus, if transistors M1 and M2 are identically sized, then the currents are also equal ($I_{ref} = I_{out}$) [29], [32].

3.7 Cascoding

As demonstrated in equation 3.10, increasing the output impedance directly increases the gain of the amplifier. One widely used method to achieve this is through cascode configurations. In a cascode structure, an additional transistor is stacked above the amplifying transistor, effectively increasing the output resistance by minimising the effect of channel length modulation.

This configuration not only improves gain, but also enhances bandwidth and reduces the Miller effect. Figure 3.7 illustrates a standard common source stage with a cascode transistor.

The gain of a cascoded amplifier stage can be approximated as follows:

$$A_v = \frac{\partial V_{DS}}{\partial V_{GS}} = \frac{\partial I}{\partial V_{in}} \frac{\partial V_{out}}{\partial I} = \frac{-g_{m1}}{g_{tot}} \tag{3.17}$$

$$\tag{3.18}$$

$$g_{tot} = g_L + g_{out} = g_L + \frac{g_{o1} g_{o2}}{g_{o1} + g_{o2} + g_{m2}} \tag{3.19}$$

After inserting 3.19 into 3.18 and assuming $g_L \approx 0$ and g_{m1} and $g_{m2} >> g_{o1}$ and g_{o1}:

$$A_v \approx \frac{g_{m1}(g_{o1} + g_{o2} + g_{m1})}{g_{o1} g_{o2}} \tag{3.20}$$

$$\approx \frac{g_{m1} g_{m2}}{g_{o1} g_{o2}} \tag{3.21}$$

Optimizing a cascode stage results in a large voltage gain over the cascode transistor's V_{DS} and a lower gain over the input transistor's V_{GS}, resulting in a lower input capacitance C_{in}, also known as the Miller effect [33].

3.8 Two-Stage Amplifier

Two-stage amplifier configurations are commonly used to achieve higher overall gain and improved output performance. The first stage is typically optimised for maximum voltage gain and consists of a differential pair with high transconductance, as seen previously. The second stage is designed to provide a large output voltage swing and sufficient drive capability for the subsequent load.

This second stage usually consists a p-type common source transistor acting as a current source, biased with a constant gate voltage. The bias current of this stage is generally higher than the tail current of the first stage, allowing for greater drive strength. As shown in Figure 3.8, the second stage typically does not include cascode devices, prioritising output swing over gain enhancement.

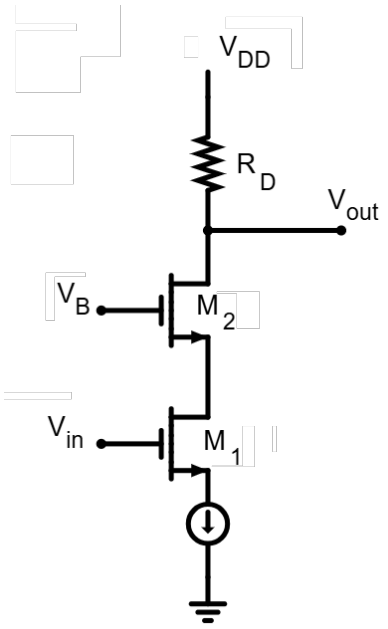


Figure 3.7: Common source stage with a cascode transistor.

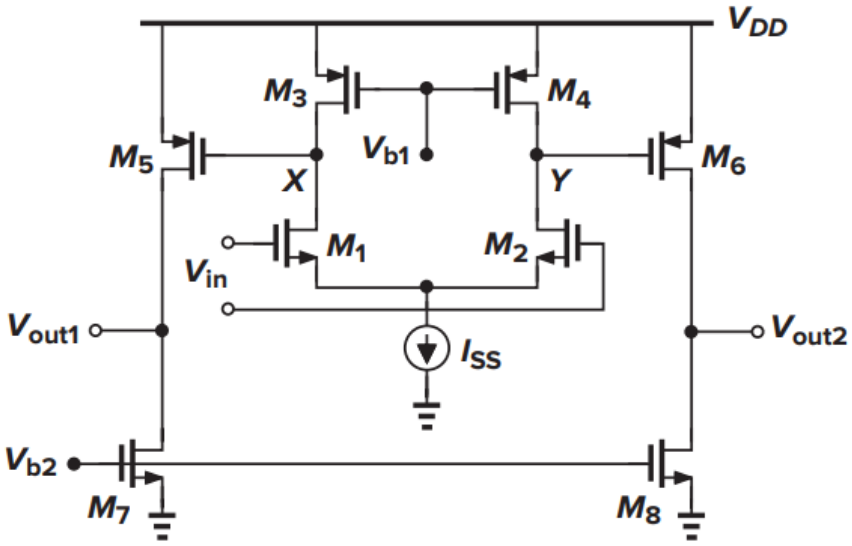


Figure 3.8: Typical two stage amplifier circuit. [29]

3.9 Common Mode Rejection Ratio

As explained before in section 3.1, the signal at the two input nodes will contain a common-mode and a differential-mode signal (V_{ICM} and V_{IDM}). An ideal fully differential amplifier will only amplify the difference between the two input nodes, which is V_{IDM}. Any non-ideal amplifier contains an undesirable differential component that is produced by the variations in V_{ICM}. This component is quantified by the common-mode rejection ratio (CMRR), which is defined as the ratio of the differential gain to the common-mode gain, defined in decibels (dB). In other words, it measures how well the amplifier amplifies the desired differential signal while rejecting the undesired common-mode signals [29].

$$CMRR = 20 \log_{10} \left(\frac{A_{\text{diff}}}{A_{\text{cm}}} \right) \tag{3.22}$$

Recommendations typically range from 85 to 120 dB [34], [35], [36]. In practice, CMRR is strongly affected by mismatches in transistor fabrication. An ideal fully differential amplifier with perfectly matched transistors would achieve an infinite CMRR. However, since this work is based exclusively on simulations under idealised conditions, the reported CMRR values will not be representative of a real-world implementation.

Chapter 4

Results and Discussion

4.1 Simulation Models

The research facility ES&S provided two different simulation models for the p-type and n-type LTPO TFTs. The first simulation model is based on an existing fabrication of LTPO. The second is based on realistic results of p-type LTPS and n-type a-IGZO TFTs, but has never been fabricated yet. This means that the performance of the second simulation model is only speculation. The first amplifier discussed in the following chapter is developed based on these first simulation models, and all the latter are based on the second simulation models.

4.2 Simulation Setup

All circuit characterisation was performed using the Cadence Virtuoso Spectre simulation environment. These simulations were designed to evaluate the amplifier's performance in both the frequency and time domains.

The frequency domain analysis is visualised through a bode plot, which highlights two primary performance metrics:

- **Magnitude Response:** The absolute gain of the amplifier expressed in decibels (dB) over a range of frequencies.
- **Phase Response:** The phase shift between the input and output signals, expressed in degrees (°), as a function of frequency.

The time domain performance was evaluated via transient simulations, providing the following information:

- **Output Waveform:** The time domain response of the amplifier output when subjected to an ECG input signal.
- **Signal Integrity:** Observations of how accurately the output replicates the input waveform, including any delay, distortion, or noise.

Additionally, the slew rate is determined by sending an impulse waveform at the positive input node and measuring the slope at the output.

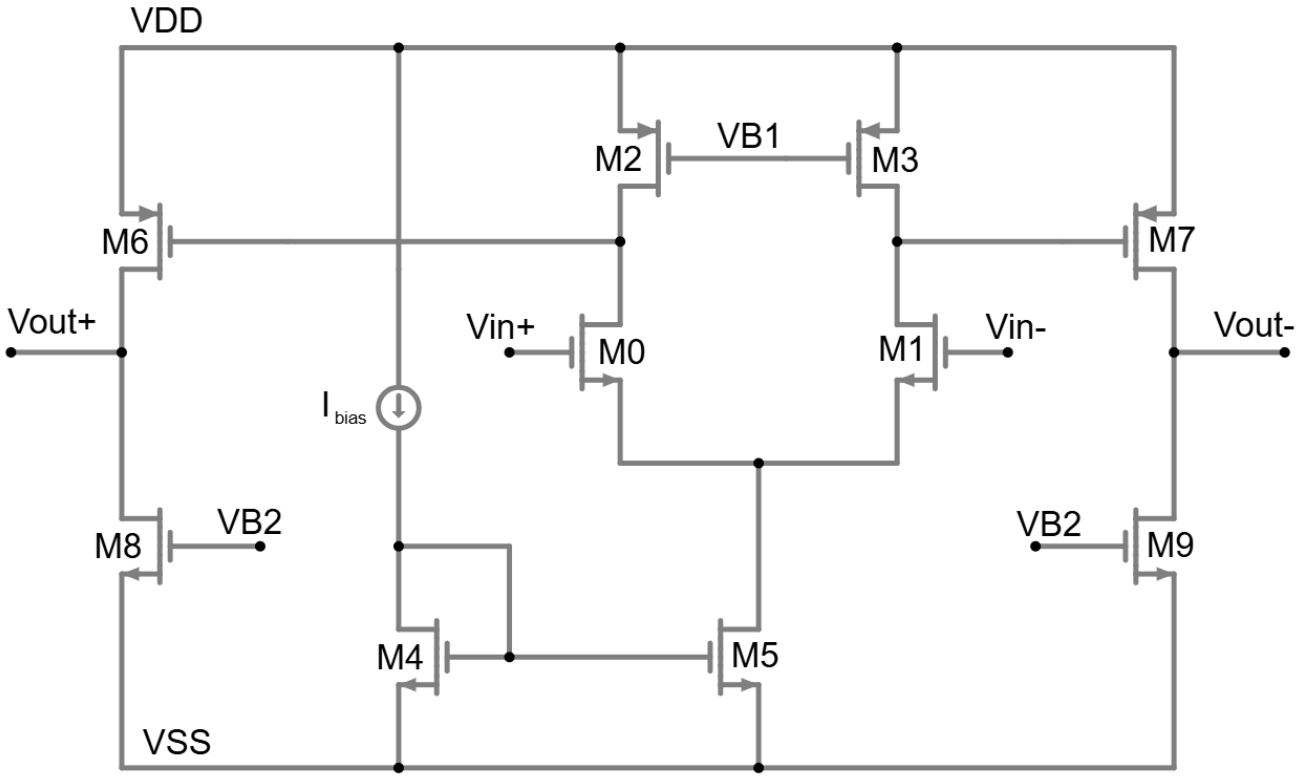


Figure 4.1: Two-stage amplifier in LTPO.

4.3 Simple Two-Stage amplifier

4.3.1 Circuit Design

Figure 4.1 illustrates the circuit schematic of the two-stage amplifier in LTPO. The amplifier contains four p-type TFTs and six n-type TFTs and can be subdivided into three parts:

- **M0,M1,M2,M3**: a differential pair input stage in common source configuration with a p-type load.
- **M4,M5**: a current mirror serving as an ideal current source.
- **M6,M7,M8,M9**: a common drain output stage.

The TFT dimensions and biasings are given in Table 4.1.

Transistors M0 and M1 recieve the input signals V_{in+} and V_{in-} respectively at their gates. Transistors M2 and M3 serve as p-type loads to increase the output impedance of the first stage. An ideal current source I_{bias} provides a constant current at the drain of M4 that is mirrored by M5 at the drain to produce a constant tail current. The p-type TFTs M6 and M7 at the second stage are placed in common drain configuration and amplify the signal a second time with higher driving capability. N-type transistors M8 and M9 serve as ideal current sources at the output stage.

Table 4.1: TFT dimensions and bias parameters of the amplifier of the two stage amplifier.

Transistor	Width [µm]	Length [µm]	Multiplier	Bias	Voltage [V]	Current [nA]
M0, M1	160.0	4.0	1	V_{B1}	-5.0	
M2, M3	5.0	40.0	1	V_{B2}	4.0	
M4, M5	160.0	0.8	16	I_{bias}		500
M6, M7	20.0	6.0	1			
M8, M9	20.0	6.0	1			

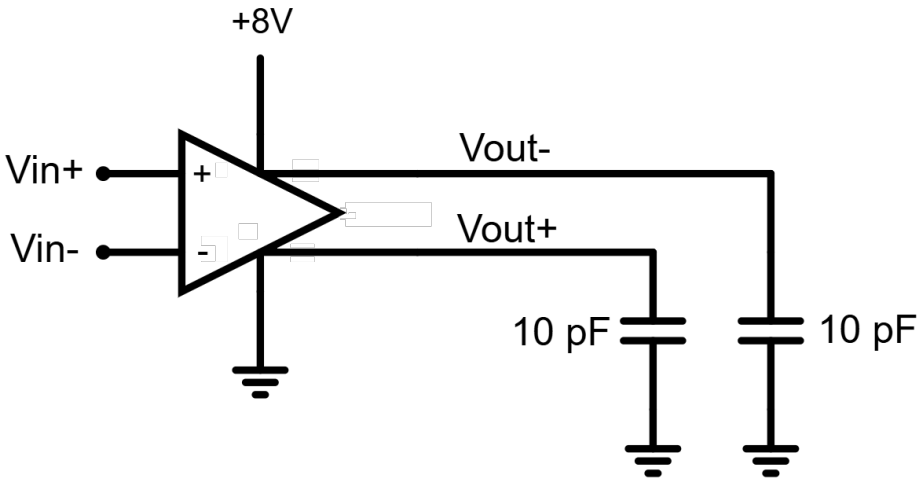


Figure 4.2: Open loop test bench used for the two stage amplifier.

4.3.2 Test Bench and Simulation Results

Figure 4.2 illustrates the test bench configuration used to characterise the open-loop gain, phase response, and transient behaviour. The amplifier operates on an 8 V supply voltage (V_{DD}). The input signals (V_{in+} and V_{in-}) are simulated representations of realistic positive and negative lead I ECG waveforms with a common-mode voltage of 4 V, corresponding to the midpoint between ground and V_{DD}. The amplifier is designed to drive a capacitive load of 10 pF at each output node.

Figure 4.3 displays the open-loop gain and phase shift of the output signal in a bode plot. The gain after the first amplification stage reaches 14.4 dB. The total low-frequency open-loop gain after the second stage is 33 dB. The -3 dB cut-off frequency is 610 Hz and the unitiy gain bandwidth (UGBW) is 29 kHz. This results in a phase margin of 94°. The slew rate is equal to 175 V/ms and is illustrated in Figure 4.5.

The transient response is shown in Figure 4.4, where the output signals operate around a common-mode voltage V_{OCM} of 3.5 V. The waveform in the transient response demonstrates excellent signal integrity of the ECG waveform at the output while amplifying the signal with a magnitude of approximately 45. A summary of the amplifier's performance parameters is provided in Table 4.2.

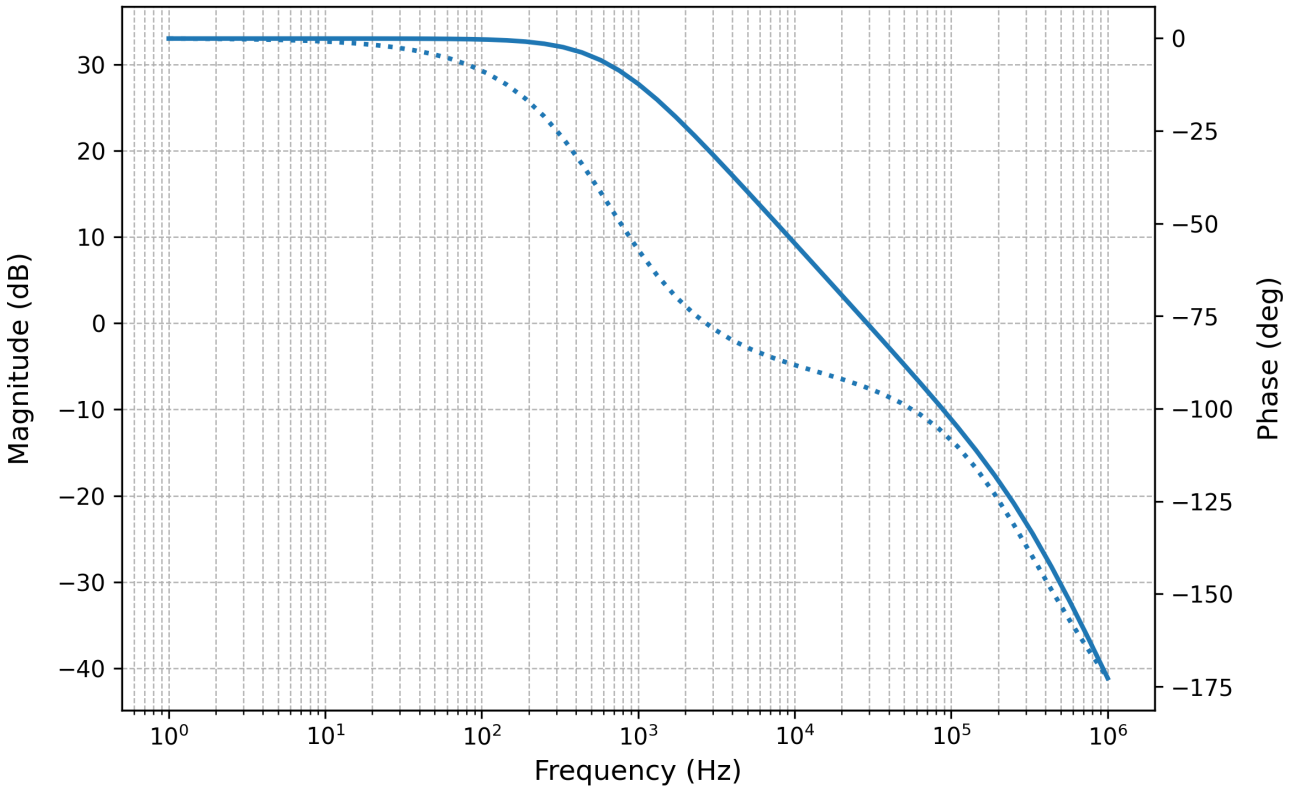


Figure 4.3: Bode plot of the open loop gain (solid line) and phase delay (dotted line) of the two stage amplifier.

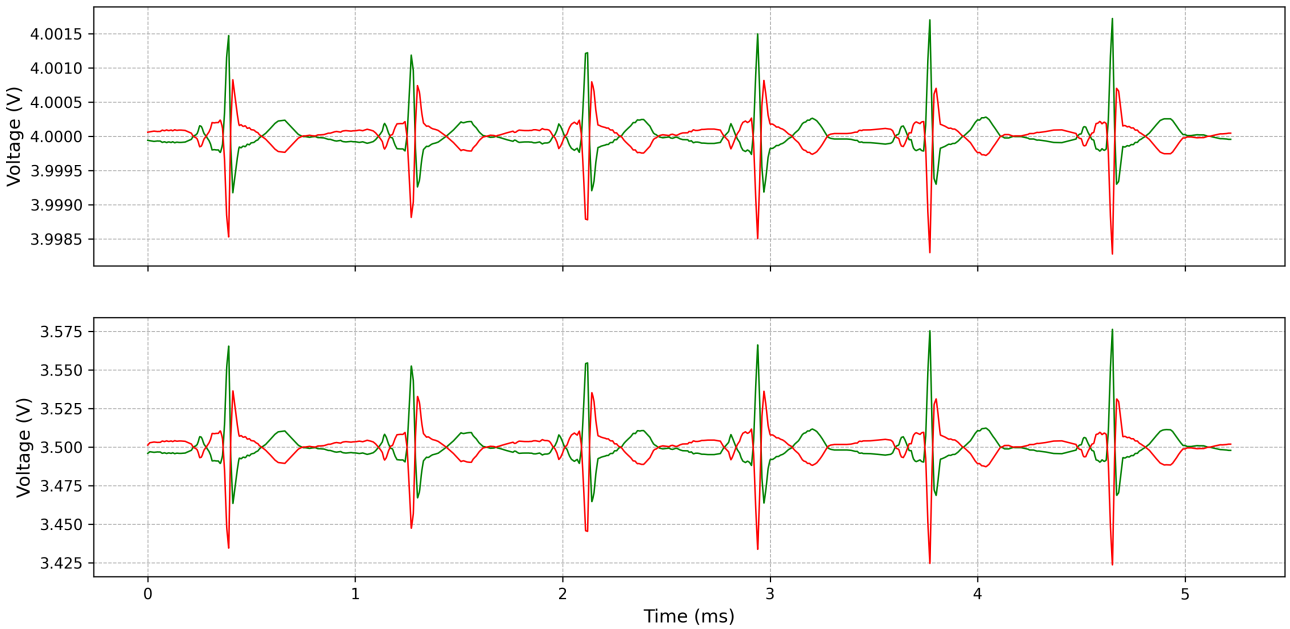


Figure 4.4: Transient response of the input (top) and output (bottom) signal of the two stage amplifier, with the positive nodes in green and negative nodes in red.

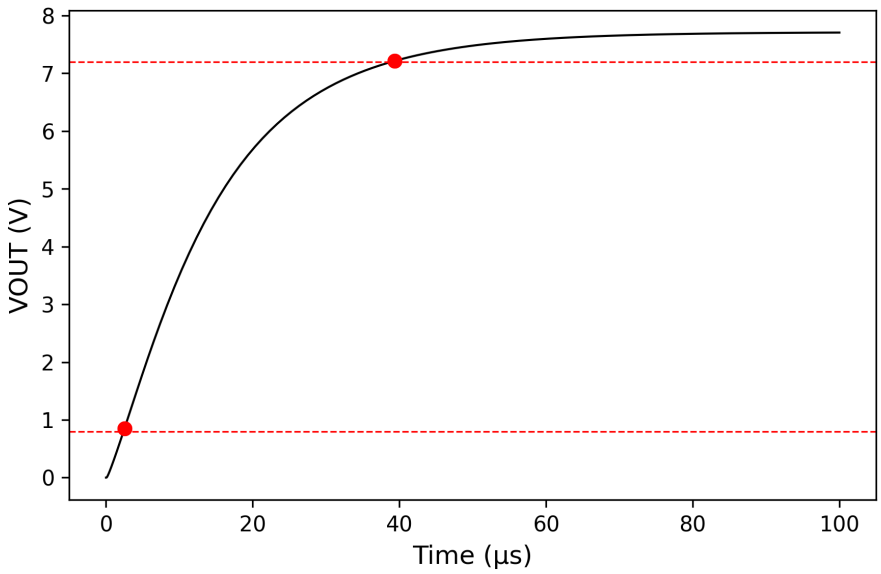


Figure 4.5: Slew rate of the two stage amplifier.

Table 4.2: Performance parameters of the two stage amplifier.

Parameter	Value
Open-loop gain (dB)	33
$f_{cut-off}$ (Hz)	600
UGBW (kHz)	29.2
PM (°)	93
V_{OCM} (V)	3.5
Power (µW)	7.34
SR (V/µs)	0.175
Approx. $V_{peak,AVG}$ (mV)	70

4.3.3 Discussion

The results at the output nodes of this amplifier are not sufficient for the requirements set. Mainly, the amplifier cannot provide enough open loop gain to achieve a reasonable resolution for a 16-bit ADC with a resolution of 122 µV when V_{ref} is equal to V_{DD} (8 V). This results in approximately 600 distinguishable data points between V_{OCM} and $V_{peak,AVG}$, failing to meet the amplification guidelines recommended by Texas Instruments (see Chapter 2). This low amplification, especially after the first stage, can be explained by the very low transconductance (g_m) of the n-type TFTs (see Chapter 3).

However, ignoring this lack of amplification, this amplifier proves to be very reliable. The phase margin of 93° ensures high stability even with a large system variability. The slew rate of 175 V/ms is more than sufficient for this application. Additionally, the cut-off frequency of 600 Hz and the UGBW of 29.2 kHz already provide a level of filtering on high-frequency noise without any active filters present. However, considering the very low average power consumption of 7.34 µW, this amplifier could still be viable in combination with a higher resolution ADC that consumes more power.

4.4 Current Mirror Based Amplifier

4.4.1 Circuit Design

Figure 4.6 illustrates the circuit schematic of an amplifier based on current mirror amplification. The amplifier consists of six p-type TFTs and ten n-type TFTs and can once again be subdivided into multiple parts:

- **M0, M1**: a differential pair input stage in common source configuration.
- **M2, M3**: a current mirror serving as an ideal tail current source.
- **M4, M5, M6, M7**: cascode transistors used to increase the output impedance in the first stage.
- **M8 ,M9, M10, M11**: p-type transistors in current mirror configuration.
- **M12, M13, M14, M15**: an n-type current mirror that serves as an ideal current source in the output stage.

The dimensions and biases of the TFT are given in Table 4.3.

Transistors M0 and M1 receive the input signals (V_{in+} and V_{in-}) at their respective gates. The ideal current source I_{B1} provides a constant current at the drain of M2 that is mirrored by M3 at the drain to produce a constant tail current. The n-type TFTs M4 and M5 and the p-type TFTs M6 and M7 are cascode transistors with a constant bias voltage at their gates to increase the output impedance of the first stage. The p-type transistors M8 to M11 form a current mirror configuration with deliberately chosen mismatched W/L ratios. This configuration scales the current flowing into the reference branch and replicates a proportionally larger current in the output branch. The remaining transistors M12 until M15, also in current mirror configuration, provide a constant current source at the output node.

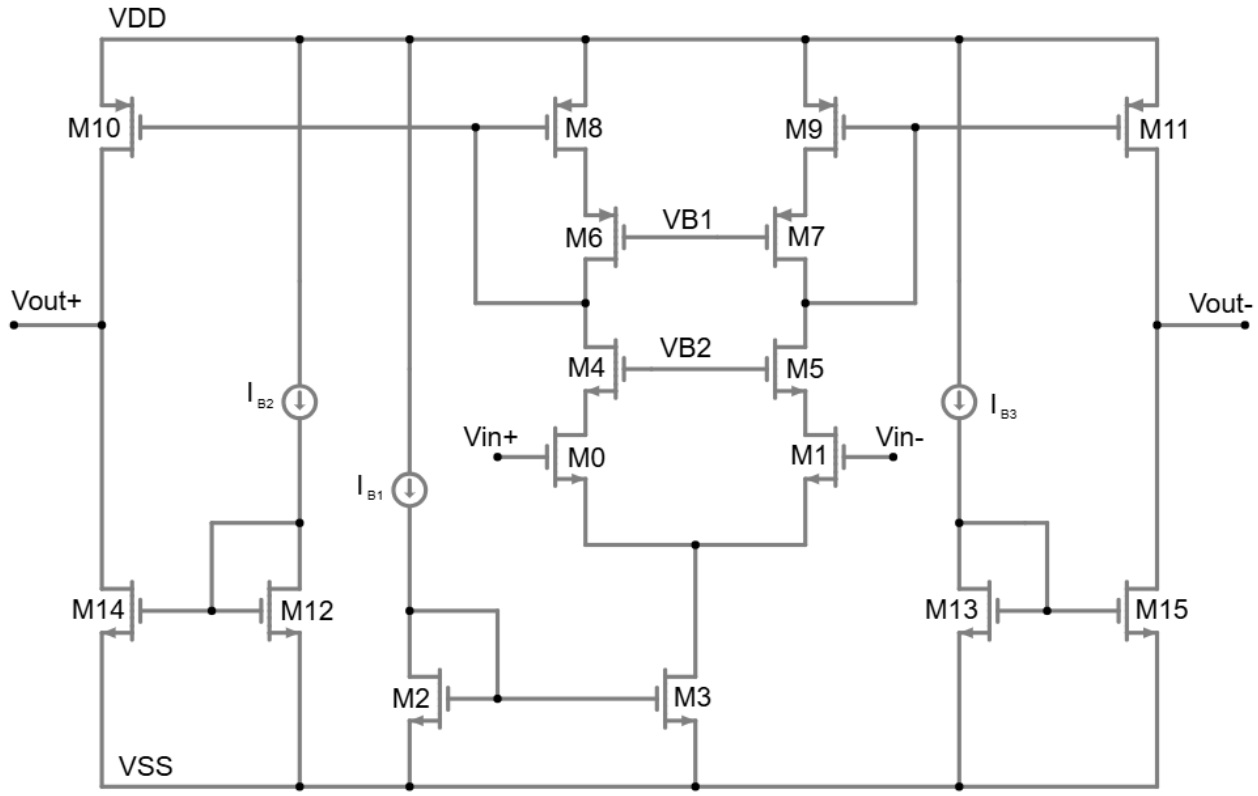


Figure 4.6: Circuit diagram of a current mirror based amplifier.

4.4.2 Test Bench and Simulation Results

Figure 4.7 illustrates the test bench configuration used to characterise the open-loop gain, phase response, and transient behaviour of the amplifier. The amplifier operates on a 3.00 V supply voltage (V_{DD}). The input signals V_{in+} and V_{in-} are simulated representations of realistic positive and negative Lead I ECG waveforms, with a common-mode voltage of 1.00 V. The amplifier is designed to drive a capacitive load of 10 pF at each output node.

Figure 4.8 displays the open-loop gain and phase shift of the output signal in a bode plot. The total low-frequency open-loop gain is 36.5 dB. The -3 dB cut-off frequency is 10.3 kHz and the UGBW is 700 kHz. This results in a phase margin of 67°.

The transient response is illustrated in Figure 4.9, where the output signals operate around a common-mode voltage V_{OCM} of 1.0 V. The waveform in the transient response demonstrates excellent signal integrity of the ECG waveform at the output while amplifying the signal with a magnitude of approximately 63x. A summary of the amplifier's performance parameters is provided in Table 4.4.

4.4.3 Discussion

Once again, this amplifier does not achieve the gain requirements set in order to achieve a sufficient amount of data points for a 16-bit ADC, with a resolution of 45.8 µV. This results in approximately 3,000 distinguishable data points between V_{OCM} and $V_{peak,AVG}$, which is again not enough for the recommended resolution by Texas Instruments (see Chapter 2).

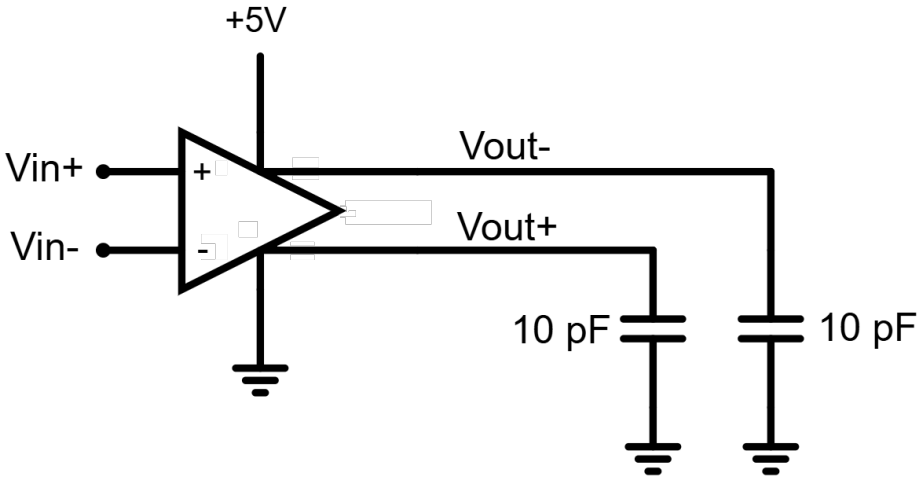


Figure 4.7: Open loop test bench of the current mirror amplifier.

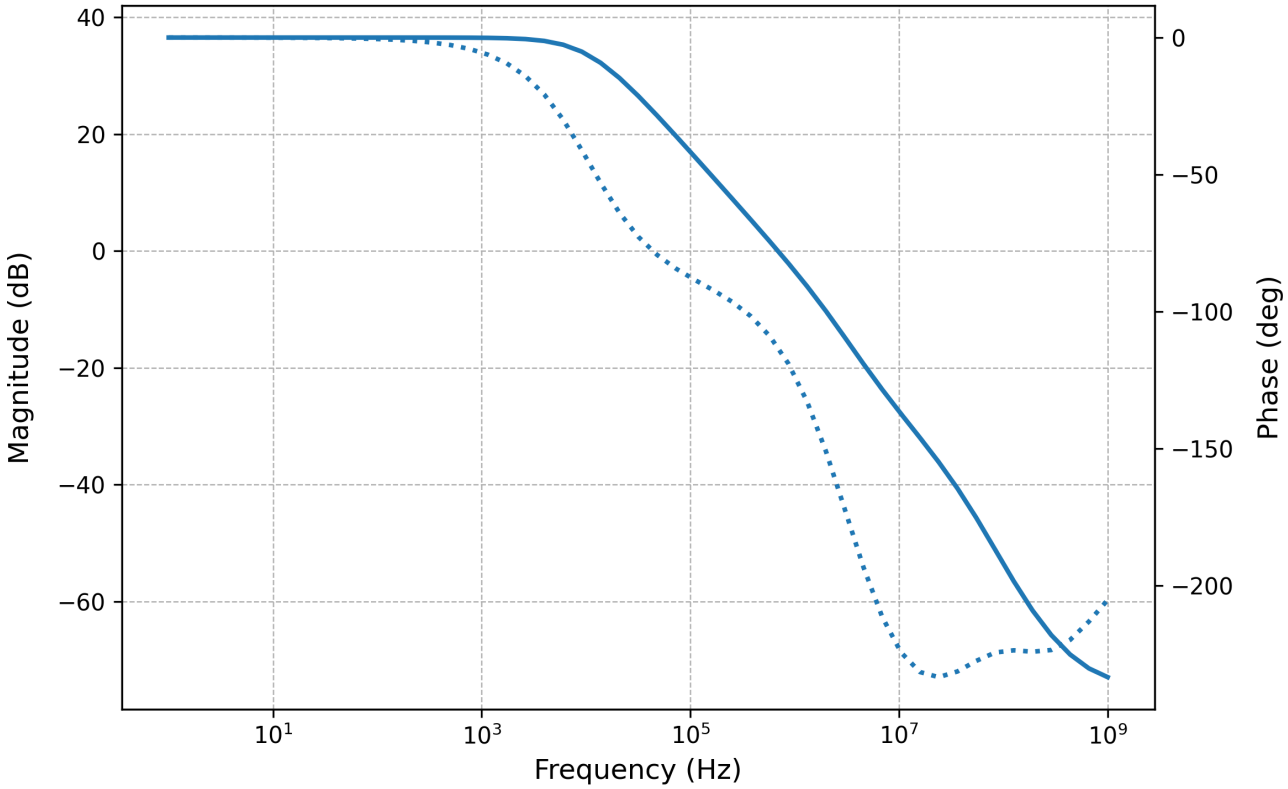


Figure 4.8: Bode plot of the open loop gain (solid line) and phase delay (dotted line) of the current mirror amplifier.

Table 4.3: TFT dimension and bias parameters of the current mirror amplifier.

Transistor	Width [µm]	Length [µm]	Multiplier	Bias	Voltage [V]	Current [µA]
M0, M1	30.0	1.2	4	V_{B1}	2.0	
M2, M3	24.0	1.2	1	V_{B2}	1.5	
M4, M5	5.0	0.8	1	I_{B1}		0.60
M6, M7	1.0	0.8	1	I_{B2}		1.00
M8, M9	2.4	1.2	1	I_{B3}		1.00
M10, M11	6.0	1.2	2			
M12, M13	2.0	0.8	1			
M14, M15	2.0	0.8	2			

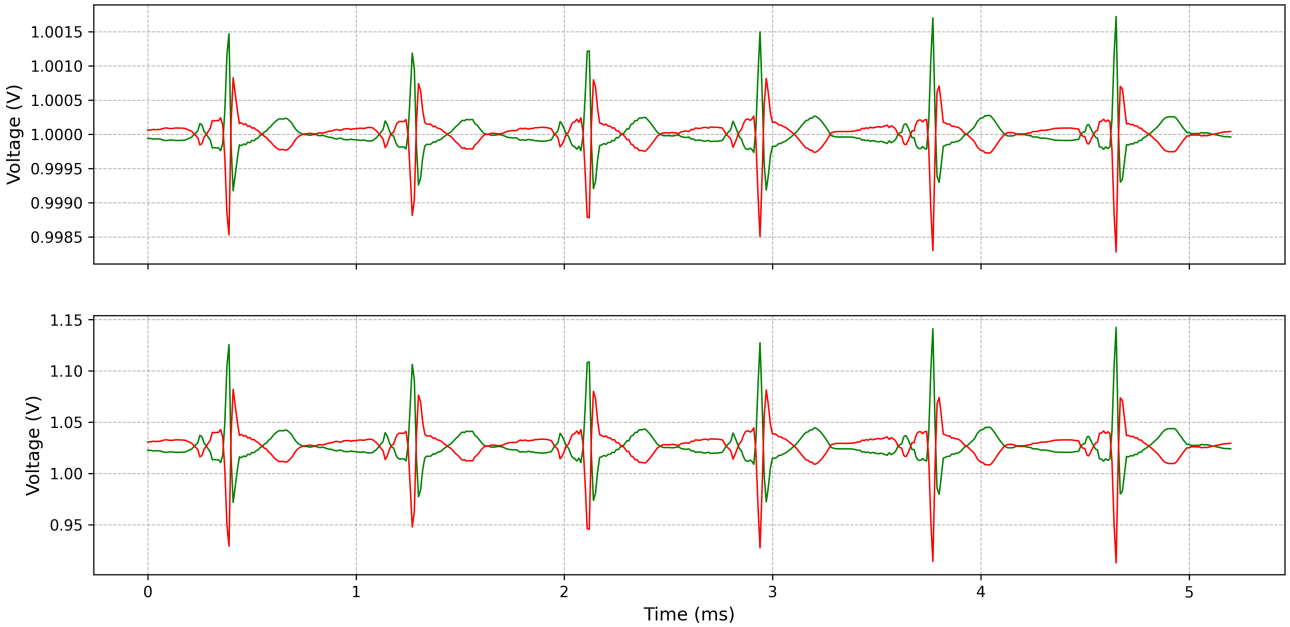


Figure 4.9: Transient response of the input (top) and output (bottom) signal of the current mirror amplifier, with the positive nodes in green and negative nodes in red.

However, ignoring this lack of amplification, this amplifier is shown to be very reliable with a phase margin of 67°. The high cut-off frequency of 10.3 kHz and the UGBW of 700 kHz indicate sufficient bandwidth headroom to accommodate an additional (third) amplification stage while still meeting minimum frequency requirements. This amplifier also consumes an average power of 8.63 µW when operating from a 3.00 V power supply, which aligns more with the low-power requirements typical for wearable and battery-powered ECG applications.

Table 4.4: Performance parameters of the current mirror amplifier.

Parameter	Value
Open-loop gain (dB)	36
f cut-off (Hz)	10.3k
UGBW (kHz)	700
PM (°)	67
V_{OCM} (V)	1.0
POWER (µW)	8.63
SR (V/µs)	-
Approx. $V_{peak,AVG}$ (mV)	140

4.5 High Gain Two Stage Amplifier

4.5.1 Circuit Design

Figure 4.10 illustrates the circuit schematic of a two-stage cascode amplifier. The amplifier consists of four p-type TFTs and ten n-type TFTs and can once again be subdivided into multiple parts:

- **M0, M1**: a differential pair input stage in common source configuration.
- **M2 ,M3**: p-type load transistors to increase the output impedance in the first stage.
- **M4, M5**: a current mirror serving as an ideal tail current source.
- **M6, M7**: n-type cascode transistors used to increase the output impedance in the first stage.
- **M8, M9**: p-type transistors in the output stage in common drain configuration.
- **M10, M11, M12, M13**: an n-type current mirror that serves as an ideal current source in the output stage.

The TFT dimensions and biasings are shown in Table 4.5.

Transistors M0 and M1 receive the input signals (V_{in+} and V_{in-}) at their respective gates. M2 and M3 are p-type load transistors in the differential pair stage. The ideal current source I_{B1} provides a constant current at the drain of M4 that is mirrored by M5 at the drain to produce a constant tail current. The n-type TFTs M6 and M7 and are cascode transistors with a constant bias voltage at their gates to increase the output impedance of the first stage. The p-type TFTs M6 and M7 in common drain configuration amplify the signal in the second stage. The remaining transistors M10 until M13 form a constant drive of current in the output stage as a current mirror with mismatched W/L ratios.

4.5.2 Test Bench and Simulation Results

This amplifier operates on the same 3.00 V supply as the previous design and is intended for identical conditions, including a 1.00 V input common-mode voltage and a 10 pF load capacitance.

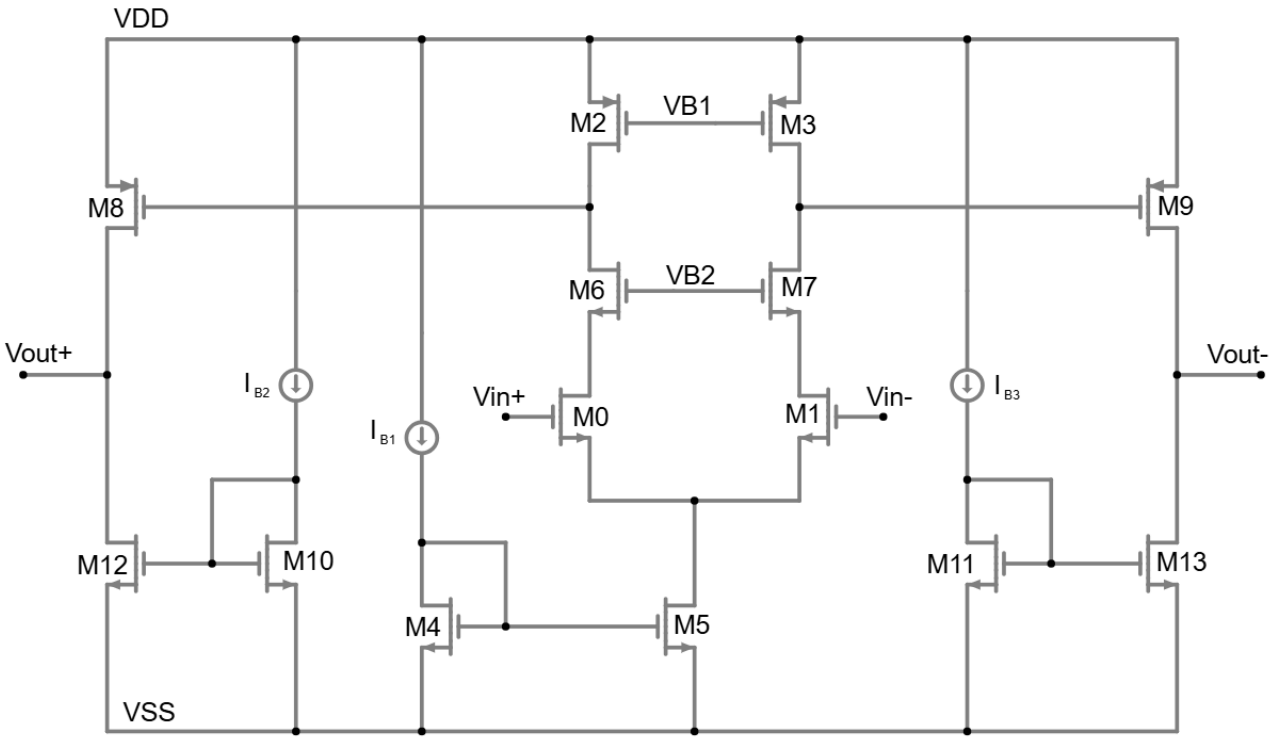


Figure 4.10: Circuit diagram the high gain two stage amplifier.

Table 4.5: TFT dimension and bias parameters of the current mirror amplifier.

Transistor	Width [µm]	Length [µm]	Multiplier	Bias	Voltage [V]	Current [µA]
M0, M1	6.0	1.2	1	V_{B1}	2.3	
M2, M3	2.0	0.8	1	V_{B2}	2.0	
M4, M5	24.0	1.2	1	I_{B1}		0.60
M6, M7	6.0	1.2	1	I_{B2}		1.00
M8, M9	1.0	1.1	1	I_{B3}		1.00
M10, M11	18.0	1.2	2			
M12, M13	13.0	0.8	2			

As a result, the same test bench setup is used to simulate its open-loop characteristics (see Figure 4.7).

Figure 4.11 displays the open-loop gain and phase shift of the output signal in a bode plot. The total low-frequency open loop gain is equal to 53.0 dB. The -3 dB cut-off frequency is 5.7 kHz and the UGBW is 1.6 MHz. The phase margin is equal to 30°.

The transient response is illustrated in Figure 4.12, where the output signals operate around a common-mode voltage V_{OCM} of 1.5 V. The waveform in the transient response demonstrates excellent signal integrity of the ECG waveform at the output while amplifying the signal with a magnitude of approximately 450x.

Figure 4.13 illustrates the amplifier with the addition of a negative feedback loop to the circuit. The feedback resistors R1 and R2 are 100 kΩ and 100 MΩ, respectively. The bode plot with closed-loop gain and phase shift is shown in Figure 4.14. This results in a closed-loop low

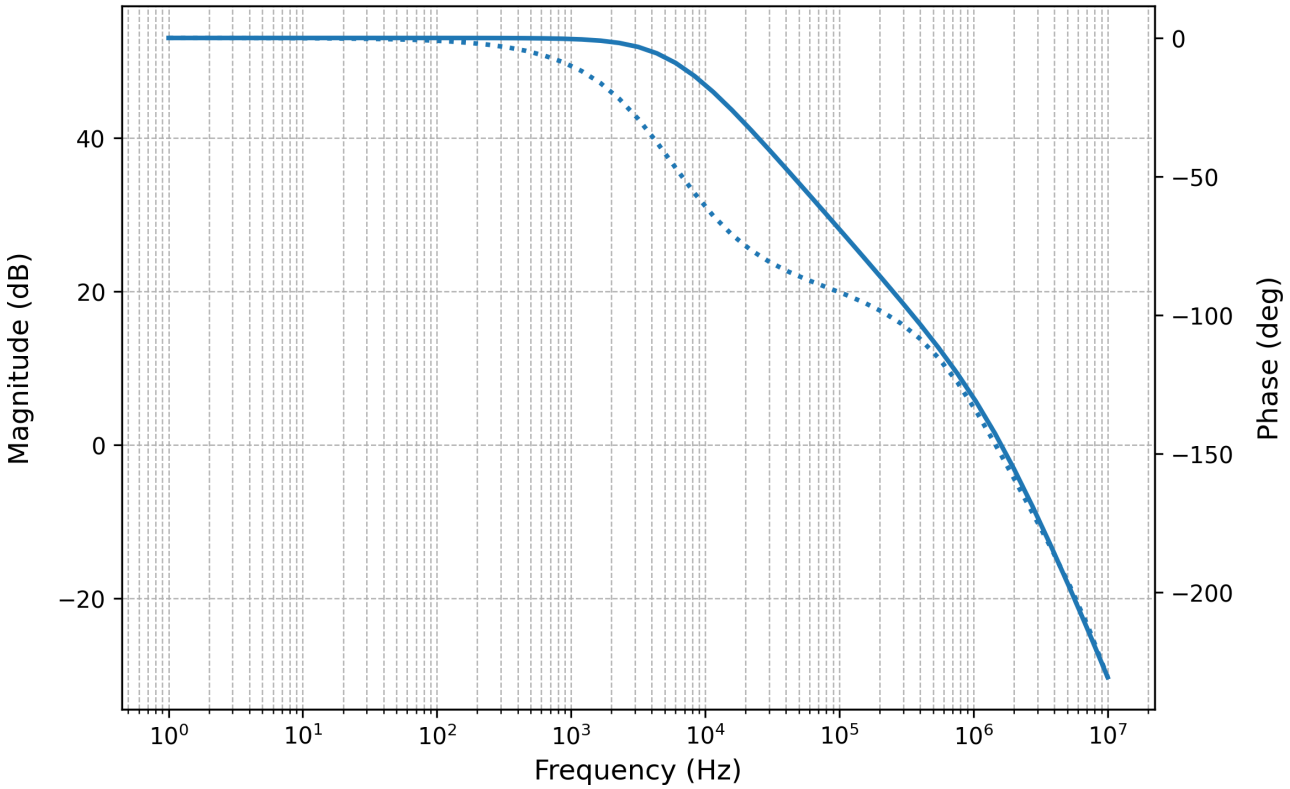


Figure 4.11: Bode plot of the open loop gain (solid line) and phase delay (dotted line) of the high gain two stage amplifier.

frequency gain of 49.6 dB, a -3 dB cut-off frequency of 8.5 kHz, a UGBW of 1.6 MHz, and a phase margin of 30°. A total summary of the amplifier's performance parameters in open and closed loop is provided in Table 4.6.

4.5.3 Discussion

Compared to the previous two designs, this amplifier demonstrates significantly superior performance. With an open-loop gain of 53 dB and a cut-off frequency of 5.7 kHz, it successfully amplifies the full spectrum of ECG signals with high signal integrity. Notably, it also achieves the lowest power consumption among all designs, operating at 6.4 µW on a 3 V power supply. The only limitation is the relatively low phase margin of 30°, which could affect stability under certain conditions.

Table 4.6: Performance parameters of the high gain two stage amplifier.

Parameter	Open Loop	Closed Loop
Gain (dB)	53.0	49.6
$f_{cut-off}$ (kHz)	5.7	8.5
UGBW (MHz)	1.6	1.6
PM (°)	30	30
V_{OCM} (V)	1.5	1.5
Power (µW)	6.4	6.4
SR (V/µs)	1.64	1.64
Approx. $V_{peak,AVG}$ (V)	0.70	0.50

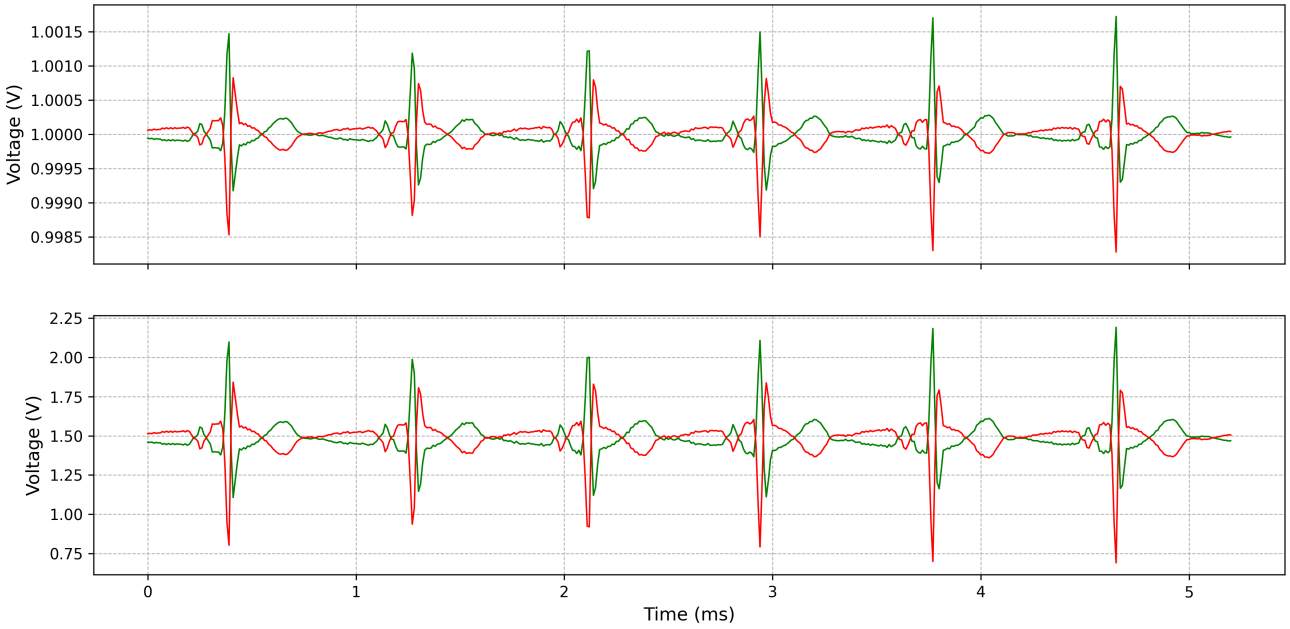


Figure 4.12: Transient response of the input and output (top) and output (bottom) signal of the high gain two stage amplifier, with the positive nodes in green and negative nodes in red.

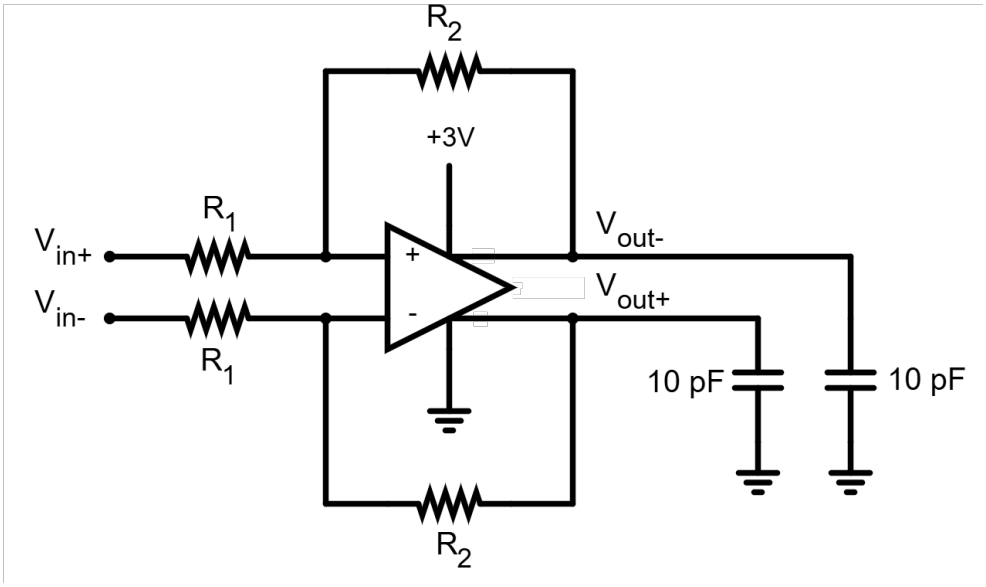


Figure 4.13: Test bench for the high gain two stage amplifier with negative feedback.

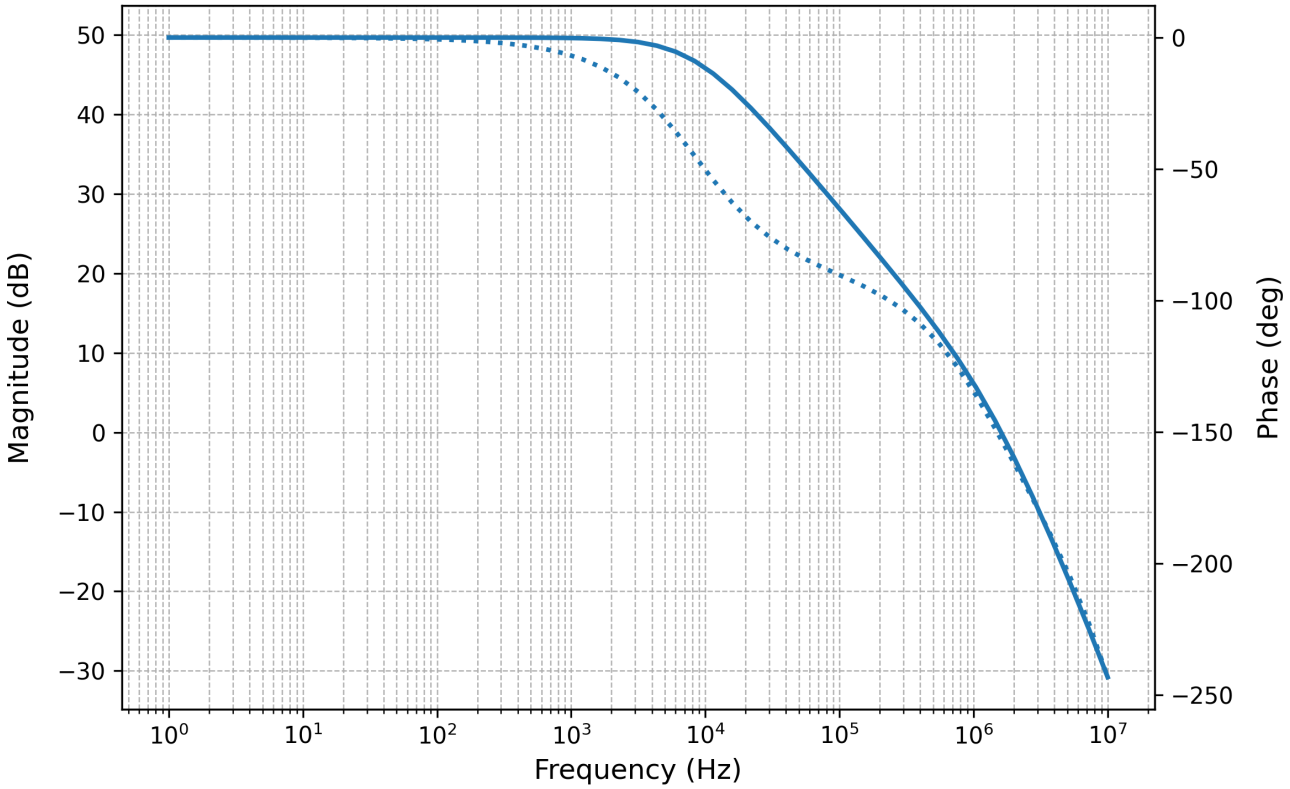


Figure 4.14: Bode plot of the closed loop gain (solid line) and phase delay (dotted line) of the high gain two stage amplifier.

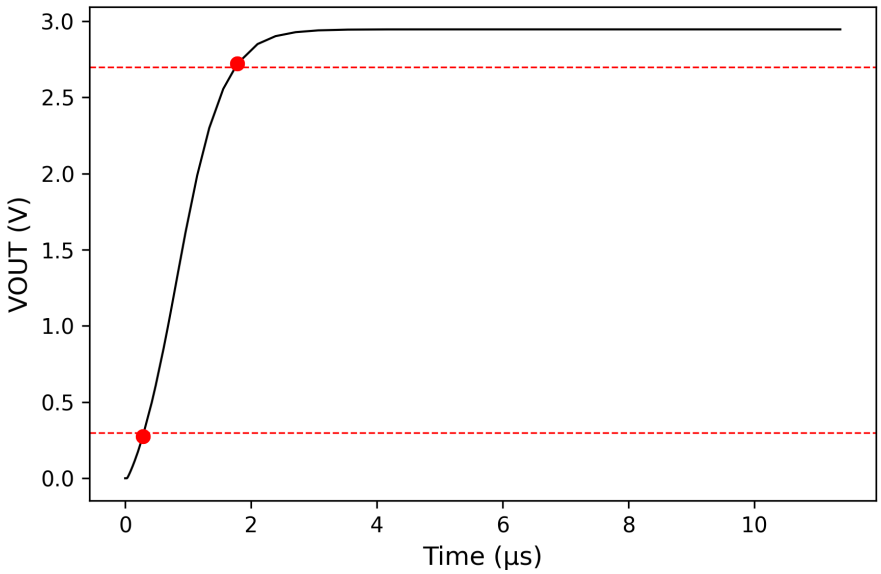


Figure 4.15: Slew rate simulation of the high gain two stage amplifier.

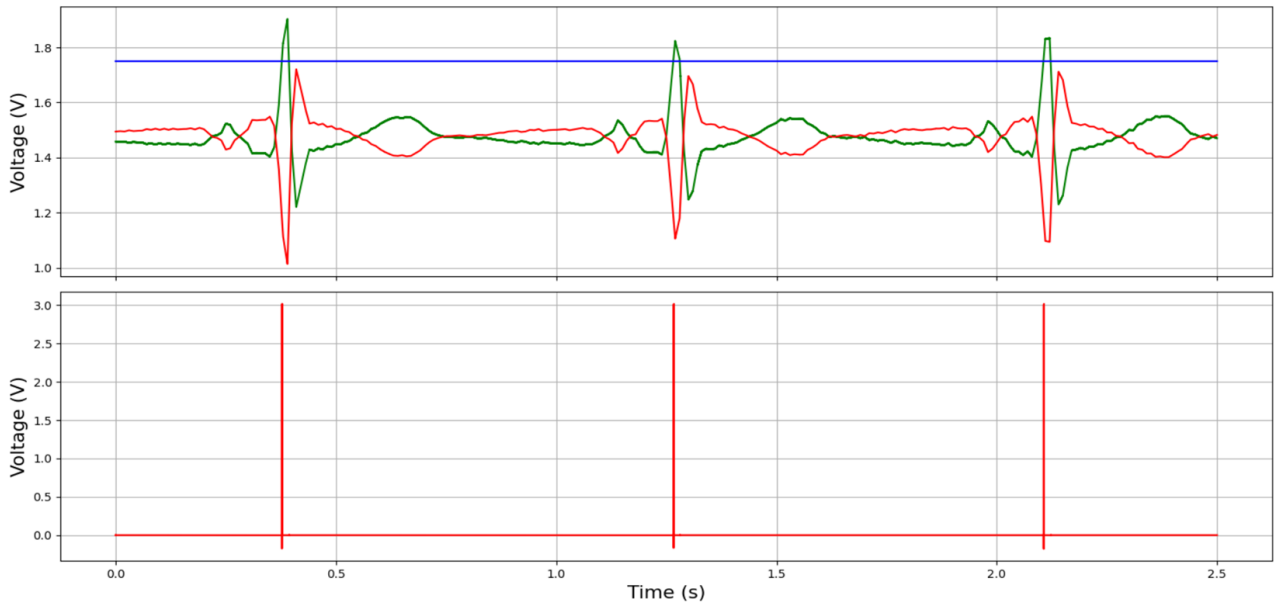


Figure 4.16: Output voltage signals of the AFE. Top: positive (green) and negative (red) output voltages, and the reference voltage (blue). Bottom: digital heartbeat pulse.

Upon introducing negative feedback, the amplifier's closed-loop gain is reduced to 49.6 dB. This results in an increase in cut-off frequency to 8.5 kHz, allowing more bandwidth. The phase margin stays the same at 30°. The lowering of the gain has caused an increase in bandwidth, enhancing overall stability and tolerance to system variability by making the low-frequency gain less dependent on the TFT's transconductance.

When this amplifier with negative feedback is paired with a 16-bit ADC (resolution: 45.8 µV), voltage peaks of approximately 0.50 V from V_{OCM} to $V_{peak,AVG}$ would result in around 11,000 distinguishable digital levels. These results show that this analogue amplifier can come within the same order of the recommended standard set by [11] (see Section 2.3.3).

4.6 Digital Signal Processing Unit

Typical AFEs incorporate a complete ADC that converts the analogue signal into a continuous stream of digital bits at the output. In its simplest form, such as a flash ADC [37], the architecture consists of an array of comparators with reference voltages that range from the lowest to the highest measurable voltage. The ADC first samples the analogue signal at fixed time intervals, defined by a constant sampling frequency. Each sampled value (still analogue) is then quantised to the nearest discrete level, as determined by the resolution of the ADC. Finally, this quantised level is encoded into its corresponding digital representation [38].

The digital component of the AFE in this thesis essentially compromises itself to a single comparator level of such a flash ADC. It compares the positive output node of the analogue amplifier with a single constant reference voltage, specifically chosen so that the signal only exceeds this value once every cycle, which is during the R wave peak of the ECG. The end result is a signal that returns a digital '1' once every heartbeat cycle, as can be seen in Figure 4.16. All transistor gates in the digital component of the AFE have a width of 1 µm and a length of 800 nm.

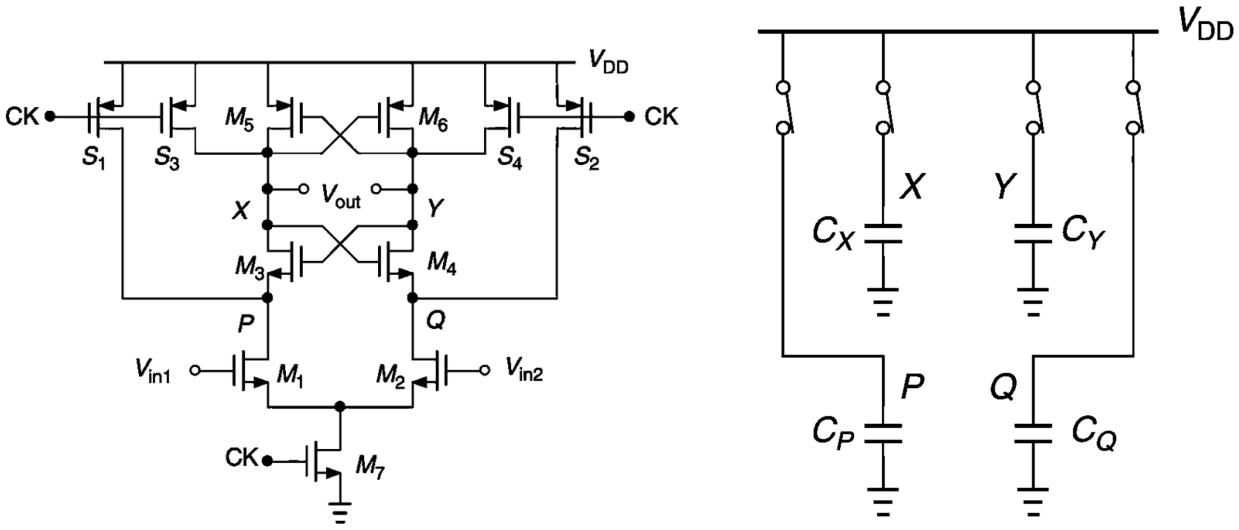


Figure 4.17: StrongARM latch (a) circuit and (b) its equivalent circuit in the reset stage. [40]

4.6.1 StrongARM Latch

The comparator is based on a StrongARM latch topology [39]. This comparator is known to have low static power consumption, rail-to-rail output, speed, and input sensitivity [23]. This serves as an ideal option for a portable and low-gain design. Figure 4.17a illustrates the StrongARM latch circuit with five n-type and six p-type transistors. The circuit consists of two input nodes (V_{in1} and V_{in2}) and two output nodes (X and Y). An additional clock input that is connected to five of the eleven transistors. Four of these serve as p-type precharge switches.

The operation of the StrongARM latch can be divided into four stages.

Stage 1: When CK is low, transistors M_1 and M_2 are off, and nodes P, Q, X, and Y are precharged to V_{DD} via the internal capacitances of the transistors. The circuit becomes the equivalent seen in Figure 4.17b consisting of four capacitances.

Stage 2: When CK transitions high, switches S_{1-4} turn off and M_7 turns on, enabling M_1 and M_2. The current flowing from the charged capacitors C_P and C_Q through M_1 and M_2 is proportional to their respective input voltages V_{in1} and V_{in2}.

Stage 3: When V_P and V_Q drop below $V_{DD} - V_{thN}$, transistors M_3 and V_4 turn on, allowing additional current flow from C_X and C_Y.

Stage 4: Now imagine $V_{in1} > V_{in2}$: this means M_1 conducts more current, causing V_X to drop faster than V_Y. When V_X reaches $V_{DD} - V_{thP}$, M_5 turns on, triggering positive feedback: V_X is rapidly pulled up to V_{DD} and V_Y is driven to ground. The latch output is then resolved as a digital '1' at node X and a digital '0' at node Y.

A more elaborate explanation of the process can be found in [40].

Connecting the positive output node of the amplifier to a constant reference voltage forms a comparator that produces a high output for 50% of the clock cycle. By adding an SR latch at the output, as shown in Figure 4.18, the signal is held constant for the entire clock cycle. The output of the StrongARM circuit can be seen in Figure 4.19. The top waveform illustrates the

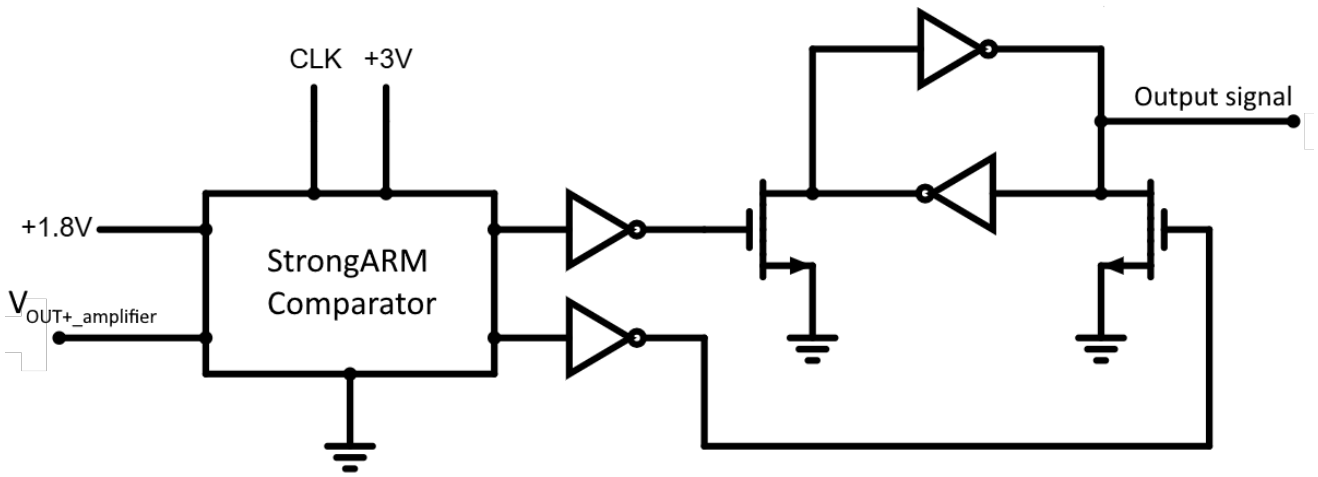


Figure 4.18: The StrongARM latch followed by the SR latch.

comparator's input signals, focusing on the R-wave of the ECG. with the positive and negative inputs relative to a fixed reference voltage. The middle waveform corresponds to the output of the strongARM comparator, while the bottom waveform represents the digital signal after processing by the SR latch, producing a stable heartbeat pulse.

4.6.2 Edge detection

The previously showcased circuit results in a constant digital '1' as long as the ECG exceeds the reference voltage. This is ideal as part of an ADC circuit. However, since this AFE only contains one comparator, it will serve a slightly different purpose: a circuit that sends a single pulse once every heartbeat, which could then be used externally to measure the patient's heart rate or heart rate variation (HRV).

The addition of an edge detection circuit can resolve this issue, as the one shown in Figure 4.20, containing eight NAND gates, one AND gate, and two inverters. The circuit is based on a master-slave D flip-flop, followed by an additional AND gate. The D flip-flop follows the input signal after the next negative clock edge. The input signal gets piped through to the AND gate, resulting in a single pulse at the output signal, as can be seen in the bottom graph of Figure 4.16. The circuit now returns a digital '1' once every heartbeat that never lasts longer than a single clock period.

4.7 Complete AFE

4.7.1 Circuit

The complete AFE circuit is illustrated in Figure 4.21, comprising, in this order, the analogue amplifier, StrongARM comparator, RS latch, and edge detector. All components operate from a 3 V supply voltage.

The AFE provides three outputs:

- Two amplified differential signals (V_{out+} and V_{out-}), that preserve high signal integrity and

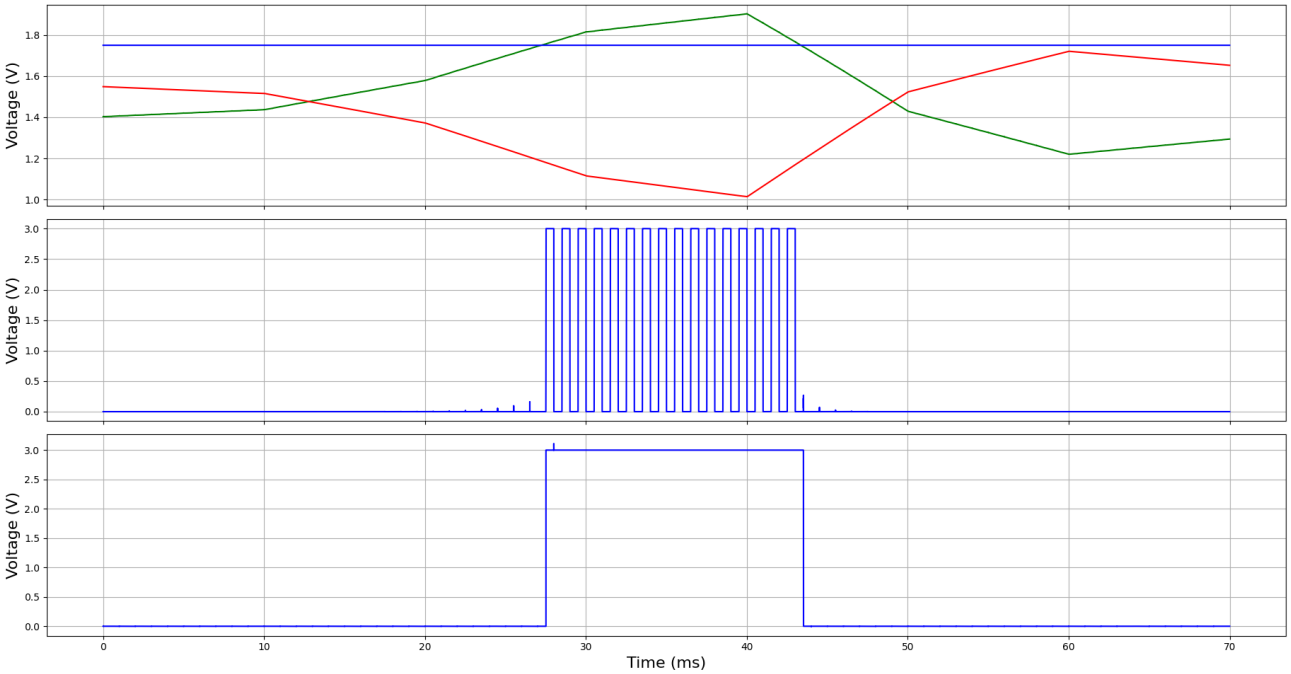


Figure 4.19: Output signals of the AFE during heartbeat detection. Top: positive (green) and negative (red) input voltages of the comparator and its reference voltage (blue). Middle: output of the StrongARM comparator. Bottom: output signal after the SR latch.

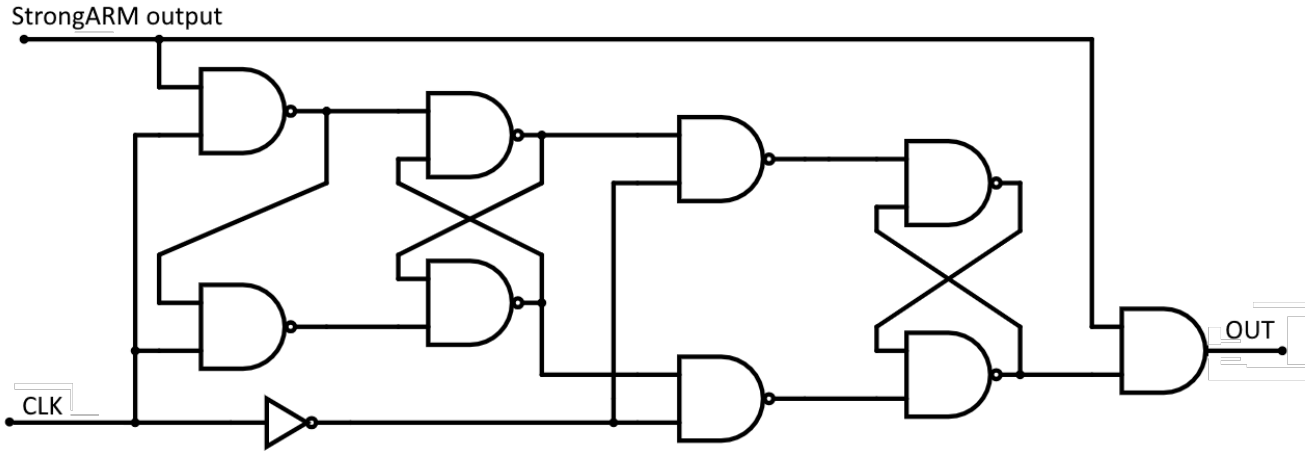


Figure 4.20: Edge detector circuit.

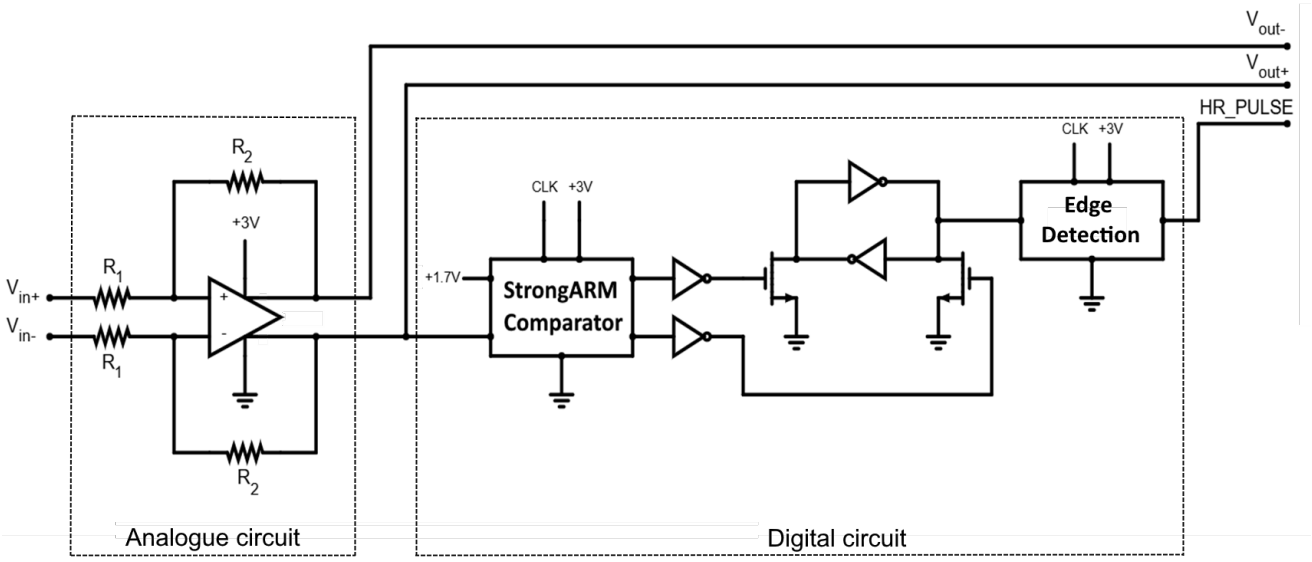


Figure 4.21: Full circuit diagram of the AFE.

provide sufficient amplification of the ECG waveform.

- The digital pulse signal that indicates heartbeat detection in real time for immediate heart rate monitoring.

Figure 4.22 presents the results of a 2.5 s ECG simulation, which contains three heartbeat cycles. The top plot illustrates the amplified positive and negative signals, and the bottom plot illustrates the digital heartbeat pulse.

4.7.2 Clock Frequency and Power Consumption

All the previous simulated results have utilised a clock frequency of 1.00 kHz. This AFE consumes an average total power of 6.8 µW, with the analogue amplifier of Section 4.5 accounting for approximately 6.4 µW. This indicates that the digital circuit consumes on average approximately 0.4 µW.

Figure 4.23 shows the ECG and power consumption in the region around the R-wave. The graph shows distinct peaks at each clock edge, reaching up to 60 µW. At the transitions of the StrongARM output (see Figure 4.19), the peaks rise to a maximum of 142 µW, with intermediate peaks of up to 80 µW occurring between these events. An increase in clock frequency to 10.0 kHz (third plot) results in an increase in power consumption to 8.0 µW. Although each individual spike in power consumption is slightly lower, the 10x increase in frequency increases power consumption by approximately 1.6 µW. Subsequently, decreasing the clock frequency to 250 Hz (fourth plot) results in a total power consumption of approximately 6.7 µW.

These results indicate that the power consumption of the digital signal processing unit rises exponentially with increasing clock frequency. Depending on the application's specific performance and power constraints, the clock frequency can be optimised to achieve the desired balance between accuracy and efficiency. For accurate HRV measurement, a sampling rate between 250 Hz and 500 Hz is sufficient [41], [42].

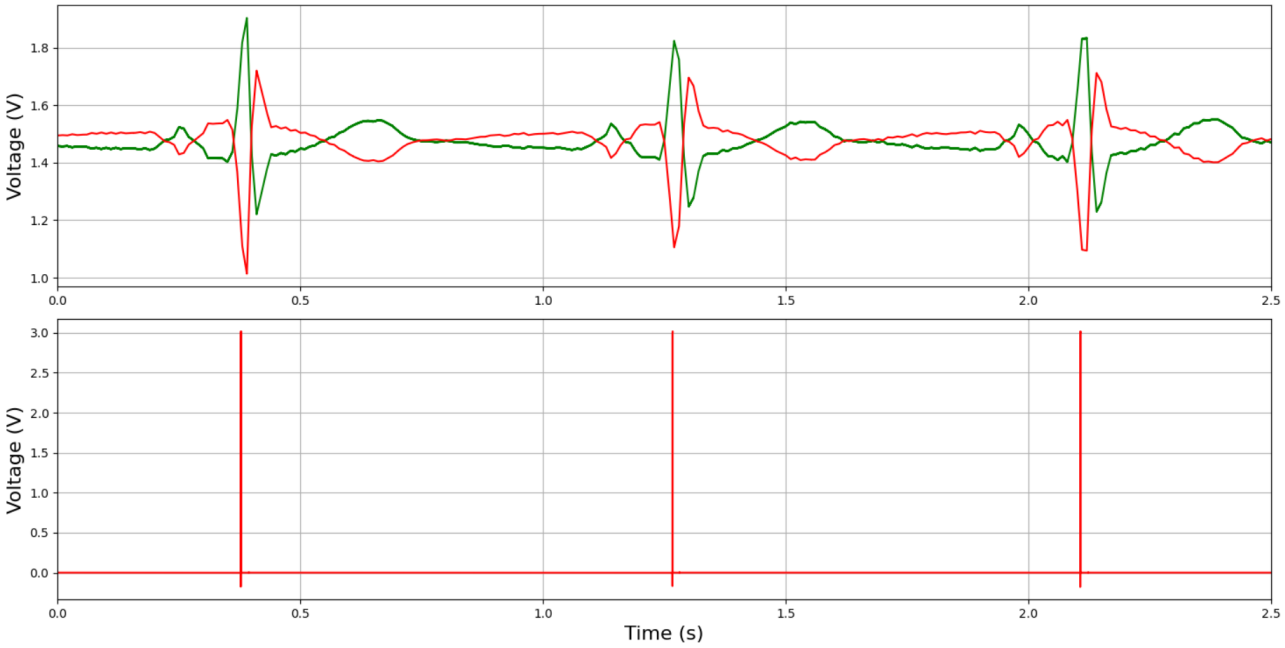


Figure 4.22: Output signals of the AFE. Top: V_{out+} and V_{out-}. Bottom: Digital heartbeat pulse.

4.8 Comparison to Other Work

This section compares the results obtained in this work with both prior LTPO research and other state-of-the-art TFT technologies. Table 4.7 summarises the key performance parameters of the three analogue amplifiers developed in this thesis, alongside those of a previously reported LTPO operational amplifier (see Section 2.2.4) and other TFT-based analogue amplifiers. The latter include designs optimised for ECG signal acquisition as well as amplifiers developed for general research purposes. The results demonstrate competitive performance across all evaluated parameters. When compared to the other LTPO amplifier, the power consumption is approximately 99% less on a similar amplification and a bandwidth more specifically designed for ECG.

A direct comparison of the DSP unit is challenging due to its specific circuit architecture. Nevertheless, it can be compared to the 1-bit ALU described in Section 2.2.3. The ALU comprises 99 transistors, whereas the DSP unit in this work contains 60 transistors. Operating from a 15.0 V supply, the ALU utilises six different clock frequencies ranging from 25 Hz to 1.00 kHz. Finally, the results show great performance in power consumption, as the ALU consumes 119.9 µW, compared to 0.4 µW at 1 kHz for the DSP unit presented in this thesis.

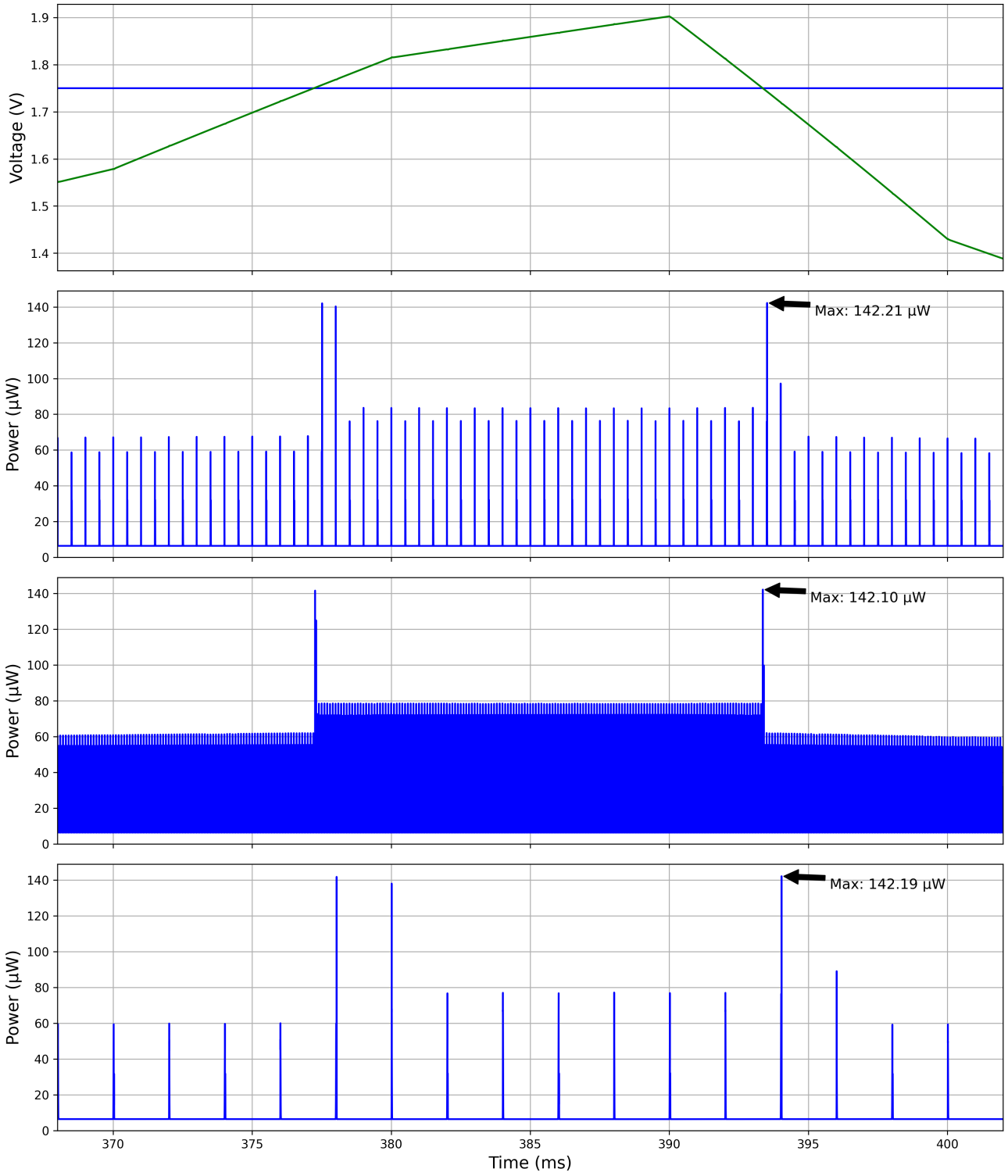


Figure 4.23: Top plot: ECG signal around the R-wave region and a 1.75 V reference voltage. Second plot: Power consumption measured with a 1 kHz clock frequency. Third plot: Power consumption measured with a 10 kHz clock frequency. Fourth plot: Power consumption measured with a 250 Hz clock frequency.

Table 4.7: Comparison of this work with other state-of-the-art TFT amplifiers.

	This work			State-of-the-Art				
	Amplifier I	Amplifier III	Amplifier II	[13]	[43]	[44]	[45]	[46]
Technology	LTPO	LTPO	LTPO	LTPO	a-IGZO	a-IGZO	LTPS	a-IGZO
Implementation	ECG	ECG	ECG	Research	Research	ECG	Research	ECG
No.of TFTs	10	16	14	13	19	22	29	18
Gain (dB)	33	36.0	49.6	50.7	23.5	30	64.2	43.5
$f_{cut-off}$ (kHz)	0.6	10	8.5	200	500	0.15	0.3	0.4-2.1
UGBW (MHz)	0.292	0.70	1.6	7.0	2.37	0.0055	0.2	0.29
PM (°)	93	67	30	93	102	-	40	58
Slew rate (V/µs)	0.175	-	1.64	22.7	2.1	-	-	-
Supply voltage (V)	8	3	3	±20	±10	20	6	15
Power (µW)	7.34	8.63	6.40	600	51,000	0.4	600	200

Chapter 5

Conclusion

5.1 Conclusion

This thesis has conducted research towards a fully flexible and wearable AFE for ECG in LTPO TFT technology by developing an analogue amplifier and a digital signal processing unit. Three analogue amplifiers have been developed based on two different simulation models. One of which is based on realistic LTPO TFTs, and the other on hypothetical results which are based on the p-type and n-type performance characteristics.

Firstly, a two-stage amplifier was developed based on the realistic simulation models. This resulted in an amplifier consisting of 10 TFTs, with a gain of 33 dB and a cut-off frequency of 600 Hz. The design proves to be very power efficient and reliable with a phase margin of 93° and a power consumption of 7.34 µW over a supply voltage of 8 V.

Secondly, based on the hypothetical simulation models, a two stage amplifier with implemented negative feedback was developed. This design consists of 14 TFTs, and reaches 49.6 dB with a cut-off frequency of 8.5 kHz. This circuit operates on a 3 V supply voltage and consumes 6.40 µW of power. These results give a high amplification and appropriate bandwidth at a very low power consumption relative to other implementations. However, the low phase margin of 30° can result in low stability when implemented in a real circuit.

Lastly, a DSP unit was developed to register the heartbeat of the patient by comparing the output signal of the analogue amplifier to a constant reference voltage. The comparator is based on the StrongARM latch topology, followed by a master-slave D flip-flop edge detector. The result is a single digital pulse once every heartbeat cycle. The DSP circuit operates on the same 3 V power supply and consumes 0.4 µW at 1 kHz.

After comparing the results to other state-of-the-art TFT implementations, they highlight the strong potential of LTPO TFT technology for reliable, low-power applications, thereby expanding its applicability in both analogue and digital circuit design. In particular, the implementation of an AFE for ECG signals demonstrates the feasibility of fully flexible, reliable, and long-lasting healthcare devices based on TFT technology.

5.2 Improvements

This thesis did not research the effects of noise on the system, nor did it perform a Monte Carlo analysis. Two vital steps towards the realisation of an analogue electrical circuit. Furthermore, the circuit does not contain any filter components that are usually present in AFEs. As for the ditital part of the AFE, which is a simplified version of a 1-bit ADC, no analysis was performed on the fall and rise time of the ADC, nor on the effect of the TFT sizings.

Additionally, the digital output signal of the ADC can be used to measure the time interval of the patient's heartbeat, which can also be realised in LTPO technology. An example of such a circuit was designed, and can be found in Appendix A. The circuit is able to count up to 2048 ms, equivalent to a heartbeat of approximately 30 BPM, and will send out the measured period since the previous heartbeat detection as an 11-bit binary.

5.3 Future Work

The findings presented in this thesis are entirely derived from simulations. In particular, the models used for the second and third amplifiers, as well as for the digital signal processing unit, are completely speculative and theoretical. The logical next step in this study would be to develop a layout and realise the circuits on a flexible substrate. The fabrication process will likely lead to some degradation in performance across all parameters and introduce additional noise. This will however enable more accurate measurements and additional data which could not be evaluated in the current work, e.g. the CMRR and signal-to-noise ratio on the analogue amplifier.

Only then could the outcome of this thesis prove to be valuable in the research towards implementations of LTPO in complex analogue and digital electrical circuit design.

Acknowledgements

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Bibliography

[1] A. J. Bandodkar and J. Wang, "Non-invasive wearable electrochemical sensors: a review," *Trends in Biotechnology*, vol. 32, no. 7, pp. 363–371, 7 2014. [Online]. Available: https://doi.org/10.1016/j.tibtech.2014.04.005

[2] D. H. Kim, R. Ghaffari, N. Lu, and J. A. Rogers, "Flexible and stretchable electronics for biointegrated devices," *Annual Review of Biomedical Engineering*, vol. 14, no. Volume 14, 2012, pp. 113–128, 8 2012. [Online]. Available: https://www.annualreviews.org/content/journals/10.1146/annurev-bioeng-071811-150018

[3] S. Xu, Y. Zhang, L. Jia, K. E. Mathewson, K.-I. Jang, J. Kim, H. Fu, X. Huang, P. Chava, R. Wang, S. Bhole, L. Wang, Y. J. Na, Y. Guan, M. Flavin, Z. Han, Y. Huang, and J. A. Rogers, "Soft Microfluidic Assemblies of Sensors, Circuits, and Radios for the Skin," *Science*, vol. 344, no. 6179, pp. 70–74, 2014. [Online]. Available: https://www.science.org/doi/abs/10.1126/science.1250169

[4] S. Imani, A. J. Bandodkar, A. M. Mohan, R. Kumar, S. Yu, J. Wang, and P. P. Mercier, "A wearable chemical–electrophysiological hybrid biosensing system for real-time health and fitness monitoring," *Nature Communications 2016 7:1*, vol. 7, no. 1, pp. 1–7, 5 2016. [Online]. Available: https://www.nature.com/articles/ncomms11650

[5] T. K. Chang, C. W. Lin, and S. Chang, "39-3: Invited Paper: LTPO TFT Technology for AMOLEDs†," *SID Symposium Digest of Technical Papers*, vol. 50, no. 1, pp. 545–548, 6 2019.

[6] H. Luo, S. Wang, J. Kang, Y. M. Wang, J. Zhao, T. Tsong, P. Lu, A. Gupta, W. Hu, H. Wu, S. Zhang, J. Kim, C. M. Chiu, B. G. Lee, Z. Yuan, and X. Yu, "24-3: Complementary LTPO Technology, Pixel Circuits and Integrated Gate Drivers for AMOLED Displays Supporting Variable Refresh Rates," *SID Symposium Digest of Technical Papers*, vol. 51, no. 1, pp. 351–354, 8 2020. [Online]. Available: /doi/pdf/10.1002/sdtp.13876 https://onlinelibrary.wiley.com/doi/abs/10.1002/sdtp.13876 https://sid.onlinelibrary.wiley.com/doi/10.1002/sdtp.13876

[7] D. R. Zhang, C. J. Deepu, X. Y. Xu, and Y. Lian, "A wireless ECG plaster for real-time cardiac health monitoring in body sensor networks," *2011 IEEE Biomedical Circuits and Systems Conference, BioCAS 2011*, pp. 205–208, 2011.

[8] "How to Measure ECG - Analog Lead Derivation — Video — TI.com." [Online]. Available: https://www.ti.com/video/5423179122001

[9] R. F. Yazicioglu, S. Kim, T. Torfs, H. Kim, and C. Van Hoof, "A 30 μw analog signal processor ASIC for portable biopotential signal monitoring," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 1, pp. 209–223, 2011.

[10] M. Sugiyama, T. Uemura, M. Kondo, M. Akiyama, N. Namba, S. Yoshimoto, Y. Noda, T. Araki, and T. Sekitani, "An ultraflexible organic differential amplifier for recording electrocardiograms," *Nature Electronics*, vol. 2, no. 8, pp. 351–360, 2019. [Online]. Available: https://doi.org/10.1038/s41928-019-0283-5

[11] "Application Report Analog Front-End Design for ECG Systems Using Delta-Sigma ADCs," 2009. [Online]. Available: www.ti.com

[12] D. Geng, K. Wang, L. Li, K. Myny, A. Nathan, J. Jang, Y. Kuo, and M. Liu, "Thin-film transistors for large-area electronics," *Nature Electronics*, vol. 6, no. 12, pp. 963–972, 2023. [Online]. Available: https://doi.org/10.1038/s41928-023-01095-8

[13] A. Rahaman, H. Jeong, and J. Jang, "A High-Gain CMOS Operational Amplifier Using Low-Temperature Poly-Si Oxide TFTs," *IEEE Transactions on Electron Devices*, vol. 67, no. 2, pp. 524–528, 2 2020.

[14] K. Myny, "The development of flexible integrated circuits based on thin-film transistors," *Nature Electronics*, vol. 1, no. 1, pp. 30–39, 2018. [Online]. Available: https://doi.org/10.1038/s41928-017-0008-6

[15] C. L. Lin, J. H. Chang, Y. C. Chen, P. H. Hsieh, Y. C. Chiu, C. H. Huang, and P. C. Lai, "LTPO-TFT Compensating Pixel Structure Reduces Thermally Generated Leakage Current in Low-Frame-Rate AMOLED Displays," *IEEE Transactions on Electron Devices*, vol. 71, no. 9, pp. 5528–5534, 2024.

[16] C. L. Lin, M. H. Cheng, C. D. Tu, C. C. Hung, and J. Y. Li, "2-D-3-D switchable gate driver circuit for TFT-LCD applications," *IEEE Transactions on Electron Devices*, vol. 61, no. 6, pp. 2098–2105, 2014.

[17] A. Rahaman, D. Y. Jeong, and J. Jang, "High Speed and Wider Swing, Level Shifter Using Low-Temperature Poly-Silicon Oxide TFTs," *IEEE Electron Device Letters*, vol. 40, no. 11, pp. 1772–1775, 11 2019.

[18] S. D. Brotherton, "Introduction to thin film transistors: Physics and technology of TFTs," *Introduction to Thin Film Transistors: Physics and Technology of TFTs*, vol. 9783319000022, pp. 1–488, 2 2013.

[19] P. Bahubalindruni, V. G. Tavares, P. G. De Oliveira, P. Barquinha, R. Martins, and E. Fortunato, "High-gain amplifier with n-type transistors," *2013 IEEE International Conference of Electron Devices and Solid-State Circuits, EDSSC 2013*, 2013.

[20] C. D. Chen, B. R. Yang, C. Liu, X. Y. Zhou, Y. J. Hsu, Y. C. Wu, J. S. Lm, P. Y. Lu, M. Wong, H. S. Kwok, and H. P. D. Shieh, "Integrating Poly-Silicon and InGaZnO Thin-Film Transistors for CMOS Inverters," *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3668–3671, 9 2017.

[21] L. Zhang, H. Yu, W. Xiao, C. Liu, J. Chen, M. Guo, H. Gao, B. Liu, and W. Wu, "Strategies for Applications of Oxide-Based Thin Film Transistors," *Electronics 2022, Vol. 11, Page*

960, vol. 11, no. 6, p. 960, 3 2022. [Online]. Available: https://www.mdpi.com/2079-9292/11/6/960/htm https://www.mdpi.com/2079-9292/11/6/960

[22] H. Ji, D. Geng, X. Chuai, X. Duan, Q. Chen, W. Wu, C. Chen, W. Jiang, J. Jiang, and L. Li, "An Advanced Full Adder Based Arithmetic Logic Unit (ALU) Using Low-Temperature Poly-Si Oxide TFTs," *IEEE Transactions on Electron Devices*, vol. 69, no. 11, pp. 6160–6165, 11 2022.

[23] W. Tesema, W. Jimma, M. I. Khan, J. Stiens, and B. da Silva, "A Taxonomy of Low-Power Techniques in Wearable Medical Devices for Healthcare Applications," *Electronics*, vol. 13, no. 15, 2024. [Online]. Available: https://www.mdpi.com/2079-9292/13/15/3097

[24] M. Zulqarnain, S. Stanzione, G. Rathinavel, S. Smout, M. Willegems, K. Myny, and E. Cantatore, "A flexible ECG patch compatible with NFC RF communication," *npj Flexible Electronics*, vol. 4, no. 1, pp. 1–8, 12 2020. [Online]. Available: https://www.nature.com/articles/s41528-020-0077-x

[25] F. Chiarugi, I. Karatzanis, G. Zacharioudakis, P. Meriggi, F. Rizzo, M. Stratakis, S. Louloudakis, C. Biniaris, M. Valentini, M. Di Rienzo, and G. Parati, "Measurement of heart rate and respiratory rate using a textile-based wearable device in heart failure patients," *Computers in Cardiology*, vol. 35, pp. 901–904, 2008.

[26] B. Xu, R. Liu, M. Shu, X. Shang, and Y. Wang, "An ECG Denoising Method Based on the Generative Adversarial Residual Network," *Computational and Mathematical Methods in Medicine*, vol. 2021, pp. 1–23, 4 2021.

[27] J. J. Bailey, A. S. Berson, A. Garson, L. G. Horan, P. W. Macfarlane, D. W. Mortara, and C. Zywietz, "Recommendations for standardization and specifications in automated electrocardiography: Bandwidth and digital signal processing. A report for health professionals by an ad hoc Writing Group of the Committee on electrocardiography and Cardiac Electrophysiology of the Council on Clinical Cardiology, American Heart Association," *Circulation*, vol. 81, no. 2, pp. 730–739, 1990. [Online]. Available: https://www.ahajournals.org/doi/pdf/10.1161/01.CIR.81.2.730?download=true

[28] P. R. Rijnbeek, J. A. Kors, and M. Witsenburg, "Minimum Bandwidth Requirements for Recording of Pediatric Electrocardiograms," *Hz from the American Heart Association. (Circulation*, vol. 104, pp. 3087–3090, 2001. [Online]. Available: http://www.circulationaha.org

[29] Behzad Razavi, *Design of analog CMOS integrated circuits*, 2nd ed., 2017.

[30] A. S. Berson and H. V. Pipberger, "Slew Rates for Electrocardiographic Signals," *IEEE Transactions on Biomedical Engineering*, vol. BME-25, no. 3, pp. 299–301, 1978.

[31] M. T. Thompson, "Review of Feedback Systems," *Intuitive Analog Circuit Design*, pp. 399–463, 2014.

[32] V. B. Guimarães, F. Z. Righi, L. Compassi-Severo, P. C. C. De Aguirre, and A. Girardi, "Analysis of topologies of MOSFET Current Mirrors."

[33] John M. Miller, "Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit." *Scientific Papers of the Bureau of Standards*, vol. 15, no. 351, pp. 367–385, 1920.

[34] P. Di Buono, L. Mistretta, and G. Costantino Giaconia, "A Novel Technique for the CMRR Improvement in a Portable ECG System," in *Applications in Electronics Pervading Industry, Environment and Society*, A. De Gloria, Ed. Cham: Springer International Publishing, 2017, pp. 219–225.

[35] *IEC 60601-2-25:2011*, 2nd ed. IEC, 10 2011. [Online]. Available: https://webstore.iec.ch/en/publication/2636

[36] "Texas Instruments: ADS1198 Datasheet (2010)," 2010. [Online]. Available: www.ti.com.

[37] B. Razavi, "The Flash ADC [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 3, pp. 9–13, 6 2017.

[38] W. Kester, "ANALOG-DIGITAL CONVERSION," 3 2004.

[39] J. Montanaro, R. T. Witek, K. Anne, A. J. Black, E. M. Cooper, D. W. Dobberpuhl, P. M. Donahue, J. Eno, G. W. Hoeppner, D. Kruckemyer, T. H. Lee, P. C. Lin, L. Madden, D. Murray, M. H. Pearce, S. Santhanam, K. J. Snyder, R. Stephany, and S. C. Thierauf, "A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 11, pp. 1703–1712, 1996.

[40] B. Razavi, "The StrongARM Latch [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, 2015.

[41] O. Kwon, J. Jeong, H. B. Kim, I. H. Kwon, S. Y. Park, J. E. Kim, and Y. Choi, "Electrocardiogram Sampling Frequency Range Acceptable for Heart Rate Variability Analysis," *Healthcare Informatics Research*, vol. 24, no. 3, p. 198, 7 2018. [Online]. Available: https://pmc.ncbi.nlm.nih.gov/articles/PMC6085204/

[42] M. Malik, A. John Camm, J. Thomas Bigger, G. Breithardt, S. Cerutti, R. J. Cohen, P. Coumel, E. L. Fallen, H. L. Kennedy, R. E. Kleiger, F. Lombardi, A. Malliani, A. J. Moss, J. N. Rottman, G. Schmidt, P. J. Schwartz, and D. H. Singer, "Heart rate variability: Standards of measurement, physiological interpretation, and clinical use," *Circulation*, vol. 93, no. 5, pp. 1043–1065, 3 1996. [Online]. Available: https://www.ahajournals.org/doi/10.1161/01.CIR.93.5.1043

[43] A. Rahaman, Y. Chen, M. M. Hasan, and J. Jang, "A High Performance Operational Amplifier Using Coplanar Dual Gate a-IGZO TFTs," *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 655–661, 2019.

[44] C. Garripoli, J. L. P. Van Der Steen, F. Torricelli, M. Ghittorelli, G. H. Gelinck, A. H. Van Roermund, and E. Cantatore, "Analogue frontend amplifiers for bio-potential measurements manufactured with a-IGZO TFTs on flexible substrate," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 7, no. 1, pp. 60–70, 3 2017.

[45] S. M. S. Faramarzi, A. Siskos, N. Papadopoulos, J. Genoe, and K. Myny, "High Performance 6V and 64.2dB LTPS TFT Operational Amplifier for Integrated Read-Out in Large Area Sensing Arrays," *Proceedings of the IEEE International Conference on Electronics, Circuits, and Systems*, 2024.

[46] M. Zhao, L. Li, R. Liu, B. Li, R. Chen, and Z. Wu, "A 43.5dB Gain Unipolar a-IGZO TFT Amplifier With Parallel Bootstrap Capacitor for Bio-Signals Sensing Applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 18, no. 6, pp. 1371–1381, 2024.

Appendix

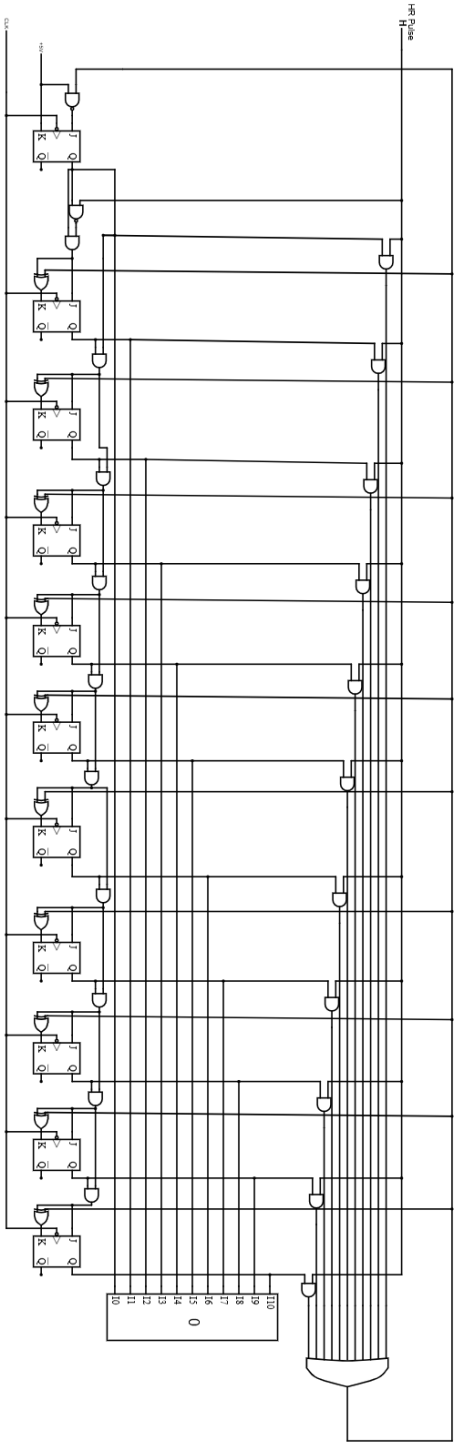

Figure 5.1: Proposal of a heart rate counter circuit in LTPO.