The Development of an Analogue Front End for ECG Signals in LTPO Technology

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Introduction

In the field of analogue circuit design, **thin-film transistors** (TFTs) are becoming increasingly prominent in specific applications due to their ability to **bend** and **fold** in any direction [1]. One promising application is in the **healthcare** sector, particularly for **electrocardiogram** (ECG) signal monitoring, where flexible chips could enable on-skin **amplification** and local **processing** of the heart's signals. This development opens the door to **passive**, **continuous** health monitoring for patients.
A recent advancement in TFT technology is the emergence of **Low-Temperature Polycrystalline Oxide** (LTPO), which hybridises the p-type TFTs **of Low-Temperature Poly Silicon** and the n-type TFTs from **Amorphous Indium Gallium Zinc Oxide** [2]. This thesis focuses on the development a **low-power analogue front end** (AFE) tailored for ECG signals using LTPO technology. The AFE consists of an **analogue amplifier** followed by a **digital heartrate detection** circuit.

Design

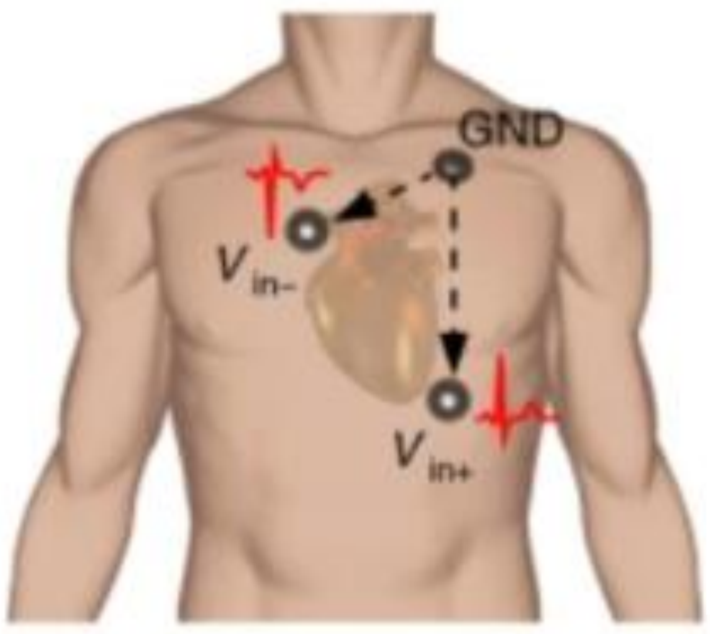

Figure 1: ECG Lead I measurement. [3]

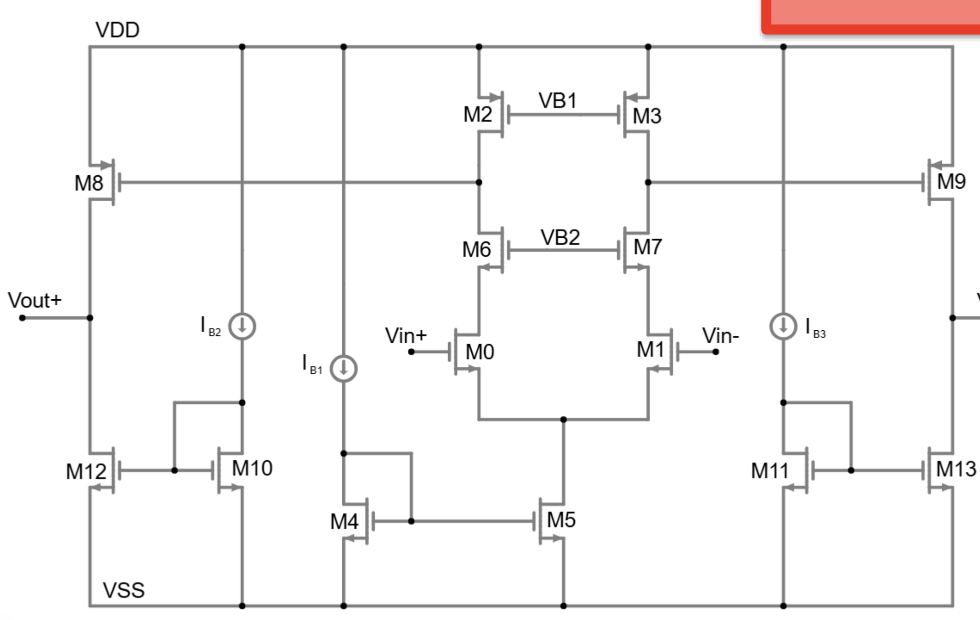

Figure 2: Amplifier circuit on transistor level.

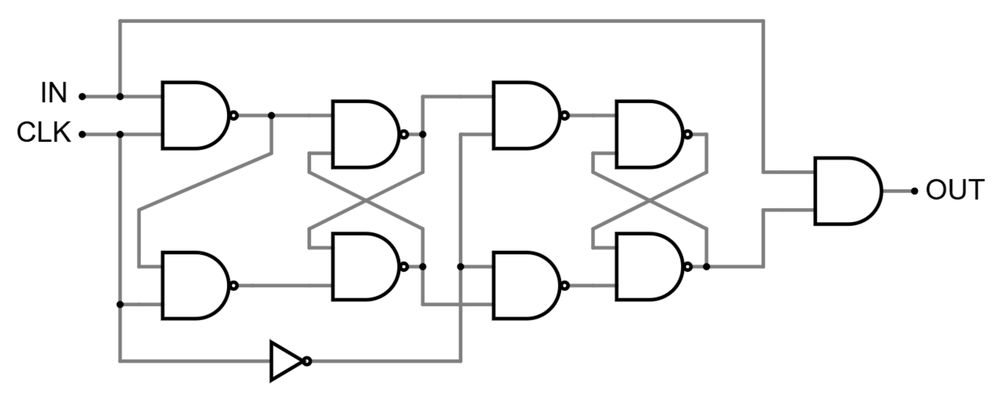

Figure 3: Edge detector design based on digital NAND and AND gates.

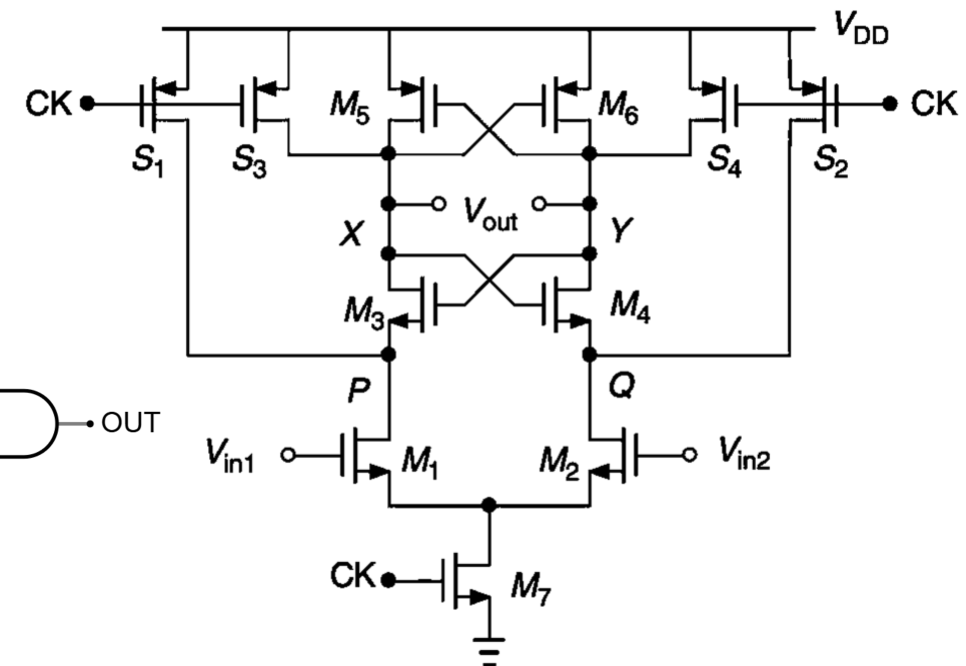

Figure 4: StrongARM comparator. [4]

The amplifier is based on a **two-stage fully differential architecture** (see Figure 2). This design achieves an open-loop gain **of 53 dB**, equivalent to approximately 450x amplification. With the addition of a **negative feedback** network, the closed-loop gain is reduced **to 49.6 dB** (≈300x), with a -3 dB cut-off frequency **of 8.5 kHz**. These results ensure **accurate amplification** of the full ECG signal bandwidth while attenuating unwanted high-frequency noise. This combination of **high gain** and **appropriate bandwidth** results in an amplifier **highly suitable** for ECG monitoring. However, the relatively **low phase margin** of **30°** causes the risk of an **unstable operation** due to **system variability** when implemented in a real circuit.

The **digital heartbeat detector** is based on a **StrongARM latch** topology (see Figure 4). Due to its simplicity and minimal static power consumption design, it is ideal for low-frequency and power implementations. The circuit functions as a **dynamic comparator**, evaluating the amplified ECG signal against a reference voltage. On each clock cycle, it outputs a **HIGH** or **LOW** signal depending on whether the input signal exceeds the reference level. Since a typical ECG waveform includes a distinct peak for each heartbeat, the comparator outputs a **HIGH** signal during each peak that crosses the reference threshold. To ensure that this signal is only triggered once per heartbeat, the output is fed into an **edge detector** (see Figure 3) that detects the transition from **LOW** to **HIGH** and **suppresses repeated outputs** from a single beat.

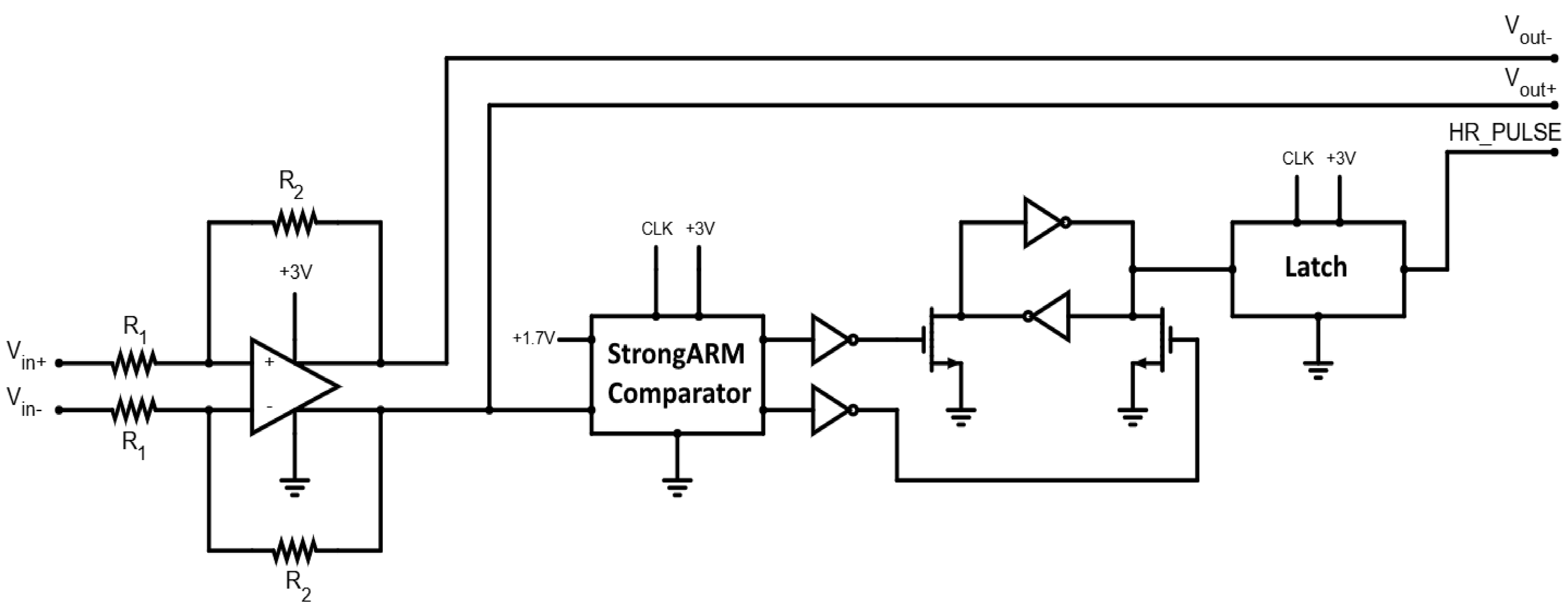

Figure 5: Full circuit diagram of the AFE.

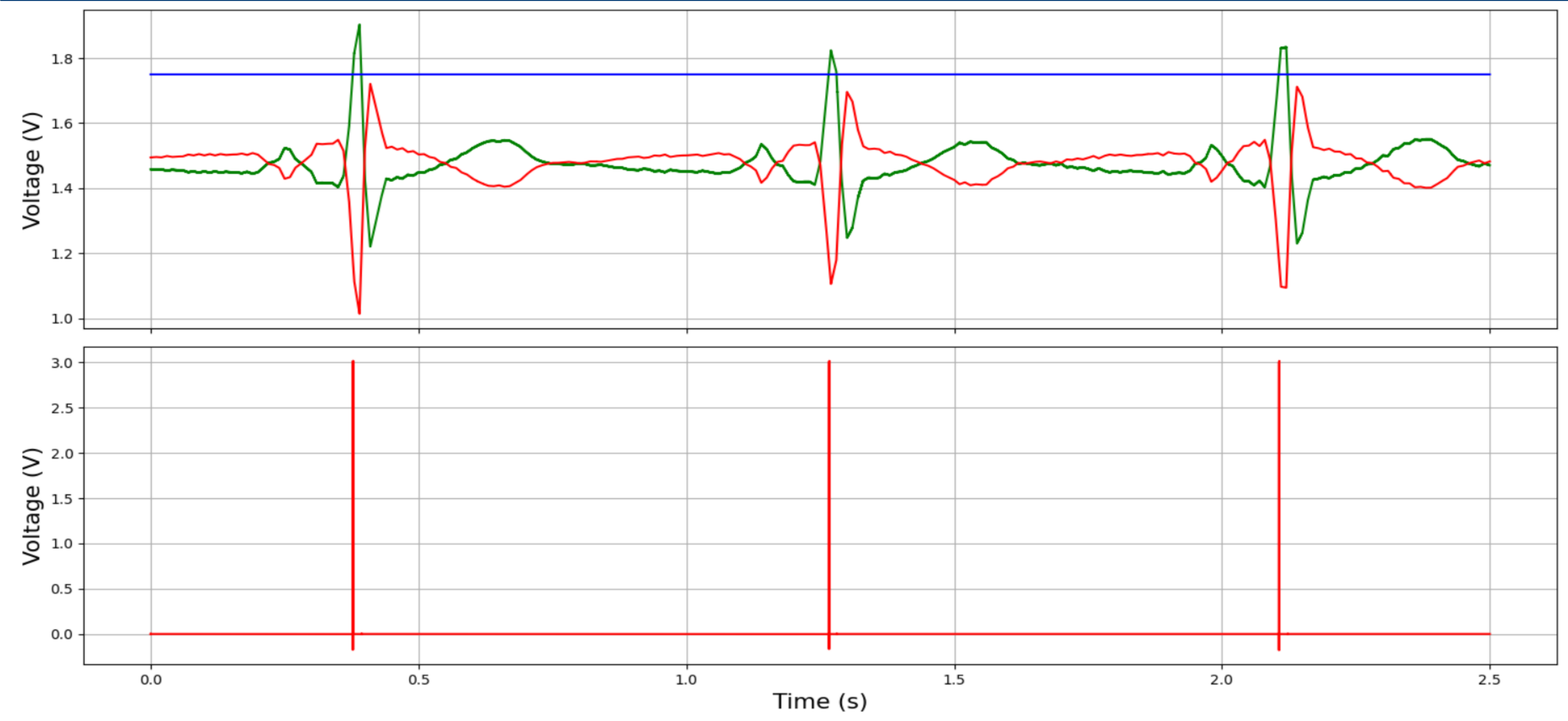

Figure 6: Output voltage signals of the AFE. Top: positive (green) and negative (red) output voltages, and the reference voltage (blue). Bottom: digital heartbeat pulse.

Results and Conclusion

The AFE consists of a fully differential signal amplifier followed by a digital signal processing (DSP) unit responsible for heartbeat detection (see Figure 5). The input consists of a **positive and negative ECG lead** sourced from the ECG dry electrode measurement setup (see Figure 1).
The AFE provides three outputs:

- **Two amplified differential outputs** (V_{out+} and V_{out-}), which preserve high signal integrity and provide **sufficient amplification** of the ECG waveform.
- **A digital pulse signal**, indicating heartbeat detection in real time for immediate **heart rate monitoring**.

An example of the output data can be seen in Figure 6, with the positive and negative nodes of the amplified signal on top, and the digital pulse signal on the bottom, that repeats every heartbeat.
The entire system operates from a low-power **3 V** supply, with an average power consumption of **6.8 µW**, well suited for long-lasting wearable devices. These results provide **considerable improvements** in performance and power consumption compared to previous research and make LTPO a **viable alternative** for flexible low-power analogue design.

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