High Sputter Bias Super Secondary Grain Growth Initiation (In Structures)

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ABSTRACT

Super secondary grain growth is initiated in thin copper seed layers on different types of barriers using high copper sputter bias conditions. In contrast to the low sputter bias initiated super secondary grains, which are dominant at room temperature, high sputter bias super secondary grain growth is dominant at elevated temperatures and leads to even bigger grain sizes (in the order of 500µm) and a nearly full super grain film coverage independent of the barrier composition/texture underneath. Moreover, by increasing the copper sputter bias conditions, a clear decrease in self annealing time at room temperature was observed. This knowledge is then used in an attempt to initiate super secondary grains in structures. For this purpose, two different methods are proposed in this paper and their efficiency on initiating super grains in structures is tested.

INTRODUCTION

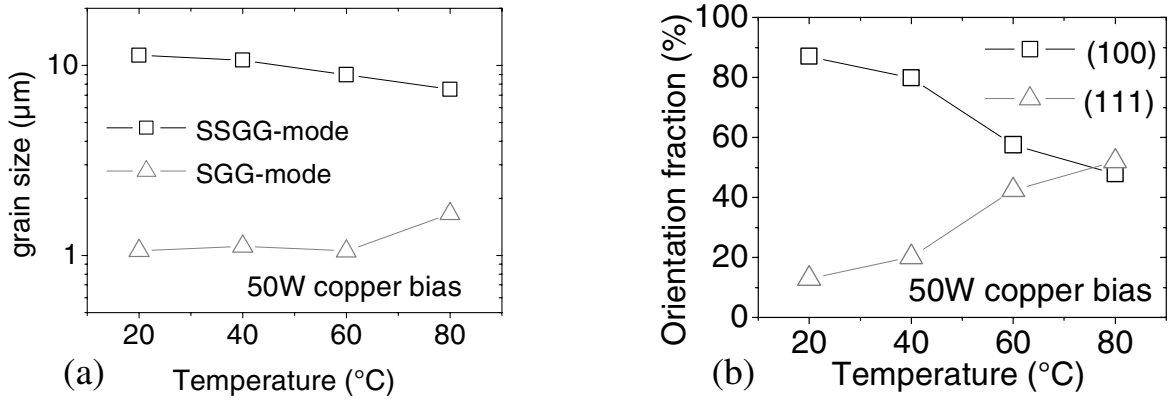
Electroplated copper has become the method of choice for filling narrow interconnect features in the back-end-of-line processing for microelectronic applications [1,2]. However, as the trench width decreases, the influence of the physical vapor deposited (PVD) seed layer becomes more important and changes the dynamics in trenches as the volume fractions of the electroplated (ECD) copper and PVD copper change significantly. Therefore, we refocused our efforts on understanding the grain growth mechanism in thin PVD copper films. In previous works, real time experiments revealed a novel highly concentric grain growth mode in copper seed layers on an α-Ta barrier, named super-secondary-grain-growth (SSGG). The initiation of these super grains depends strongly on the barrier layer microstructure, while strain energy minimization seems to be a very important driving force [3]. It was also shown that super grains can be initiated in ECD copper of various thickness on thick PVD seed layers [4]. In this work, we will further study the influence of the copper bias conditions and annealing temperatures on the SSGG growth dynamics, grain size and film coverage, using a combination of stress measurements with a real-time monitoring of the annealing process at elevated temperatures with a scanning electron microscope (SEM) and an automated electron backscatter diffraction (EBSD) technique. In a next step, we use this knowledge in an attempt to initiate super grains in structures using two different methods.

EXPERIMENTAL

All layers were deposited on 200 mm Si(100) wafers with standard layers of 50 nm Si_3N_4 and 500 nm SiO_2. The standard layers are followed by SIP (Self Ionised Plasma) deposition of various barrier layers and Cu seed layers. The standard bias condition used for both barrier and seed layer deposition is 100W. For the diffusion barriers, 3 different barrier types (with a different composition and structure as determined by XRD) were used in order to reveal the influence on the film texture and grain growth rate in thin PVD films: 15nm TaN (amorphous), 15nm β-Ta and 10nmTaN/5nm α-Ta. For the seed layer deposition, the copper bias conditions were varied from 0W, 50W, 150W to 250W. The stress measurements on thin films are made with a KLA-Tencor RS75 four point probe and FLEXUS curvature measurement. A XL30-FEG SEM (scanning electron microscope) has been redesigned to enable us to monitor grain growth in "real-time" at elevated temperatures up to 300 ^{O}C by taking backscattered electron (BSE) images of a certain region of the sample at well defined moments in time. Moreover, using cross-correlation functions it is also possible to take a large number of detailed overlapping images and construct a detailed overall image of a large area. In this way, it is possible to construct grain growth 'movies' e.g. of both bond-pads and long narrow lines. Additionally, an automated EBSD system is used to obtain additional information about the crystallographic orientation of the grown copper grains.

RESULTS AND DISCUSSION

For low copper bias conditions (i.e. copper sputter bias between 0-150W), real time grain growth monitoring at different temperatures clearly reveals a decrease in the final super-secondary-grain-growth (SSGG) grain size and film coverage while the opposite trend can be found for the secondary-grain-growth-mode (SGG) (figures 1a-b). This suggests that either the initiation rate is lower at the higher temperature, or the thermal activation of normal SGG is higher, thereby inhibiting extensive SSGG. Increasing the copper sputter bias conditions clearly reveals a decrease in self-annealing time of the super grains at room temperature, as shown in figure 2a.



Figures 1a-b: the influence of the annealing temperature on (a) the SSGG and SGG grain size and (b) the orientation fraction of both growth modes, as determined with the EBSD technique. As shown in a previous work, the super grains are all (100) oriented while the secondary grains are predominantly (111) oriented.

For a 0W copper bias, super grains were already observed after a day, while for a 150W copper bias it took up to 6 months to observe considerable super grain growth. For a 250W copper bias condition, no SSGG was observed even after 6 months self-annealing at room temperature, as shown in figure 2b.

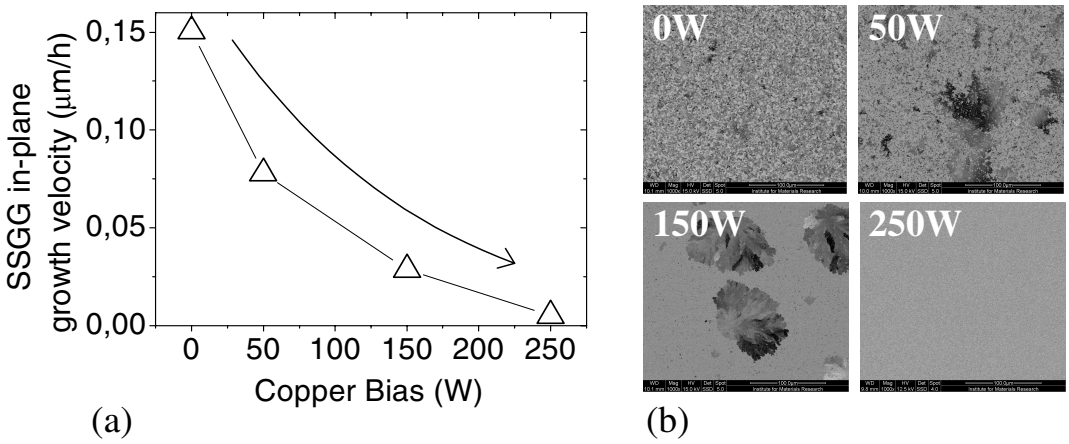
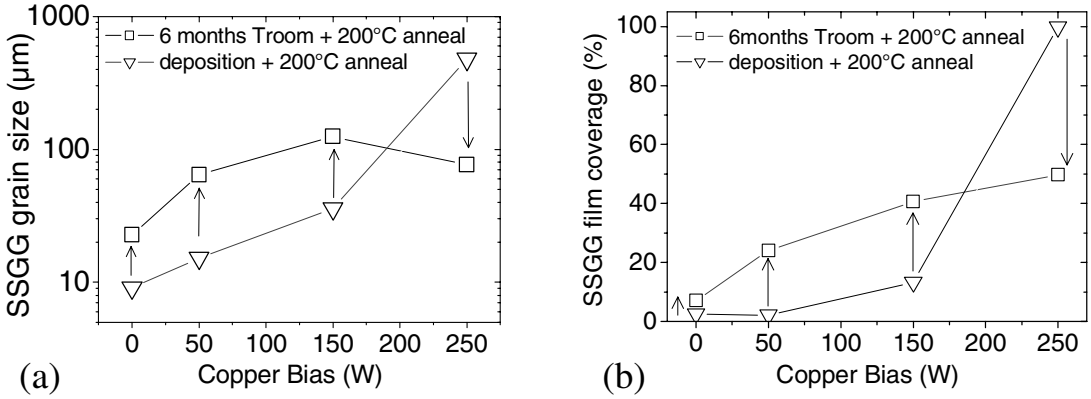


Figure 2a-b: (a) influence of the copper bias on the SSGG in-plane growth velocity and (b) Top view SEM images of 500nm copper seed layer, deposited with respectively a 0W, 50W, 150W and 250W copper sputter bias. The images are taken from a "real time" SEM measurement at room temperature, 6 months after deposition.

Figures 3a-b show the influence of the copper bias on the final SSGG grain size and film coverage for two different annealing conditions: (A) 200°C anneal for 5 hours just after deposition (triangular dots) and (B) 200°C anneal for 5 hours after 6 months self-annealing at room temperature (squared dots). In both cases, the SSGG grain size and film coverage increases with increasing copper bias. This correlates well with the increasing initial film stress with higher copper sputter bias conditions (-210MPa for a 50W seed layer compared to -290MPa for a 250W seed layer) and an orientation dependent driving force for super grains, where strain energy minimization seems to be an important driving force. For low copper sputter bias conditions up to 150W, the largest SSGG grain size and film coverage was found when films were annealed after 6 months self-annealing. This agrees well with the observed dominant behaviour of these super grains at room temperature for low copper bias conditions (see figures 1a-b). However, the opposite trend is observed when a high 250W copper bias condition is used, resulting in even larger SSGG grain sizes up to 500µm and a film coverage of almost 100%.



Figures 3a-b: the influence of the copper bias conditions on (a) the SSGG grain size and (b) the SSGG orientation fraction, as determined with the EBSD technique. The samples were given an additional anneal just after deposition (squares) or after 6 months self-annealing at room temperature (triangles).

These observed trends are independent of the barrier composition underneath, as shown in figure 4. This was not the case for low copper bias conditions, as here super grains mostly seem to appear in copper films on α-Ta barrier layers and to a lesser degree on other barrier compositions. Both grain size and the amount of SSGG film coverage as a function of copper bias can be explained in terms of initial film stress values and strain energy minimization as an important driving force for super grains.

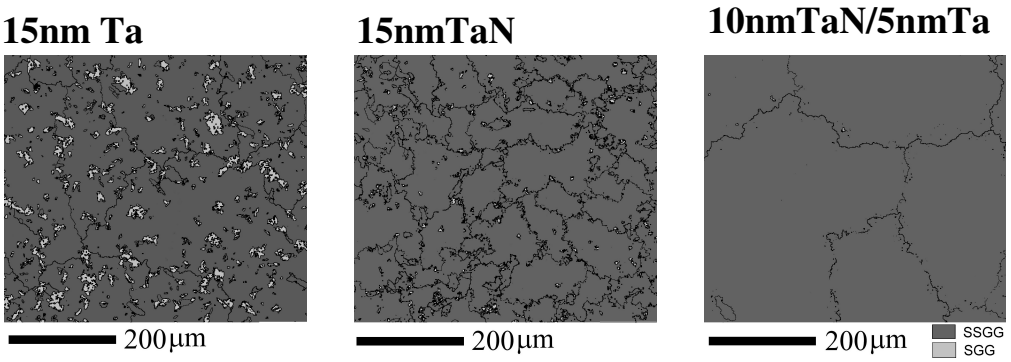


Figure 4: EBSD mapping of a 500nm (250W) PVD seed layer on respectively a 15nm TaN, a 15nm Ta and a 10nmTaN/5nm Ta barrier layer after a 200°C anneal for 5hours; the dark grey colors show the SSGG-mode, while the light grey colors show the SGG-mode

As determined in an earlier work, the activation energy for super grain growth using 50W copper bias conditions was found to be around 0.77eV [4]. Figures 5a show the SSGG activation energy for both 50W and 250W super grains, using the mean in-plane growth velocity of the super grains at different temperatures as determined by real-time measurements. These results indicate that the SSGG activation energy seems independent of the copper bias conditions. However, the high sputter bias super secondary grains are activated at elevated temperatures compared to low sputter bias super secondary grains which are dominant at room temperatures. Figures 5b-c show an example of the grain diameter evolution versus time for a set of super grains initiated in a 500nm (250W) copper seed layer during a 200°C anneal. Despite the advantages of larger super grains and an almost full film coverage for high bias sputtered copper films, one of the major disadvantages is the increasing number of hillocks observed in the copper films with copper sputter bias (figure 7b).

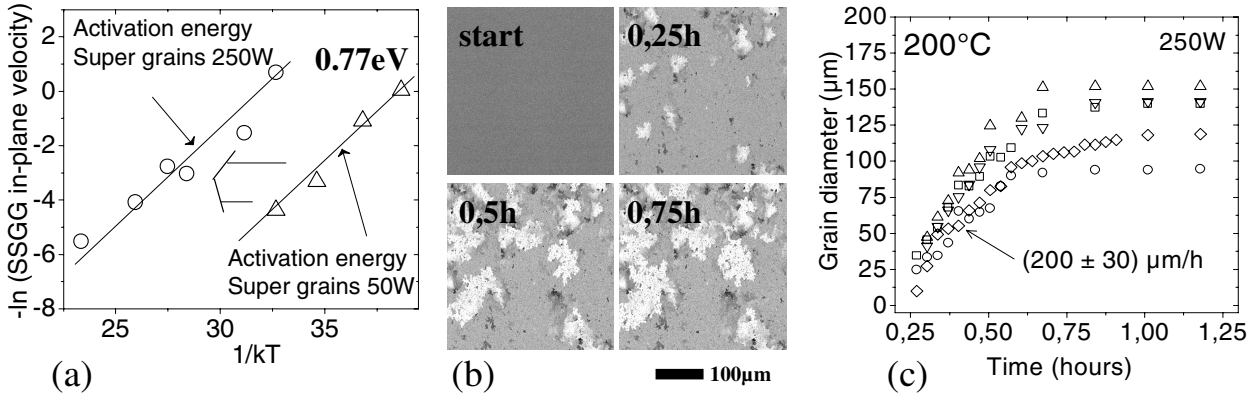


Figure 5a-c: (a) determination of the SSGG activation energy for two different copper bias conditions, using the SSGG in-plane growth velocity (b) microstructural evolution of a 500nm (250W) copper seed layer annealed at 200°C and (c) the SSGG grain diameter evolution versus time for a 500nm (250W) seed layer annealed at 200°C. The bending of the grain diameter versus time curves above 0,5h is due to the collisions of the grains.

As mentioned earlier, strain energy minimization is a very important driving force for the SSGG-mode. In order to get a better understanding of the stress relaxation mechanism in these copper thin films, a termal cycling experiment was performed on a 500nm (250W sputter bias) thick copper film just after deposition, monitoring both stress and microstructural evolution in the copper film. During the 1st cycle, the stress follows the thermoelastic line up to 100°C with a slope of –3.0 MPa/°C due to the difference in thermal expansion coefficients of copper and silicon. At higher temperatures, a deviation of the thermoelastic line is observed, showing a huge stress relaxation in the order of 350MPa between 100-150°C (zone a-d on figure 6), followed by a large stress plateau.

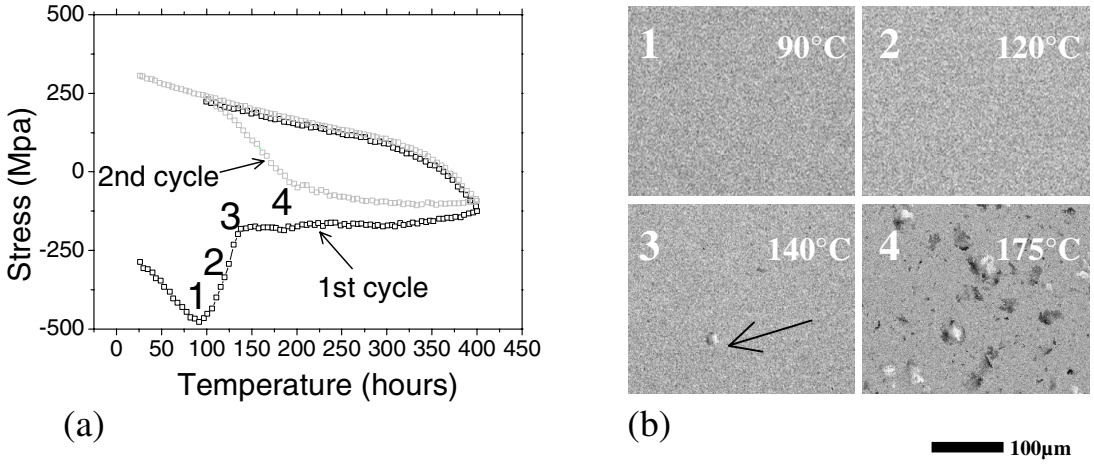


Figure 6: (a) termal cycling experiment (1st cycle: black dots; 2nd cycle: grey dots) on a 500nm copper seed layer with 250W copper bias showing the film stress as a function of the temperature during heating and cooling. (b) real time SEM images during the heating of the film, showing that the SSGG only appear at the copper surface when the stress plateau is reached (region b on the curve)

During this large stress relaxation step (zone 1-2-3 on figure 6a), hillock formation was observed between 120°C and 140°C using real time SEM monitoring (see figures 7a-b). Super grains were observed at the copper surface for the first time around 140-150°C, and continued to grow from this point on eventually covering the whole film (figure 6b). This stress relaxation/microstructural evolution is not yet fully understood and therefore needs additional thermal cycling experiments on copper films with different thickness and copper bias conditions.

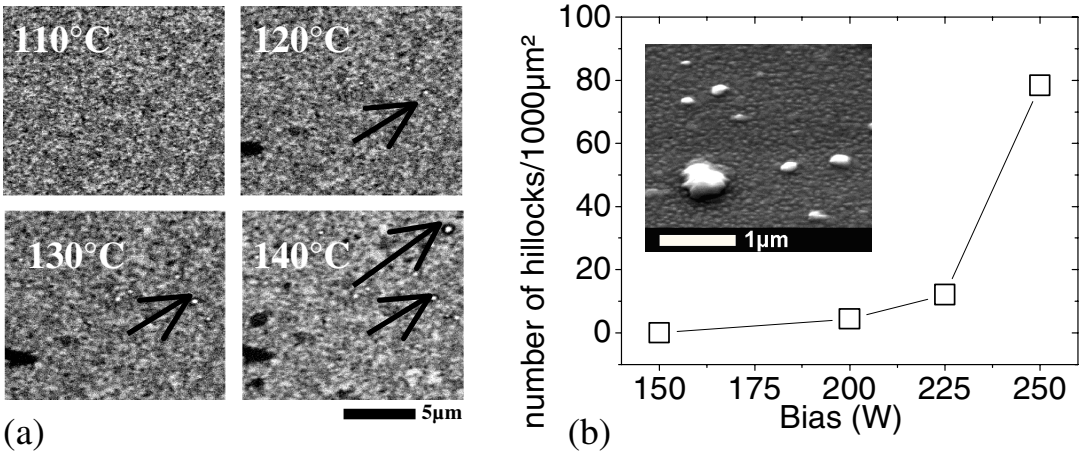


Figure 7: (a) real time top SEM images during a termal cycling experiment, revealing hillock formation (b) influence of the copper bias on the number of hillocks

In an attempt to implement super grains into structures, two different process methods A and B are considered and evaluated. An overview of both methods is shown in figure 8. In a first method A, the trenches (as wel as the regions in between the trenches) were filled with a 600nm 250W copper sputtered seed layer in stead of the standard copper filling process (i.e. seed layer followed by electroplated copper) and afterwards annealed at 200°C for several hours. In order to prevent void formation in the trenches, only the very wide and shallow trenches are considered during subsequent characterization.

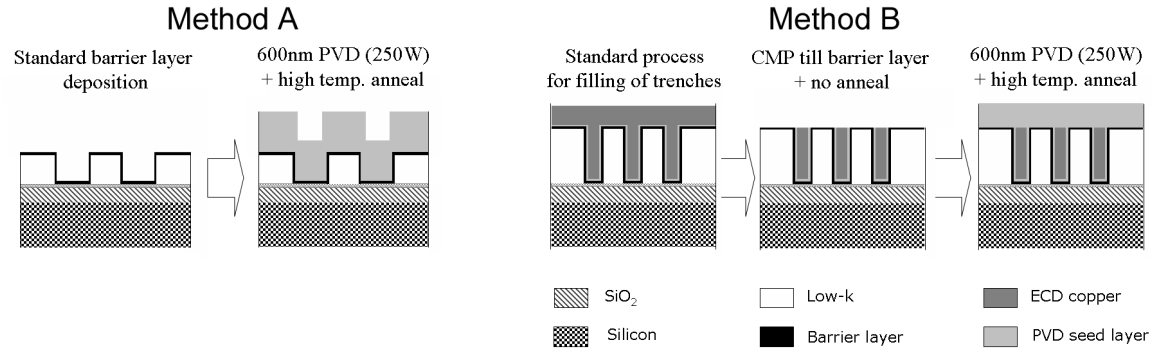
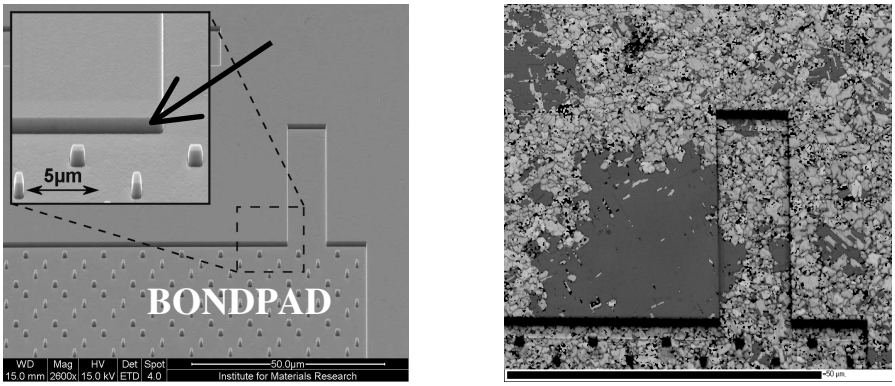


Figure 8: schematic overview of the two methods that were used to initiate super grains in structures. For method A, all trenches as well as the regions in between the trenches are filled with a 600nm (250W) sputtered copper seed layer in stead of the standard copper filling process, followed by a 200°C annealing step. For method B, all the trenches were filled using the standard filling process, followed by a CMP step back to the barrier layer and a subsequently cleaning step. In a final step, a 600nm (250W) copper layer is sputtered on top of the structures, followed by a high temperature anneal and a CMP step.

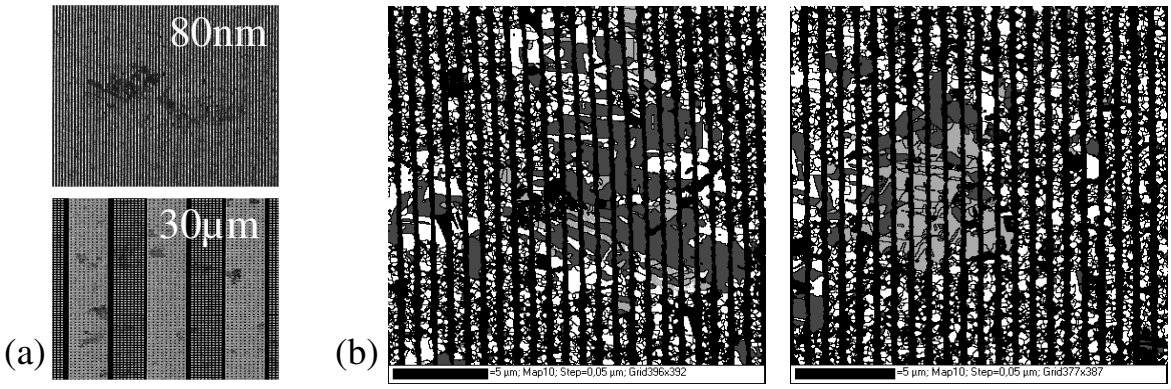
Figure 9b shows the results for method A after an anneal step at 200°C for 5 hours. These figures reveal that super grains can be initiated in large areas near structures and bondpads. However, only a very small number of super grains can actually grow further into the structures after annealing due to difference in height between the copper in the lines and on top of the region in between (arrow on figure 9a). Moreover, another disadvantage of this method is the fact that it doesn't deal with the formation of hillocks after the anneal step.



(a) (b)

Figure 9: (a) SEM image of a bondpad filled with a 600nm PVD seed layer, tilted at 70° (b) EBSD image of the same region. The dark grey colors show the SSGG-mode, while the light grey colors show the SGG-mode

A second method (method B) to initiate super grains in structures uses a standard filling process of trenches, followed by a chemically mechanically polishing (CMP) step back to the barrier layer with a subsequently cleaning step and no annealing step to prevent self-annealing of ECD copper in trenches. In a final step, a 600nm (250W) copper layer is sputtered on top of the structures, followed by high temperature anneal and a CMP step in order to initate super grains in the overburden and investigate the influence of SSGG in-growth in structures. Figure 10a shows a first result using a standard anneal at 200°C for 30 seconds, revealing some SSGG in-growth in 30µm wide lines up to 80nm wide lines. This SSGG in-growth is still insufficient due to the limited annealing time of 30 seconds (the SSGG in-plane growth velocity at 200°C is around 200µm/hour as determined using "real time" in-situ SEM measurements; see figure 5c). Figure 10b shows two EBSD maps on 400nm wide lines, revealing a variety of orientations for the observed super grains that have grown into these structures. Further optimization of both SSGG grain size and film coverage in structures by increasing the annealing time, together with a better understanding of stress relaxation/growth dynamics are in progress.



Figures 10a-b: (a) SEM images of 80nm and 30µm wide lines after applying method B as described in figure 8, revealing some SSGG in-growth. (b) EBSD mapping of a two different super grains in 400nm wide lines, revealing the different orientations. The white regions correspond to the (111) orientation parallel to the normal film direction (ND). Dark and light grey regions correspond respectively to the (100) orientation // ND and the (110) direction //ND

CONCLUSIONS

Super secondary grain growth is initiated in thin copper seed layers on different barrier types using high copper sputter bias conditions. This high sputter bias super secondary grain growth is dominant at elevated temperatures and leads bigger grain sizes up to 500µm and a nearly full super grain film coverage independent of the barrier composition/texture. Two different methods were proposed and evaluated in an attempt to initiate super secondary grains in structures.

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