D O C T O R A A T S P R O E F S C H R I F T

Faculteit Wetenschappen

Modelling of the hot-carrier degradation behaviour of submicron nMOSFETs making use of high-resolution measurements

Proefschrift voorgelegd tot het behalen van de graad van
Doctor in de Wetenschappen, richting Natuurkunde

RAF DREESEN

Promotor : Prof. dr. L. De Schepper
Co-promotor : Prof. dr. ir. H. Maes

2000

INSTITUUT VOOR MATERIAALONDERZOEK

LIMBURGS UNIVERSITAIR CENTRUM
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If we knew what it was we were
doing, it would not be called
research, would it?

A. Einstein (1879-1955)

Een woord van dank...

Op de voorpagina van dit proefschrift staat enkel mijn naam geschreven. Dit werk is echter tot stand gekomen dankzij het feit dat ik op de juiste momenten een beroep kon doen op de geschikte specialisten. Ieder van deze specialisten heeft zijn eigen vakgebied, en dat is niet noodzakelijk enkel in het wetenschappelijk onderzoek gesitueerd. De onderstaande lijst is waarschijnlijk verre van volledig, maar toont wel aan dat dit geen persoonlijk werk is: ere wie ere toekomt...

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De laatste die ik wil bedanken moet eigenlijk helemaal vanboven staan. Leven met zo'n vent als mij moet niet gemakkelijk zijn. Ze heeft wel beloofd mij te steunen in goede en kwade dagen maar je moet het nog maar doen ook. Bedankt Monique, een volgende stap in ons leven is weer voltooid, hopelijk wordt het vervolg zo mooi als de afgelopen negen jaren...

Bedankt allemaal,

Raf

Contents

Nederlandse samenvatting

Algemene Inleiding

Dit werk kan best gesitueerd worden in het onderzoek naar het testen van de betrouwbaarheid van geïntegreerde schakelingen (IC's). Deze testen zijn belangrijk omdat enerzijds vanuit het oogpunt van veiligheid continu operationele IC's onontbeerlijk zijn, en anderzijds omdat de concurrentiekracht van fabrikanten sterk afhangt van de aantoonbare betrouwbaarheid van de geproduceerde IC's. De toenemende miniaturisatie in de microtechnologie zorgt ervoor de betrouwbaarheid van een IC steeds moeilijker te garanderen is.

De betrouwbaarheid van een IC wordt meestal gecontroleerd door na te gaan of alle verschillende soorten componenten op de IC betrouwbaar zijn. Deze componenten kunnen opgesplitst worden in off-chip en on-chip onderdelen. Op het on-chip niveau moeten zowel de actieve als de passieve componenten getest worden. Enkele van die on-chip elementen zijn MOSFET's, diëlektrica, interconnecties, ...

Een cruciaal probleem dat opduikt bij het testen van een nieuwe technologie is dat de levensduur van de geteste componenten onder normale werkingscondities zeer lang is (in orde van jaren). Daarom is het nodig dat de fysische mechanismen die verantwoordelijk zijn voor faling grondig bestudeerd worden en moeten er methodes ontwikkeld worden die deze mechanismen versnellen. Ook moeten er modellen ontwikkeld worden om de resultaten die bekomen zijn op de versnelde condities te extrapoleren naar normale werkingscondities.

Dit werk onderzoekt de betrouwbaarheid van de MOSFET. MOSFET staat voor "Metal Oxide Semiconductor Field Effect Transistor", een transistor met drie opeenvolgende lagen: een metaal met daaronder een oxide en vervolgens een stukje halfgeleidermateriaal. De werking van deze transistor berust op het veldeffect. Door de toenemende miniaturisatie zijn ook de dimensies van de MOSFET alsmaar gedaald sinds zijn ontstaan. Dit heeft geleid tot een sterke toename van de elektrische velden in de MOSFET omdat de voedingsspanning niet evenredig is meegedaald. De energie van de elektronen die in het kanaal van de nMOSFET bewegen in deze hoge velden, neemt

continu toe. Deze hoogenergetische ladingsdragers kunnen voldoende energie krijgen om de Si-SiO_2 barrière te overwinnen en in het oxide geïnjecteerd te worden. De schade die door deze geïnjecteerde ladingsdragers wordt veroorzaakt kan leiden tot een vervorming van de elektrische karakteristieken van de MOSFET wat op zijn beurt een negatieve invloed heeft op de IC waarin hij zich bevindt.

De afgelopen decennia is de degradatie van MOSFETs onder invloed van hoogenergetische ladingsdragers uitvoerig bestudeerd. In het begin werd vooral onderzoek gedaan op conventionele MOSFETs, met een zwaar gedopeerde drainstructuur. Op dit moment zijn de degradatiemechanismen van deze MOSFETs gekend en enkele goede modellen zijn ontwikkeld om het degradatiegedrag te beschrijven en om de levensduur van de component bij normale werkingscondities te schatten. Met het invoeren van de "Lightly Doped Drain" (LDD) nMOSFETs werden nieuwe degradatiemechanismen geïntroduceerd. Ondanks het feit dat een algemeen aanvaard beeld is ontwikkeld over de fysische degradatiemechanismen van deze MOSFETs bestaat er nog geen algemeen aanvaard model om het degradatiegedrag te beschrijven en de levensduur van deze component bij normale werkingscondities te bepalen.

De testsystemen die de dag van vandaag beschikbaar zijn om de degradatie van MOSFETs onder invloed van hoogenergetische ladingsdragers te bestuderen hebben een meetresolutie van ongeveer 0.5 %. Dit betekent dat de karakteristieken van de MOSFET met meer dan 0.5 % moeten verschuiven alvorens de degradatie detecteerbaar is. Dit heeft als gevolg dat het initiële degradatiegedrag met deze systemen niet kan bestudeerd worden. Bovendien moeten de aangelegde stresscondities tijdens een test veel hoger zijn dan de normale werkingscondities. Dit kan extra degradatiemechanismen veroorzaken die niet optreden bij normale werkingscondities.

De Hoge Resolutie Meettechniek

Het eerste doel van dit doctoraat bestaat erin om een nieuwe meettechniek te ontwikkelen waardoor de degradatiemetingen kunnen gebeuren met een hoge meetresolutie.

In de Hoge Resolutie Meettechniek (HRMT) worden de degradatieparameters afgeleid van de I-V karakteristieken van de MOSFET. Om zo een parameter te bepalen wordt de I-V karakteristiek niet volledig opgemeten maar enkel een dense meting in een beperkt gebied rond de gewenste parameter wordt opgemeten met erg nauwkeurige

meetapparatuur. Om een hoge meetresolutie te bekomen is het nog nodig dat de omgevingstemperatuur van de MOSFET onder controle wordt gehouden. Allereerst moet de meetprocedure zo ontwikkeld worden dat de tijd dat er stroom door het kanaal vloeit geminimaliseerd is. Daardoor is de interne opwarming van de MOSFET geminimaliseerd. Dan is de inwendige temperatuur praktisch gelijk aan de uitwendige. Vervolgens zijn er 2 manieren om de uitwendige temperatuur onder controle te houden:

- Correctie van de degradatiemetingen voor de veranderingen van de omgevingstemperatuur. Dit wordt gedaan in twee opeenvolgende stappen: eerst wordt de temperatuurscoëfficiënt (TC) bepaald uit een karakterisatiemeting en vervolgens wordt de degradatiemeting gecorrigeerd voor de veranderingen van de omgevingstemperatuur met behulp van deze TC
- Stabilisatie van de omgevingstemperatuur van de MOSFET

In dit werk zal de tweede methode gebruikt worden. Daarom wordt de MOSFET in een afgesloten ruimte ondergebracht en de temperatuur in deze ruimte wordt gestabiliseerd op 29.6 °C en de stabiliteit bedraagt 0.03 °C. Deze techniek laat toe om degradatiemetingen op MOSFETs uit te voeren met een meetresolutie van minder dan 200 ppm.

De degradatie van conventionele nMOSFETs onder invloed van hoogenergetische ladingsdragers.

De HRMT zal eerst worden toegepast om de betrouwbaarheid van conventionele nMOSFETs te bestuderen. Degradatiemetingen op MOSFETs van een 2.4 μm technologie zullen worden uitgevoerd. Het model van Hu en het model van Takeda zullen uitvoerig besproken worden en het model van Takeda zal worden afgeleid van het model van Hu door 2 benaderingen te maken. Vervolgens worden de degradatiemetingen gefit aan beide modellen door gebruik te maken van de kleinste kwadratenschatting. Verder zal worden aangetoond dat een correcter levensduurmodel van Takeda wordt bekomen wanneer $V_{d,sat}$ niet verwaarloosd wordt ten opzichte van V_d.

In plaats van elke degradatiecurve apart te fitten en gebruik te maken van een levensduurplot om de levensduur bij normale werkingscondities te voorspellen, wordt er in dit werk voorgesteld om alle degradatiecurves simultaan te fitten met een lineaire kleinste kwadratenfit. Met behulp van de fitcoëfficiënten kan niet alleen de levensduur, maar het volledig degradatiegedrag bij normale werkingscondities voorspeld worden.

Op het einde van dit hoofdstuk worden de voordelen van de HRMT bestudeerd op het

gebied van fysische degradatiemechanismen, nauwkeurigheid van levensduur-voorspelling en testtijdreductie. Hieruit kan worden besloten dat er slechts 1 degradatiemechanisme actief is in het volledig degradatiegebied, namelijk het creëren van toestanden in het tussenvlak tussen het Si en het SiO_2. Bovendien wordt hier aangetoond dat de nauwkeurigheid op de levensduurvoorspelling niet significant kan verbeterd worden door gebruik te maken van de HRMT. De testtijden kunnen wel serieus worden gereduceerd met deze nieuwe meettechniek.

De degradatie van LDD nMOSFETs onder invloed van hoogenergetische ladingsdragers.

In dit laatste hoofdstuk wordt de degradatie van LDD nMOSFETs bestudeerd. Degradatiemetingen, uitgevoerd op drie verschillende technologieën, tonen aan dat het degradatiegedrag kan beschreven worden met behulp van een tweetraps mechanisme. In een eerste stadium neemt de serieweerstand toe en deze toename satureert. Vervolgens daalt de mobiliteit van het kanaal. Dit degradatiegedrag kan niet worden beschreven met het model van Hu of Takeda.

Tot nu toe bestond er geen model om dit degradatiegedrag correct te beschrijven en de levensduur van deze componenten bij normale werkingscondities te bepalen. Door een combinatie te maken van het model van Chan en Goo, en het geheel in een vorm te gieten, zal een nieuw model ontwikkeld worden waarmee een simultane kleinste kwadratenfit van alle degradatiecurves kan uitgevoerd worden. Met behulp van de fitcoëfficiënten kan vervolgens het volledig degradatiegedrag bij normale werkingscondities voorspeld worden. Dit nieuw model zal gebruikt worden om het degradatiegedrag van de drie verschillende technologieën te beschrijven en de levensduur van deze MOSFETs te voorspellen.

List of abbreviations and symbols

CMOS	complementary MOS structure
C_{ox}	gate oxide capacitance
D	drain
D_H	effective diffusion constant
DUT	device under test
DDD	double diffused drain
E_c	energy of the bottom of the conduction band
E_C	critical field at which the carrier velocity saturates
E_m	maximum electric field at the drain
FC	failure criterion
φ_i	impact ionisation energy
φ_{it}	energy for interface trap generation
$g_{m,max}$	maximum of the transconductance
HRMT	high resolution measurement technique
IC	integrated circuit
I_d	drain to source current
$I_{d,lin}$	linear drain to source current
$I_{d_{n^-}}$	drain to source current through the n^- region of an LDD MOSFET
$I_{d,sat}$	saturation drain to source current
$I_{d,with}$	drain to source current through a MOSFET with a source/drain side series resistance
$I_{d,without}$	drain to source current through a MOSFET without a source/drain side series resistance
I_{sub}	substrate current

k	Boltzmann's constant
l	effective length of the velocity saturation region
L	channel length of a MOSFET
LDD	lightly doped drain
LOCOS	local oxidation of silicon
LSE	least-square estimation
λ	hot-electron scattering mean free path
MOSFET	metal oxide semiconductor field-effect transistor
$n_H(0)$	concentration of interstitial hydrogen atoms H_i at the interface
nMOSFET	n-channel MOSFET
N_{it}	number of interface traps
P	property
ppm	parts per million
q	electron charge
R_{ch}	channel resistance
R_D	drain-side series resistance
R_{eq}	equivalent resistance
R_S	source-side series resistance
S	source
σ_S	dispersion parameter of the lognormal distribution
T	temperature
T_e	effective electron temperature
t	time
TC	temperature coefficient
t_{ox}	gate oxide thickness
τ	lifetime

ULSI	ultra-large-scale integration
V_d	drain to source voltage
V_{dd}	power supply voltage
V_g	gate to source voltage
VLSI	very-large-scale integration
V_t	threshold voltage
$V_{t_{n^-}}$	threshold voltage of the n^- region
μ	channel mobility
μ_{n^-}	mobility of the n^- region
W	channel width of a MOSFET
X_H	effective length of diffusion

1. General Introduction

1.1. Introduction

In today's modern society, it's impossible to imagine the life of an average family without products such as automobiles, personal computers, home appliances, mobile telephones, ... As a user, we have noticed an enormous growth in performance and complexity of these products during the past few decades without a significant price increase. This evolution is mainly due to the enormous work researchers performed on the basic building block of these products: the integrated circuit (IC). The growth in performance and complexity is reached by drastically reducing the basic building blocks of an IC and increasing the circuit density. This ongoing miniaturisation of microelectronics is shown in Figure 1-1 graphically. The number of transistors per chip or IC are plotted as a function of time for two IC-types: memory cells and microprocessors. It can be observed that the transistor density doubles about every two years. Since the cost per unit area of a fully fabricated IC has remained nearly constant through the same time period, the price of a Pentium Pro was hardly higher than the price of a 80486 in the beginning of the nineties or a 80286 10 years before [Trou98].

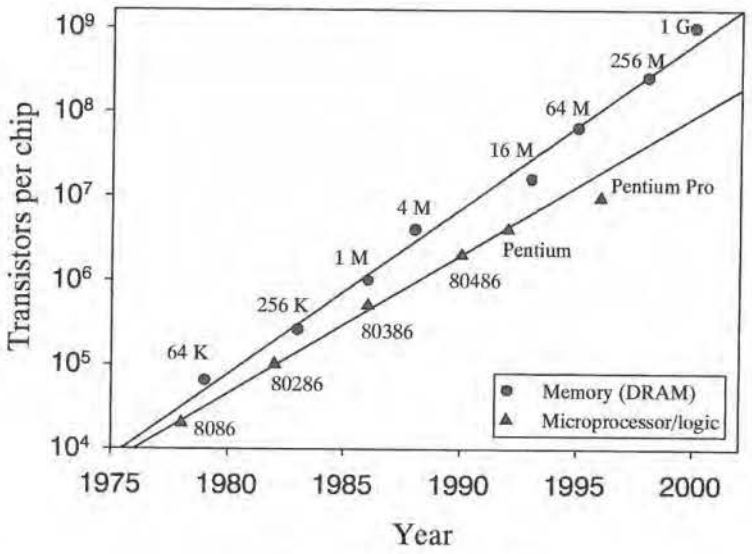

Figure 1-1: Number of transistors per chip in memory cells and microprocessors.

When a new product is introduced on the market, it is important that it works properly during the first 5 or even 10 years. Consequently, reliability research has evolved to a very important topic in the high-tech world of the IC. As a definition, reliability is stated to be the probability that an item, operating under normal operating conditions, will survive for a stated period of time. The 'normal operating conditions' include the total physical environment including mechanical, thermal and electrical conditions. The term survive means that the item does not fail. Failures may be related to the design and use of a particular product, or they may be related to the manufacturing process or to the unpredictable man-made or nature determined events in their final operating environment [Jens95]. For the reputation of the manufacturer, it is very important for him to have a good knowledge of the reliability of his products.

IC's are incredibly complex modules with millions of electronic components. They can be divided in two different types: active and passive components. Active components are mainly transistors and diodes. Passive components can be capacitors or on-chip interconnections. Capacitors are used in order to store charges in an IC. On-chip interconnections are needed for the interconnection between active components. Other commonly used names for on-chip interconnections are metal stripes or simply lines. The failure of one component can be sufficient to destroy the complete IC. The reliability of a product thus starts with a study of the reliability of the basic components on the IC's in the product. Then, with this knowledge, the reliability of the complete IC can be estimated and this finally leads to an estimation of the reliability of the product.

1.2. The subject of this thesis

This thesis deals with the study of the reliability of one specific type of electronic component, the Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET). MOSFETs have been in use since the beginning of the sixties. They have several advantages:

- The LOCOS (Local Oxidation of Silicon) isolation enables the separation of devices.
- The structure has superb scaling possibilities.
- The use of n-type and p-type devices on the same substrate allows building circuits with complementary MOS structures (CMOS), which results in ultra-low power consumption.

These advantages have made the MOSFET the basic building block of semiconductor

very-large-scale integration (VLSI) and ultra-large-scale integration (ULSI) products, such as memory cells and microprocessors.

Figure 1-2 shows a cross-sectional view of the conventional n-channel MOS (nMOS) transistor structure built on a p-type substrate. An n-type silicon (n stands for negative) is developed by adding pentavalent atoms, such as arsenic and phosphorus, to pure silicon. These atoms donate an extra electron to the silicon. Thus in an n-type semiconductor, the free electrons outnumber the holes. Similar, in p-type silicon, the holes outnumber the free electrons.

The MOSFET has three or four contacts: the source (S), the drain (D), the gate and eventually the substrate. For operation, S and substrate are usually grounded. When the applied gate to source voltage (V_g) is zero, the applied drain to source voltage (V_d) tries to force free electrons from source to drain, but the p-type substrate has only a few thermally produced free electrons. Besides these minority carriers and some surface leakage, the current between source and drain is zero. Therefore, a MOSFET is normally off when V_g is zero.

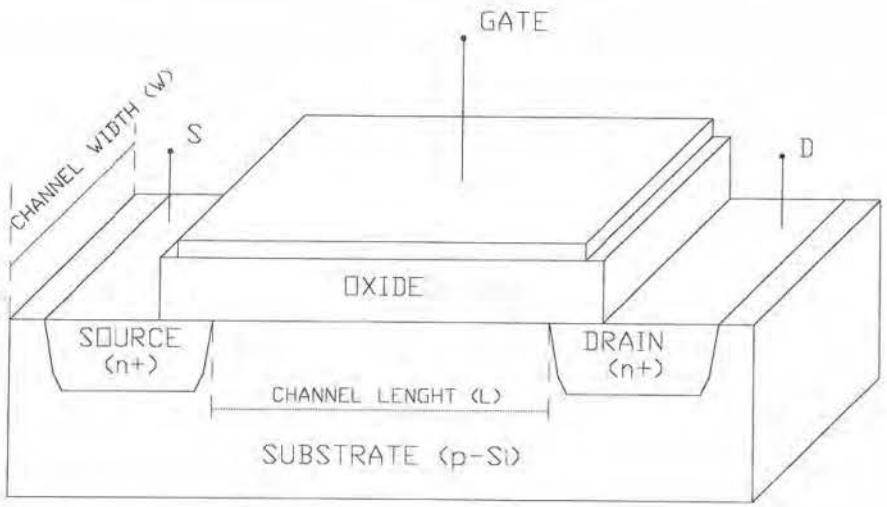

Figure 1-2: Cross-sectional view of the conventional nMOS transistor

When V_g is positive enough, free electrons in the p-region are attracted in the direction of the gate. These free electrons don't have enough energy for crossing the Si-SiO_2 barrier and consequently they will recombine with the holes in the region of the barrier. When these holes are filled, free electrons start to flow from source to drain. This effect

can be compared with the creation of a thin layer of n-type material under the SiO_2. This conducting layer is defined as the n-type inversion layer. When it exists, the normally off device suddenly turns on and free electrons flow easily from source to drain. This flow of electrons from source to drain is called the drain current (I_d). The minimum V_g that creates this n-type inversion layer is called the threshold-voltage (V_t) [Malv93].

The urge for faster and more complex circuits (more functions per chip) as well as requirements of smaller power consumption have driven the MOSFET since its invention to ever smaller dimensions. With the scaling of devices, the power-supply voltages or operating voltages should also decrease if a constant-electric-field-scaling is desired. This enables the reduction of power dissipation and the reduction of the high internal electric fields. However for reasons of speed, compatibility with former process generations,... a non-constant field scaling is obtained in practice. As a consequence, the internal fields in the devices tend to increase. The most important fields in the MOSFET are the transversal field in the gate insulator and the lateral field in the semiconductor near the drain. To a certain extent, this is beneficial, because it increases the carrier velocity and hence the speed of the device. However, there exists a critical field E_C at which the carrier velocity saturates: $E_C=2.10^4$ V/cm for electrons and $E_C=1.10^5$ V/cm for holes in silicon. Thus, increasing the fields beyond this value is no longer useful. In today's short-channel MOSFETs, with typical channel lengths well below 1 μm, the lateral field near the drain exceeds by far this limit, and has become a major source of problems [Here90].

The energy of the carriers, moving horizontally along the channel from source to drain in the high internal fields, increases continuously. High-energetic carriers are also called hot-carriers. Once the energy exceeds 1.1 eV, a collision with a silicon atom can generate an electron-hole pair. This process is called impact ionisation. The created holes are collected by the substrate (and make up the substrate current I_{sub}) while most of the created electrons are attracted toward the drain junction. However, some electrons and holes can gain sufficient energy to surmount the $Si\text{-}SiO_2$ potential barrier and are injected into the gate oxide. These hot-carriers may generate damage to the substrate-insulator interface, but they also may be trapped in the oxide. This results in fixed charge in the oxide and electrically active states at the interface, inducing changes in key MOSFET parameters such as the threshold voltage. So the oxide degradation leads to a deformation of the electrical characteristics of the MOSFET which has a negative influence on its function in the IC. When a certain level of oxide degradation is reached, the MOSFET is unable to execute this function and as a consequence, the total IC will fail.

A major problem when testing the reliability of MOSFETs under hot-carrier injection is that under normal operating conditions, where V_d equals the power supply voltage V_{dd}, the oxide degradation occurs very slow and it can take many years to determine the lifetime of a device. It is therefore necessary to use accelerated ageing: by increasing V_d during the test, oxide degradation is accelerated and lifetime determination is only a question of hours instead of years. A stress condition is created in order to accelerate the ageing of the MOSFET. When using accelerated ageing, a lifetime model is necessary for the determination of the device's lifetime at operating conditions.

The hot-carrier related instabilities due to the degradation of the gate oxide and the interface have been a major reliability concern over the past few decades. In order to enable scaling down of the MOSFET dimensions while keeping the required lifetime to the desired value, several solutions have been proposed [Here90]:

1. Reduction of the operation voltage: The semiconductor device manufacturing industry is not keen on reducing V_{dd}, mainly because of compatibility requirements. Yet, the urge for a reduction of the operation voltage has become stronger than the forces for conservation of the 5 V standard, and as a result the operation voltage has already been reduced and will decrease further in the future.

2. Improved gate insulators: The quality of the gate insulator is a key parameter that determines the hot-carrier resistance of devices and circuits. A continuous search for better insulators has resulted in some new developments. This subject is beyond the scope of this work and will not be discussed here.

3. Drain engineering: The hot-carrier generation in the channel near the drain can be reduced by reducing the high lateral electric field at this place. This field can be reduced under constant voltages by reducing the doping concentration of the drain, and providing a smooth junction instead of an abrupt one. It is also important to keep this region of reduced concentration under control of the gate, because otherwise any degradation of this region strongly effects device characteristics. Therefore, the conventional MOSFET, with a highly doped As or P junction, is replaced by the LDD MOSFET, with a lightly doped drain. Here, an n^- region underneath a spacer oxide connects the channel to the highly doped junction. This structure, however, does not always allow gate-control of the n^- region. An optimisation has to be carried out for the n^- implantation dose and for the shape of the spacer in order to obtain optimum hot-carrier immunity. Although the LDD structure is widely used in today's MOSFET technologies, it may be necessary to

develop new structures for tomorrow's ultra short-channel MOSFETs. A detailed discussion on these LDD structures will be given in chapter 4.

4. Hot-carrier-immune circuit design: It has become clear that a clever design can significantly improve the reliability of circuits against hot-carrier instabilities. From the calculation of the lateral field in the MOSFETs of a circuit, a prediction of the corresponding hazards can be made. Effective solutions can then be provided by appropriate circuit design. In this work, only single devices will be studied. The hot-carrier degradation on circuit-level is beyond the scope of this thesis.

All proposed solutions are based on a clear understanding of the fields in MOSFETs, of the mechanisms by which carriers are injected into the gate insulator and of the instabilities resulting from the hot-carrier injection. It is the aim of this work to contribute to this understanding, especially in the last domain.

1.3. Motivation of this work

During the last 20 years, hot-carrier phenomena in nMOSFETs have been studied intensively. In the beginning, attention was focussed on conventional nMOSFETs, with a highly doped drain structure. Today, the degradation of these conventional nMOSFETs is quite well understood and some good models for describing the degradation behaviour and for determining the lifetime of the device at the operating conditions have been developed. LDD nMOSFETs introduced new degradation mechanisms that are associated with the spacer oxide above the n^- region. Although a generally accepted picture of the physical degradation mechanisms exists, a lot of work needs to be done concerning the development of a generally accepted model for these devices.

Figure 1-3 shows a typical degradation behaviour of an nMOSFET. The drift in terms of percentage of a typical MOSFET parameter is given as a function of stress time. All typical MOSFET parameters will be discussed in the next chapter. The presented measurement has been performed using a commercial measurement system. Several devices were measured at the same stress condition (blue lines). The mean (green line) and the median (red line) behaviour are also shown. With a failure criterion of 10 %, the lifetime of these devices at this stress condition is approximately between 150 and 600 hours. Notice that the first measurement point is taken after about 10 hours of stress. This is because the measurement resolution of the commercial available test systems is about 0.5 %. So, the MOSFET parameter needs to drift more than 0.5 % in order to be

detectable. Consequently, the degradation behaviour at small stress times and at small degradation levels can not be studied with these test systems. Because a relatively high degradation is required, the stress conditions need to be much higher than the operating conditions. These high stress conditions can generate degradation mechanisms which do not occur at the operating conditions.

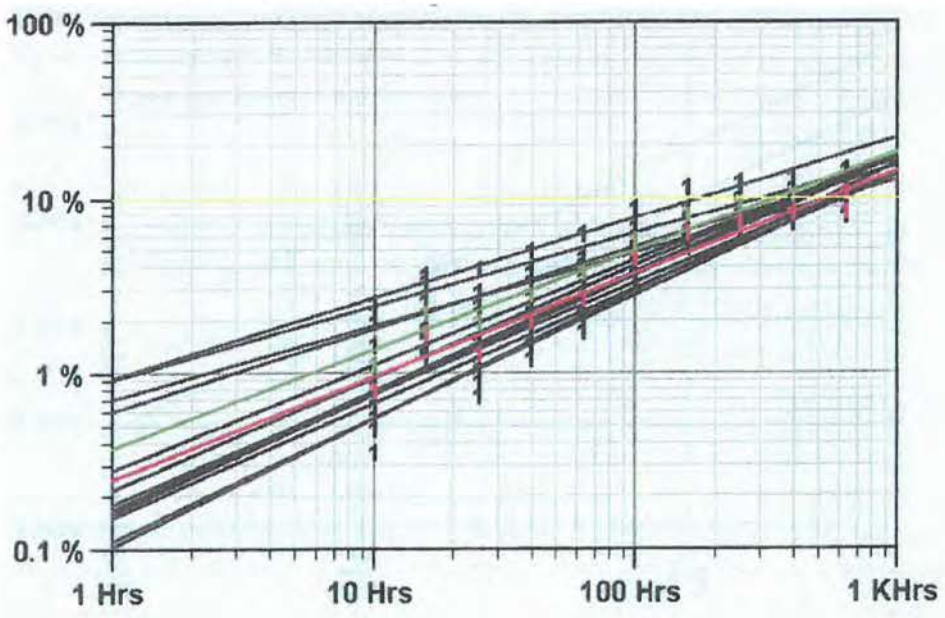

Figure 1-3: Percentage degradation of a characteristic MOSFET parameter as a function of stress time measured with the classical measurement technique.

The unknown initial degradation area and the high stress conditions leave some questions unanswered:

- What are the degradation mechanisms in the initial degradation phase ?
- How is the behaviour of the initial degradation as a function of time ?
- Are new failure mechanisms introduced when high stress levels are applied ?

It is the aim of this work to answer these questions. Therefore, a new measurement methodology will be developed in order to perform degradation measurements with a high measurement resolution. With these results, the existence of an offset voltage can be checked. Further, the degradation mechanisms of the initial degradation phase can be recognised and the initial degradation behaviour as a function of time can be measured.

Finally, the existing extrapolation techniques can be checked with the measurements at the lower stress conditions, close to the operating conditions.

In this work, two kinds of MOSFETs will be studied: conventional nMOSFETs and LDD nMOSFETs. Because the degradation behaviour of conventional devices is well known, the only new aspect that can be added is the degradation behaviour at low stress times and at low degradation levels in order to answer the above questions. For LDD devices, no generally accepted model exists and it is the aim of this work, except answering the above questions, to develop a model for the complete degradation region: from 0.02 % up to 10 %.

Most of the measurements will be done on wafer-level. One wafer contains hundreds of devices. Packaging of devices has several disadvantages: it is time and money consuming and there is always a risk of damaging the device. The outline of this thesis is now presented in view of the goals described above.

1.4. Outline

Chapter 2 describes the high-resolution measurement technique (HRMT), developed to perform high-resolution measurements on the hot-carrier degradation of nMOSFETs. First, the characteristic MOSFET parameters, which will be used as degradation parameters, are defined. Then, the measured set-up, which can be used to measure packaged devices and wafers, is shown. The chapter continues with a description of the measurement procedure. This section starts with a description of the measurement cycle and the extraction of the degradation parameters. Then, the measurement resolution is determined. This measurement resolution is still influenced by temperature fluctuations. There are two ways to increase this resolution: correcting for the temperature fluctuations or stabilising the temperature in the MOSFET environment. The temperature correction method can be divided in two steps: first the determination of the temperature coefficient (TC) and then the correction of the measurement for the temperature fluctuations. However, for avoiding the temperature fluctuations, the device under test (DUT) can be placed in a protective chamber with stabilised temperature. With the aid of this technique, degradations of nMOSFETs under hot-carrier stress as low as 0.02 % can be measured.

In chapter 3, the hot-carrier degradation of conventional nMOSFETs is studied. After an introduction, the hot-carrier degradation mechanisms, which are known and described in the literature, will be discussed. Then, the degradation measurements on a

conventional 2.4 μm wafer technology will be described. The model of Takeda and the model of Hu are well accepted for the description of the degradation behaviour and for the determination of the lifetime of conventional nMOSFETs. These models are described and applied to the conventional wafer technology by using the least-square estimation (LSE). In this work, a new lifetime prediction procedure is proposed. The chapter ends with a description of the advantages of the HRMT concerning the detection of physical degradation mechanisms, the accuracy of the lifetime prediction and the reduction of the test times in comparison with the "classical" measurement techniques. These advantages are proved by Monte-Carlo simulations.

Chapter 4 contains a detailed study of the design and degradation of the LDD nMOSFET. First, the LDD structure is shown and the need for this new structure is explained. Then, the degradation measurements on three different wafer technologies are shown. This degradation behaviour is much more complicated than in the case of conventional nMOSFETs. Thus, the model of Hu can not be used anymore. An overview of the different studies of the hot-carrier degradation of LDD nMOSFETs is given. In a next step, a new degradation model, based on the model of Goo et al. [Goo95] and Chan et al. [Chan95] has been developed. The new model has been verified on the three different wafer technologies.

The conclusions of this work will be presented in chapter 5.

2. The high-resolution measurement technique.

2.1. Introduction

The in-situ accelerated ageing technique with electrical testing was developed by the Institute for Materials Research (IMO) and IMEC [Pate90]. The initial goal of this technique was to study the electrical behaviour of a given material during thermal annealing, as a function of temperature, time, ... With this technique, a test structure can be submitted to a desired temperature profile and the electrical property of interest can be measured continuously during the thermal treatment, i.e. in-situ.

In the beginning, the method has only been used to study accelerated ageing of material systems of which the ageing can be characterised by the DC electrical resistance. A high measurement resolution is obtained: it is in the order of 1 to 5 parts per million (ppm) for a system with a temperature coefficient[1] of 100 ppm/°C, whereas the comparable resolution with the conventional method (off-line) is in the order of 500 ppm [Sche90a]. Therefore, the ageing kinetics of a system can be studied in more detail and on a shorter time scale. Till now, some typical applications of the in-situ technique are hybrid thick film ageing [Sche90b], ageing behaviour of ball bonds [Tiel89], diffusion in thin film resistors [Ceun92], defect relaxation [Ceun90, Stul94a], ageing behaviour of glass-ceramic dielectrics in thick film multilayers [Manc94] and electromigration [Dhae97, Cose99].

Thus, most of the studies performed with the in-situ accelerated ageing technique were done on passive components with temperature as one of the stress parameters. In this work, the technique will be used to study the degradation behaviour of an active component at room temperature. The drain to source voltage V_d is the stress parameter. The commercial available test systems who investigate the hot-carrier degradation of MOSFETs have a measurement resolution of about 0.5 %. This means that a characteristic parameter of the MOSFET should shift more than 0.5 % before the degradation can be detected. To obtain these relatively high degradation levels, either

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[1] The temperature coeficient α is defined by:

$$\Delta R = \alpha\left(T - T_0\right)$$

where ΔR is the resistance change, T is the measured temperature and T_0 is the setpoint temperature.

the test times should be very long or the stress conditions should be very high. Long test times are very expensive and high stress conditions increase the risk of generating other effects than those occurring at normal operating conditions. From a physical point of view, it is impossible to study the initial hot-carrier degradation mechanisms of MOSFETs. A degradation of 0.5% implies that a lot of damage has already occurred in the oxide or in the silicon-oxide interface. A possible incubation period preceding the onset of degradation which could be caused by other mechanisms, cannot be detected with such a poor resolution.

In this chapter, the HRMT is proposed in order to perform high-resolution measurements on the hot-carrier degradation of nMOSFETs. The advantages of such high-resolution measurements are:

- test times can be reduced
- the stress conditions can be lowered in comparison to the measurements performed with the existing, low resolution techniques
- the initial degradation mechanisms can be studied to extend the knowledge of the degradation process

In section 2.2, the characteristic parameters of the MOSFET, which will be used as degradation parameters, are defined. Then (section 2.3), the measurement set-up for measurements on packaged devices and wafers, is shown. Section 2.4 describes the measurement procedure. The last two sections (2.5 and 2.6) describe two ways to obtain a high measurement resolution: correcting for the temperature fluctuations or stabilising the temperature in the DUT-environment. In the last section, conclusions will be drawn.

2.2. The degradation parameters

As described in chapter 1, the oxide degradation of the MOSFET, due to the injection of hot carriers, leads to a deformation of the electrical characteristics that has a negative influence on its function in the IC it is part of. When a certain level of oxide degradation is reached, the MOSFET is unable to execute this function and as a consequence, the total IC will fail.

It was also discussed that when the reliability of nMOSFETs is tested at normal operating conditions, the oxide degradation occurs very slow. It can take many years to determine the lifetime of one device. Therefore, it is necessary to use accelerated ageing. During an in-situ accelerated ageing test, there will be continuously switched between

measurement and stress. During measurement, certain characteristic parameters of the MOSFET are measured: the so-called degradation parameters. Most of these parameters are determined from the I-V characteristics of the MOSFET. Stress means that a high V_d is applied in order to accelerated the oxide degradation.

An accelerated ageing test outputs the behaviour of the degradation parameters as a function of stress time. The lifetime of a DUT is defined as the time that the drift of the degradation parameter exceeds a predefined failure criterion. Finally, with the aid of an appropriate lifetime model, the lifetime at normal operating conditions can be extrapolated.

With the new measurement methodology, 4 degradation parameters can be measured. Two of them ($g_{m,max}$ and $I_{d,lin}$) are determined from the linear region of the I-V characteristic and two (V_t and $I_{d,sat}$) from the saturation region. In what follows, the degradation parameters will be defined.

2.2.1. The MOSFET characteristics

With a constant V_g and an increasing V_d, I_d will increase as long as the difference in potential between a random point in the conducting channel and the gate is higher than V_t. This region is defined as the linear or triode region. One has:

$$I_d = K\left[2\left(V_g - V_t\right)V_d - V_d^2\right] \qquad (2\text{-}1)$$

for $0 < V_d < (V_g - V_t)$ and $V_g > V_t$. The constant K, called the conductance parameter depends on the size and the material properties of the silicon. When V_d is further increased, the difference in potential will drop below V_t and will be to small for keeping the electrons in the channel and maintain the inversion. The MOSFET is in saturation. One has:

$$I_d = I_{d,sat} = K\left(V_g - V_t\right)^2 \qquad (2\text{-}2)$$

for $V_d > (V_g - V_t)$ and $V_g > V_t$ [Hore90].

Figure 2-1 shows the resulting I-V characteristics of an n-MOSFET computed with the theoretical equations (2-1) and (2-2). In reality however, I_d in the saturation region is not constant but increases slowly.

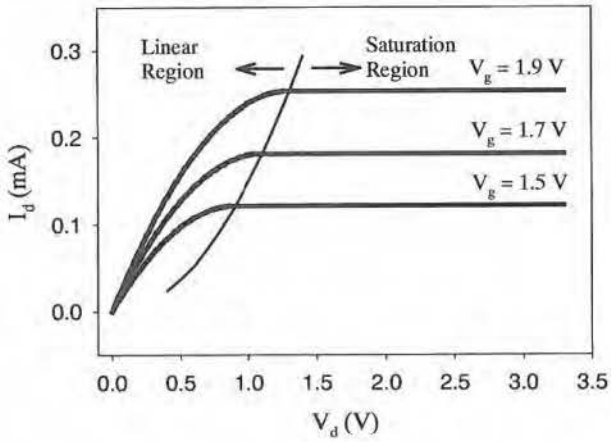

Figure 2-1: Theoretical I-V characteristics of a nMOSFET.

2.2.2. Parameters of the linear region

For defining the parameters in the linear region, V_d is always chosen to be 0.1 V. Figure 2-2 shows the I_d - V_g characteristic at this V_d measured on a packaged nMOSFET with W/L=20μm/2μm from a 0.5 μm technology. The dotted line shows the derivative of the full line. The first parameter, $g_{m,max}$ (unit: mA/V) is defined as the maximum value of the dotted line. The second parameter, $I_{d,lin}$ (unit: mA), defines I_d at a V_g of 3.3 V.

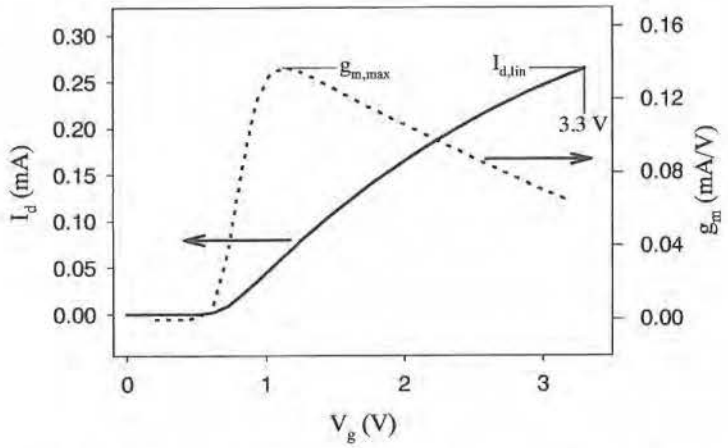

Figure 2-2: The parameters in the linear region of the MOSFET characteristics (V_d=0.1V).

2.2.3. Parameters in the saturation region

For the saturation region, V_d is chosen to be 3.3 V. Figure 2-3 shows the I_d - V_g characteristic at this V_d. The V_g needed to create a channel current of 1 μA is the third degradation parameter, called the threshold voltage V_t (unit: V). The fourth parameter $I_{d,sat}$ (unit: mA) defines the I_d at a V_g of 3.3 V.

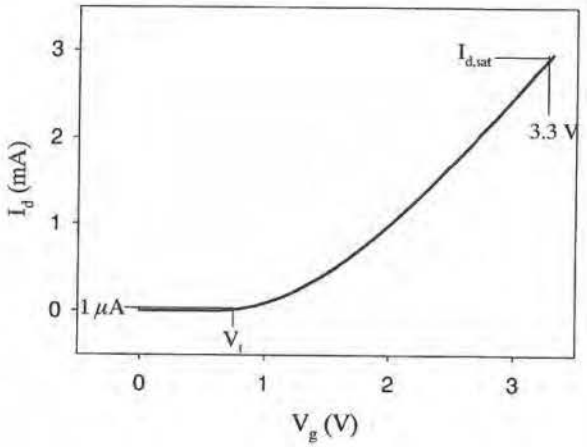

Figure 2-3: The parameters in the saturation region of the MOSFET characteristics (V_d=3.3V).

2.3. The measurement set-up

Figure 2-4 shows a schematic overview of the main parts of the measurement set-up for high-resolution measurements on the hot-carrier degradation of MOSFETs. The measurement equipment is connected to the relay box. This box contains all the relays necessary for the flexibility of the system. From the relays box, a direct connection with the DUT and a PT100 is established. The PT100 is a platinum resistor which will be used to measure the temperature close to the DUT. The DUT can be a packaged device or a wafer and is placed in a protective chamber.

All measurements performed in this work are done at room temperature. The system provides two different ways in order to account for the temperature fluctuations in the room. First, to measure the temperature with the PT100. Then, the measurement of the degradation parameters can be corrected for these temperature fluctuations. Second, it is possible to stabilise the temperature in the protective chamber such that a temperature

correction is not necessary. A disadvantage of this last possibility is that one needs an extra multimeter for performing a continuous measurement of the resistance of the PT100. At the start of this work, the measurements were performed without using the temperature stabilisation. In section 2.5, it will be demonstrated that the temperature correction method shows some drawbacks. All measurements presented in chapter 3 and 4 of this thesis were performed in a stabilised temperature environment.

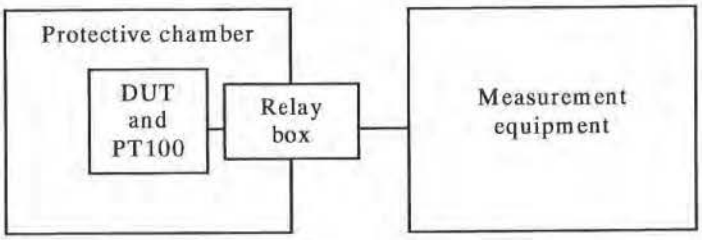

Figure 2-4: Schematic overview of the main parts of the measurement set-up.

Figure 2-5 gives a detailed overview of the measurement equipment:

- Multimeter 1 is needed for the temperature stabilisation in the protective chamber. When this temperature stabilisation is used, the temperature is set to 29.6°C ± 0.03°C as will be discussed in section 2.6. The temperature is stabilised close to the DUT.
- Multimeter 2 both measures the V_g and the voltage over the PT100 close to the DUT, in case the temperature in the protective chamber is not stabilised.
- The current meter is used for measuring the I_d or the I_{sub}.
- The current source sends a current of 1 mA through the PT100. That way, the measured voltage over this PT100 gives a good indication of the temperature fluctuations in the DUT.
- The two voltage sources are used for the application of V_d and V_g.

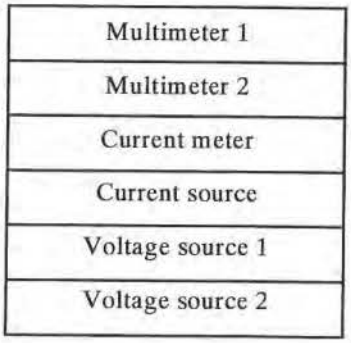

Figure 2-5: Schematic overview of the measurement equipment

Figure 2-6 shows the relay box, which is used for the definition of the correct measurement condition. The aluminium box contains 9 relays (R1-R9) and a multiplexer print (MP):

- R 1 connects drain 1 to V_{d1} or leaves it floating.
- R 2 has the same function for drain 2.
- R 4 connects the substrate with the source or leaves it floating.
- R 8 permits a shortcut between the gate and the source. This is just a safety shortcut in case a new sample is connected or when a potentially 'dangerous' action is performed, e.g. a change in the ammeter range.
- R 9 selects between a voltage source and a function generator at the gate. In this work, this relay always selects a voltage source.
- The other four relays (R 3, R 5, R 6 and R 7) are for the connection of the current meter with the sample. It is possible to measure the I_{sub} and the I_d. The I_d can be measured at the source or at the drain.
- MP switches the multimeter between measuring the voltage over the PT100 and the gate voltage.

The complete measurement cycle is explained in section 2.4.1.

The output of the relay box (upper line of the figure) is connected to the DUT. In case of a wafer, coax cables are connected to the wafer probe. With packaged devices, coax cables are connected to the sample holder.

A schematic overview of the measurement circuit is depicted in Figure 2-7. A large flexibility is obtained thanks to the relays. Examples of this flexibility are the fact that it is possible to measure one or two samples, the ability of the system to measure I_{sub} or I_d, the fact that this I_d can be measured at the source or at the drain and that a normal voltage source or a function generator can be applied to the gate.

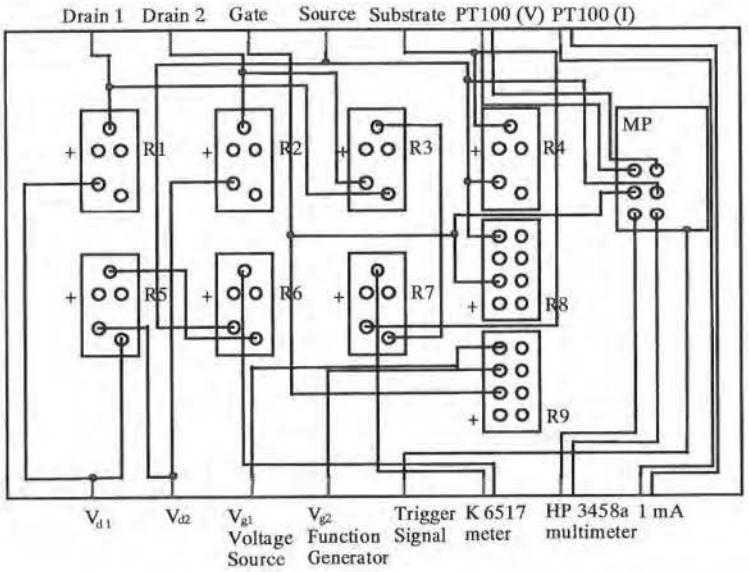

Figure 2-6: Schematic overview of the relais box of the set-up

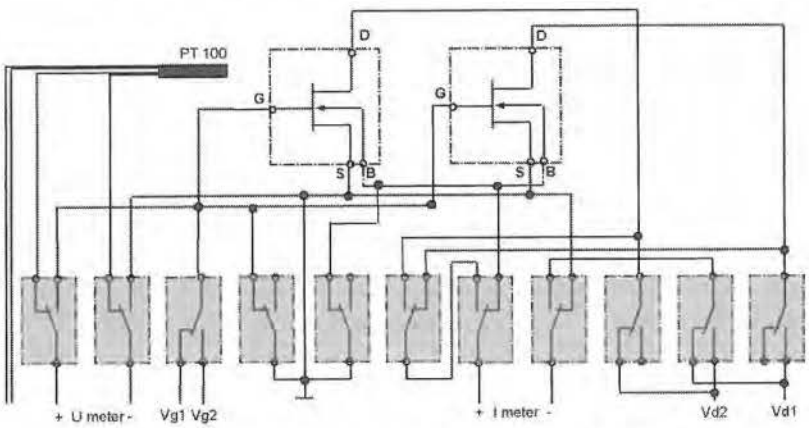

Figure 2-7:Schematic overview of the measurement circuit

Performing high-resolution measurements on nMOSFETs is not straight forward. During this work, the total testbench has to be protected from environmental influences. During the development of the new measurement methodology certain inabilities of the measurement equipment have been detected. These inabilities, and the build-in safeties to eliminate them are described in appendix A.

2.4. The measurement procedure

In the previous sections, it was discussed which parameters are of importance for the determination of an nMOSFET's lifetime. Then, the measurement equipment and the measurement circuit have been described. In this section, it will be explained in detail how this equipment has been used for measuring the degradation parameter of interest.

First, the procedure for measuring I_d-V_g curves, that has been used in this work, will be explained. Then, it is shown how the degradation parameters are extracted from these curves. Finally, the measurement resolution will be shown.

2.4.1. The measurement cycle

The parameters, discussed in 2.2, are determined from the I_d-V_g curve. For measuring this curve, a new methodology has been developed. This methodology will be explained now.

It is very important to mention that a measurement resolution strongly depends on the temperature stability in the DUT during measurements. The higher this stability, the better the resolution will be. Therefore, it is important that the internal temperature of the component does not change too much during the measurement. Due to Joule heating, this internal temperature increases when a current starts to flow through the channel. Therefore, the time that a current flows through the channel, and thus the time that the gate voltage is on, should be as small as possible.

Figure 2-8 gives a schematic representation of the measurement cycle for measuring one point of the I_d-V_g curve.

- Figure 2-8 (a) shows the voltage measurement of the HP 3458a multimeter (multimeter 2 on Figure 2-5) as a function of time. A software trigger is given to the multimeter and then two measurements are performed: the voltage over the PT 100 and the applied gate voltage V_g.

- The reading complete signal of the measurement of the voltage over the PT100 triggers the voltage source at the gate: the gate voltage switches from zero to the desired value (Figure 2-8 (b)).
- The Keithley current meter is also triggered and after a delay of 30 ms the I_d or I_{sub} is measured (Figure 2-8 (c)).
- The reading complete signal also triggers the MP in Figure 2-6 so that the second measurement of the HP 3458a multimeter measures the gate voltage (Figure 2-8 (a)).
- The reading complete of this second measurement triggers the voltage source at the gate: the gate voltage switches back to zero.

Because of this intelligent hardware triggering, the gate voltage is on for only 70 ms and the internal heating of the DUT is thus minimised.

At the end of this measurement cycle, one point of the I_d-V_g curve is measured and a small waiting loop is inserted to eliminate the small internal temperature increase. Using this procedure, the complete I_d-V_g curves are measured, in the linear region as well as in the saturation region. The degradation parameters are extracted from these I_d-V_g curves. This will be explained in the next section.

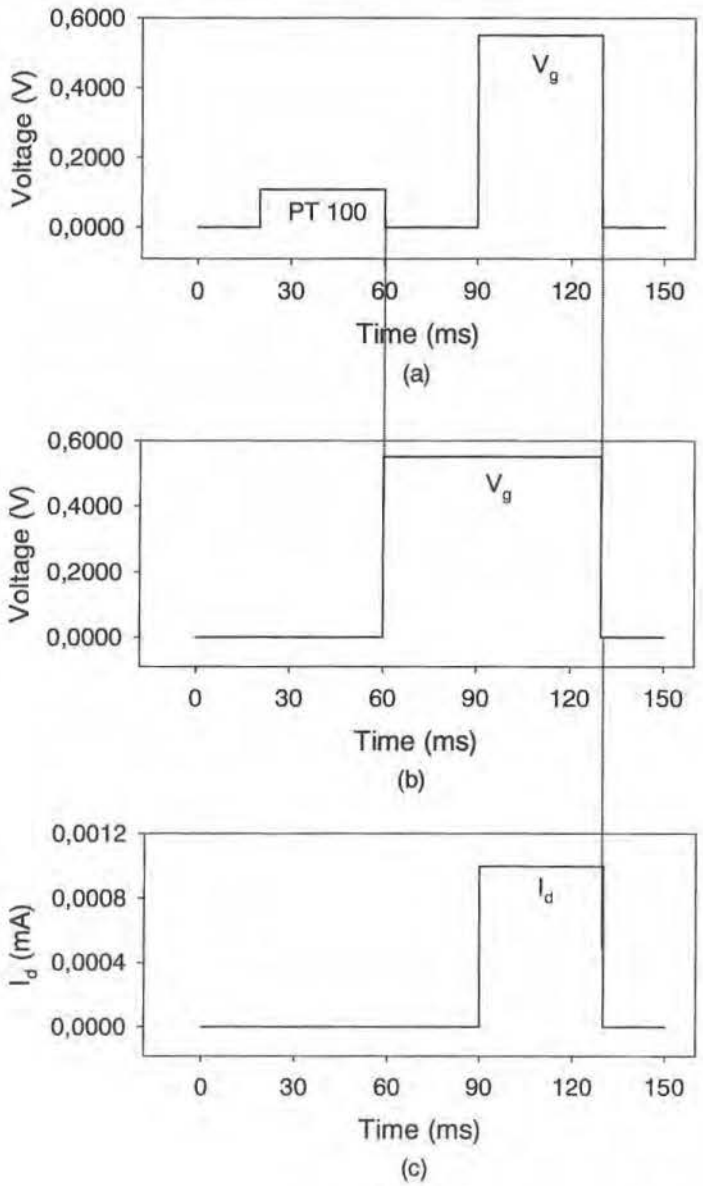

Figure 2-8: Schematic review of the measurement cycle: (a) The multimeter; (b) The voltage source at the gate; (c) The current meter.

2.4.2. Extraction of degradation parameters

The four degradation parameters, $g_{m,max}$, $I_{d,lin}$, V_t and $I_{d,sat}$, described in 2.2, are all extracted from the I_d-V_g characteristics in either the linear or the saturation region. For the determination of these parameters, the I_d-V_g characteristics are not measured completely but only a dense measurement in a small region is obtained. The choice of this region depends on the parameter of interest. For the parameter $I_{d,lin}$, for example, V_d is set to 0.1 V and a V_g from 3.27 V to 3.33 V is applied with a stepsize of 0.001 V. An analogue measurement is done for $I_{d,sat}$, except that V_d is now set at 3.3 V. For the parameters V_t and $g_{m,max}$, an initialisation step is performed in order to set the restricted V_g-region in which a dense I_d-V_g measurement will be performed. During initialisation, the I_d-V_g curve is measured completely, from 0 up to 3.3 V. After the dense measurement in the restricted region, the measurement is fitted to a 4th order polynoom. The desired parameter can then be directly obtained from this fit.

Figure 2-9 shows a measurement and fit of a small area around V_t. In the initialisation step, it has been determined that $V_t \approx 0.56$ V. The gate voltage is stepped from 0.53 V to 0.59 V. This I_d-V_g curve has been fitted to a 4th order polynoom and V_t is found to be 0.5524 V. A similar procedure is used for the determination of $g_{m,max}$.

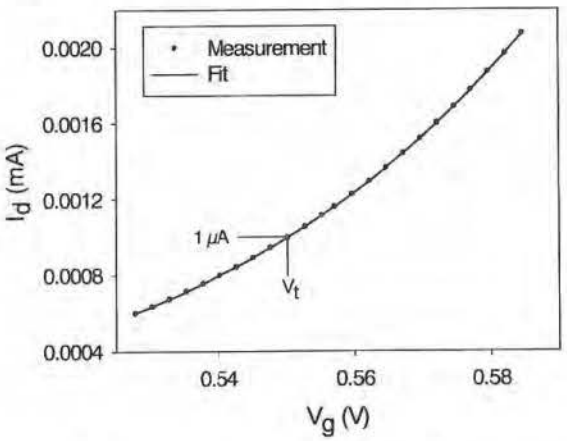

Figure 2-9: Measurement and fit of a small area around V_t

2.4.3. The measurement resolution

The measurement resolution is influenced by different factors. First, it is obvious that the dense measurement of a small region around the desired parameter has a positive influence on the measurement resolution in comparison with the "classical" measurement of the complete I_d-V_g curve. Second, the stability of the voltage supply and the current meter also influences the measurement resolution. The applied V_d and V_g and the measurement of the current can be stabilised by using highly accurate measurement equipment. Therefore, the voltages are supplied by a HP 3245 A and the current is measured by a Keithley 6517.

In order to determine the resolution of the method, a characterisation measurement has been executed on packaged samples from a 0.5μm technology. This is done by measuring all four parameters of the MOSFET several times without stressing the device. Figure 2-10 shows the result of this measurement for the parameter $I_{d,lin}$ for a sample with W/L=15μm/0.7μm.

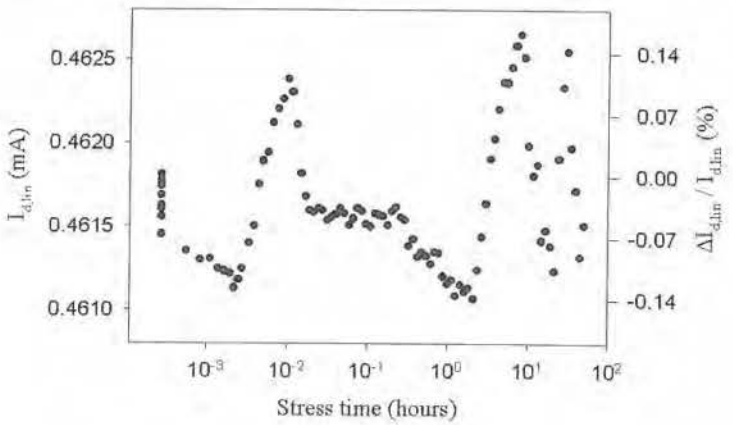

Figure 2-10: Left axis: $I_{d,lin}$ as a function of time
Right axis: Relative change of $I_{d,lin}$ in ppm

The calculated resolution of 0.5 % for the "classical" method can be improved down to less than 0.3 % peak-to-peak. It is obvious from this figure that the measurement resolution from point to point is much better than 0.3 %. There is one factor which is still influencing the measurement resolution. In the next section it will be shown that the temperature fluctuations are responsible for this influence.

The problem of controlling the influence of temperature can be approached by using two different procedures. First (section 2.5), the temperature will be measured with a platinum resistor (PT100), which is mounted close to the DUT, in order to correct the measurement for the temperature fluctuations. Second (section 2.6), the temperature in the DUT-environment will be stabilised and thus the temperature correction is not necessary anymore.

2.5. Obtaining a high resolution: temperature correction

A PT100 is mounted close to the DUT in order to measure the internal MOSFET temperature as good as possible. The Joule heating in the MOSFET is minimised by applying the V_g for only 70 ms. Therefore, the only fluctuations in the MOSFET temperature are caused by room temperature fluctuations. The measurements can be corrected for these temperature fluctuations as will be shown in this section.

2.5.1. The correlation between characterisation measurement and temperature

In the previous section, it has been shown that the point-to-point measurement resolution is much better than the long-term resolution of 0.3 %. It will now be shown that the long-term fluctuations are caused by fluctuations of the room temperature. To do this, the same measurement as shown in the previous section (Figure 2-10) will be used. During this measurement, the temperature in the room was measured close to the DUT with a PT100.

The results of the measurement is shown in Figure 2-11. The left figure shows the temperature fluctuations in the room measured by a PT100 as a function of time. The right figure shows the behaviour of $I_{d,lin}$ as a function of time.

From these two figures, it can be concluded that the property behaviour is inverse proportional to the temperature behaviour. Now, it will be shown how this measurement can be corrected for the temperature fluctuations.

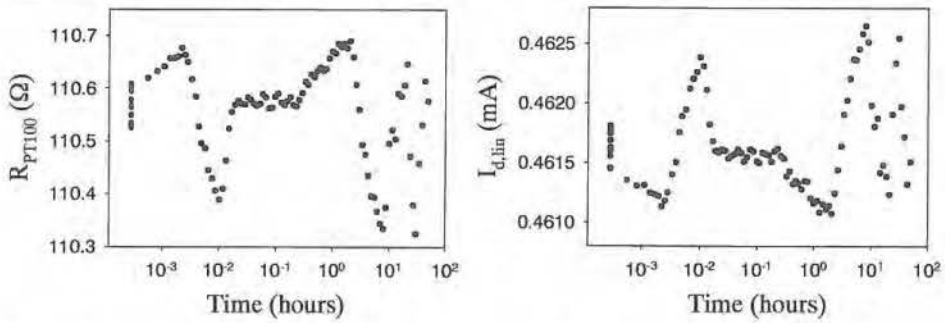

Figure 2-11: Room temperature fluctuations as a function of time during a dummy stress period (left); $I_{d,lin}$ as a function of time, not corrected for temperature (right).

2.5.2. The temperature correction method

The temperature correction method can be divided into two parts: first, the TC needs to be determined. Second, with the aid of this TC, the degradation measurement needs to be corrected for the temperature fluctuations.

2.5.2.1. Determination of the TC

When the DUT degrades, the change in property is given by:

$$\Delta P(t) = \Delta f(t) + TC\,\Delta T(t) \qquad (2\text{-}3)$$

where f is the unknown degradation model which is a function of the stress time t, thus Δf is the change in f for a given time interval and ΔT is the corresponding change in temperature. From equation (2-3) the TC can be determined with the LTSCA method [Pate96]. However, in practice, it does not work very well in our case. This can be due to the fact that:

- the time axis is logarithmic in hot-carrier degradation measurements
- the frequency of the temperature changes of the room temperature is about the same as the frequency of the property changes

Therefore, in our case, the TC will be determined from a characterisation measurement. This is a measurement without stress, so that all the fluctuations of the degradation parameters are due to the temperature fluctuations.

With the aid of simulations, it will be shown that the TC can be correctly determined from two types of temperature behaviour: an oscillating temperature around a certain

setpoint and an increasing temperature.

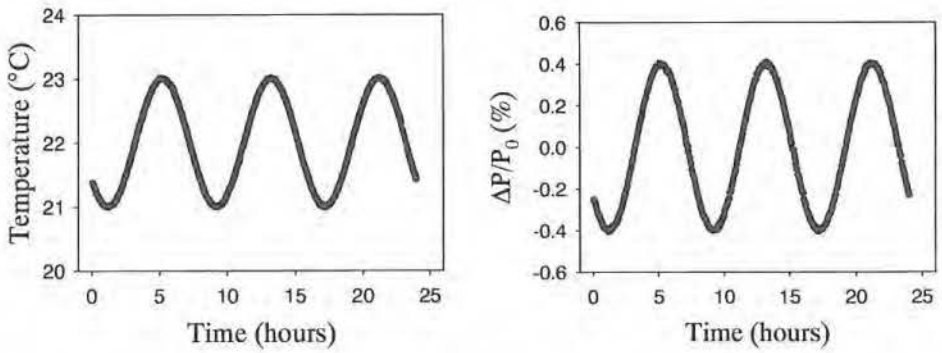

Figure 2-12: Simulated temperature behaviour during 1 day (left); Corresponding property behaviour during 1 day (right).

The left part of Figure 2-12 shows a simulated temperature behaviour during one day. The temperature behaviour is taken to be a sine with a period of 8 hours and an amplitude of 1 °C. The short-term temperature is taken to be normally distributed with a standard deviation of 0.05°C divided by 6. This implies that 99 % of the short-term temperature measurements are within 0.05 °C.

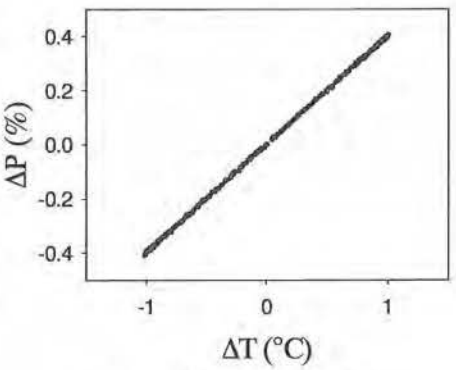

Figure 2-13: ΔP versus ΔT

The right part of Figure 2-12 shows the behaviour of the property of interest assuming that no drain voltage stress is applied. This behaviour is calculated as a sum of two terms:

1. Temperature: a TC of 4000 ppm/°C is used, which is a good estimation of the TC of the parameter $I_{d,lin}$ of the nMOSFETs used in this work. Using this TC, this term can be calculated directly from the left part of Figure 2-12.
2. Measurement noise: the determination of the property is also influenced by several other factors such as stability of voltage supply, … The noise introduced by those factors is assumed to be normally distributed with a standard deviation of the measurement resolution divided by 6. This means that 99 % of the short-term measurements are within the measurement resolution, which is 200 ppm in this case.

Figure 2-13 shows the plot of ΔP versus ΔT. A straight line is obtained and the TC is defined as the slope of this line. In this example, a TC of 3981 ppm/°C is obtained which is close to the setted value.

In practice, the room temperature does not always fluctuate like a sine around a certain setpoint. The next simulated temperature behaviour, not fluctuating around a certain setpoint but slightly increasing, is also possible in practice.

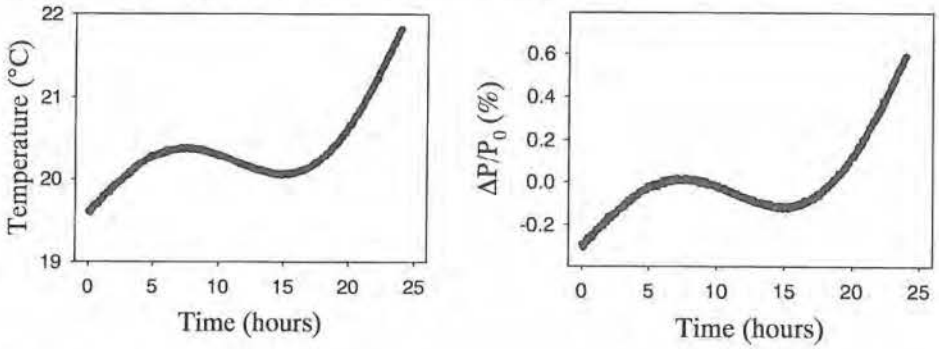

Figure 2-14: Simulated temperature behaviour during 1 day (left); Corresponding property behaviour during 1 day (right).

The left part of Figure 2-14 shows again a simulated temperature behaviour during one day. The temperature behaviour drifts away from its setpoint. The temperature increases from 20 °C up to almost 22 °C. The short-term temperature is again assumed to be normal distributed with a standard deviation of 0.05°C divided by 6.

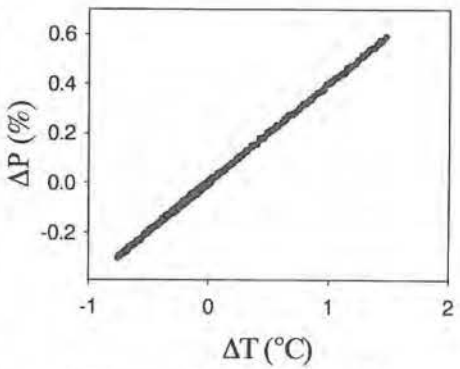

Figure 2-15: ΔP versus ΔT

The right part of Figure 2-14 shows the behaviour of the property of interest assuming again that no drain voltage stress is applied. This behaviour has again been calculated as a sum of the two terms introduced above, assuming a TC of 4000 ppm/°C.

Figure 2-15 shows again the plot of ΔP versus ΔT. A straight line is obtained and the TC is equal to 4120 ppm/°C which is again close to the setted value.

2.5.2.2. Correction of the degradation measurement

Once the TC has been determined from a characterisation measurement, it can be used to correct a degradation measurement for the temperature fluctuations. This will be shown in this section, again for two types of temperature behaviour: one fluctuating around a certain setpoint and one increasing temperature behaviour.

The left part of Figure 2-16 shows the same temperature behaviour as the left part of Figure 2-12, except that it is now shown on a logarithmic scale. In the right part, the simulated property behaviour is shown. In contrast to the previous simulations, the DUT is now degrading according to $A.t^n$ where t is the stress time and A and n are two fit parameters. This behaviour is often observed when a hot-carrier stress is applied on nMOSFETs as will be shown in the next chapter. Again, a short-term fluctuation which represents the instability of the measurement equipment is added.

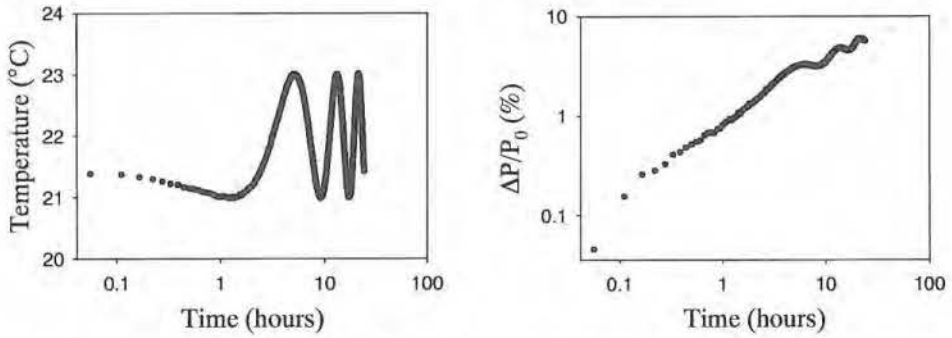

Figure 2-16: Simulated temperature behaviour during 1 day (left); Corresponding property behaviour during 1 day (right).

Figure 2-17 shows the comparison between the theoretical property (line), and the property measurement (full dots), corrected for the temperature fluctuations. The correction has been done with a TC of 3981 ppm/°C, as it was determined from the characterisation measurement. There is no significant difference between both plots and this means that the temperature correction worked fine in this case.

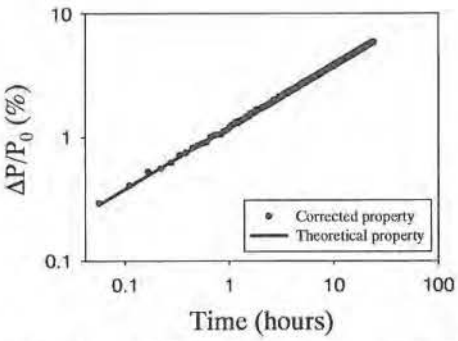

Figure 2-17: Corrected property behaviour during 1 day (full dots); Theoretical property behaviour during 1 day (line).

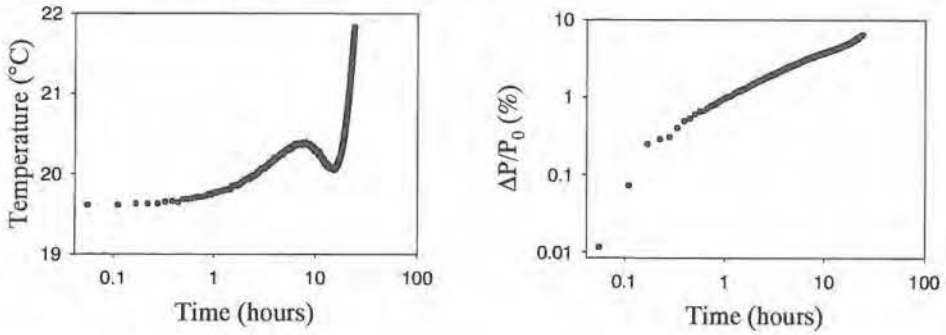

Figure 2-18: Simulated temperature behaviour during 1 day (left); Corresponding property behaviour during 1 day (right).

Is the temperature correction still possible when the room temperature increases monotonically? The left part of Figure 2-18 shows the same temperature behaviour as in the left part of Figure 2-14, except that it is now shown on a logarithmic scale. The property behaviour is shown in the right part of the figure. The property is degrading according to $A.t^n$. Again, a short-term fluctuation which represents the measurement resolution is added.

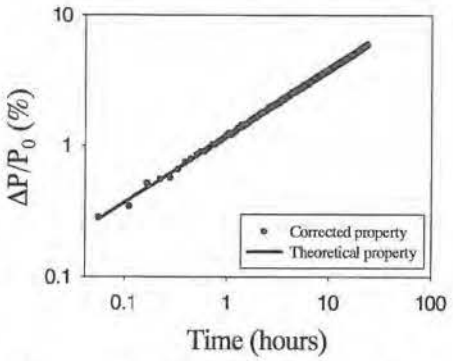

Figure 2-19: Corrected property behaviour during 1 day (full dots); Theoretical property behaviour during 1 day (line).

Figure 2-19 shows the comparison between the theoretical property (line), and the property measurement (full dots), corrected for the temperature fluctuations. The correction has been done with a TC of 4120 ppm/°C, as it was determined from the characterisation measurement. There is again no significant difference between both plots and this means that the temperature correction worked fine in this case.

2.5.2.3. Measurement with temperature correction

Once the temperature correction method is known, the measurement, shown in section 2.5.1, can be corrected for the room temperature fluctuations. The result is shown in Figure 2-20. The left part of this figure shows the behaviour of the room temperature, as it was measured by a PT100 mounted close to the DUT. The right part

shows the behaviour of the parameter $I_{d,lin}$. The full dots represent $I_{d,lin}$ not corrected for temperature while the open dots stand for the corrected measurements. The right axes shows the deviation in ppm. The measurement resolution of 0.3 %, obtained without temperature correction, can be improved down to less than 200 ppm after the correction for the temperature fluctuations.

Similar plots concerning the other three parameters give comparable results. The resolution of the corrected measurement is below 500 ppm for $g_{m,max}$ and well below 200 ppm for both V_t and $I_{d,sat}$.

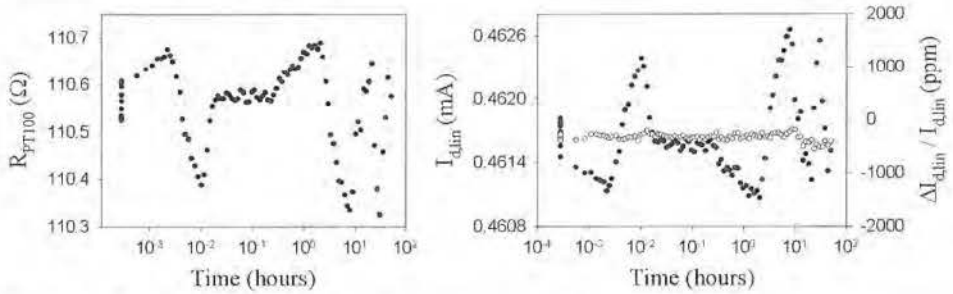

Figure 2-20: Room temperature fluctuations as a function of time during a dummy stress period (left); $I_{d,lin}$ as a function of time not corrected for temperature (right, left axis, full dots); $I_{d,lin}$ as a function of time corrected for temperature (right, left axis, open dots); Relative change of $I_{d,lin}$ in ppm (right, right axis)

2.5.2.4. Conclusion of the temperature correction

Correcting a degradation measurement for temperature fluctuations needs to be done in two steps: first, the TC has to be determined from a characterisation measurement and then, with this TC, the degradation measurement can be corrected. This procedure has some disadvantages:

1. The TC can not be determined exactly from a characterisation measurement.
2. It is assumed that the TC does not change during a degradation measurement.
3. It is assumed that the change in property is a linear function of the change in temperature.

The simulations of this section and the field-experience show that the temperature correction works fine. Although, in this academic work, no risk is taken. Therefore, from now on, the temperature in the DUT-environment will be stabilised and then, no temperature correction needs to be performed.

2.6. Obtaining a high resolution: stabilised temperature

From now on, the DUT will be placed in a protective chamber and the temperature in this chamber will be stabilised. Therefore, a heating element is placed in the protective chamber. The current through this heating element is provided by a DC-stabilised voltage source. The same PT100 as in the previous section is used to determine the temperature close to the DUT. The resistance of this PT100 is now measured with an additional high-precision multimeter (multimeter 1 on figure 2-5) because this resistance needs to be measured continuously. From this value, the related temperature value is calculated. If this temperature deviates from setpoint, the voltage of the source of the heating element is regulated. This regulation is calculated by a PID-regulation algorithm [Min88, Cool69]. Details about the optimal PID-parameters and the application of the algorithm are stated in papers of De Ceuninck et al. [Ceun90] and Stulens et al. [Stul94b].

The temperature stabilisation will be performed slightly above room temperature, at 29.6 °C. The temperature stabilisation is higher than 0.03°C. This is demonstrated in Figure 2-21, where the temperature in the protective chamber is plotted as a function of time. When the temperature in the protective chamber is stabilised, it is no longer necessary to measure and correct for the temperature fluctuations as in the previous section.

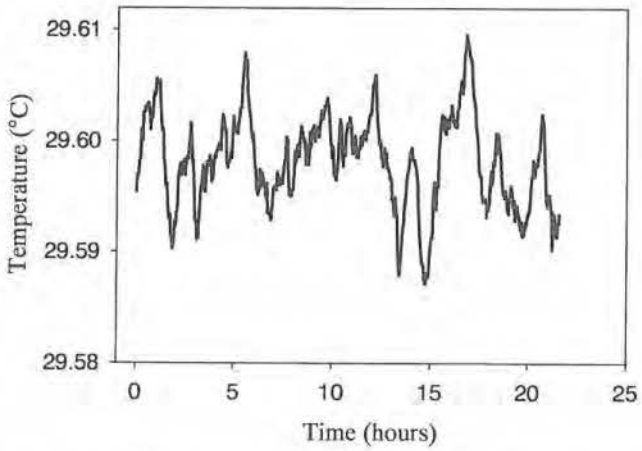

Figure 2-21:Temperature stabilisation in the protective chamber surrounding the DUT during a measurement of 1 day.

The measurement cycle and the method for the extraction of the degradation parameter are exactly the same as in the previous section.

2.6.1. Determination of the resolution

In order to determine the resolution of the method, again a characterisation measurement has been executed. This time, on a wafer from a 0.5μm technology. This is done by measuring all four parameters of the MOSFET several times without stressing the device. The left part of Figure 2-22 shows the result of this measurement for the parameter $I_{d,lin}$ for a sample with W/L=2μm/1μm. The right part of the figure represents the measurement corrected for room temperature fluctuations shown in the right part of Figure 2-20. The results are comparable.

The temperature around the DUT is stabilised at 0.03°C. With a TC of approximately 4000 ppm/°C, the maximum parameter change due to a temperature fluctuation is 120 ppm. Thus, the temperature fluctuation is no longer the crucial factor that determines the measurement resolution. Other factors such as cabling can play a role of importance.

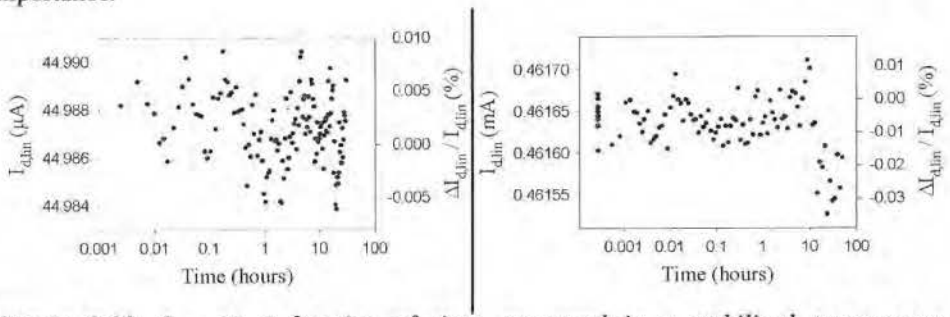

Figure 2-22: $I_{d,lin}$ as a function of time, measured in a stabilised temperature environment (left, left axis); Relative change of $I_{d,lin}$ in % (left, right axis); $I_{d,lin}$ as a function of time, the measurement is corrected for room temperature fluctuations (right, left axis); Relative change of $I_{d,lin}$ in % (right, right axis).

The measurement resolution of the parameter $I_{d,lin}$ is 200 ppm peak to peak. Similar plots concerning the other three parameters give comparable results. The resolution of the corrected measurement is below 500 ppm for $g_{m,max}$ and well below 200 ppm for both V_t and $I_{d,sat}$.

2.7. Conclusions

In this chapter, the high-resolution measurement technique (HRMT) is proposed to perform hot-carrier degradation measurements on packaged or wafer-level nMOSFETs.

The degradation parameters are extracted from the MOSFET I-V characteristics. In order to determine a parameter, the I-V characteristic is not measured completely but only a dense measurement in a restricted region around the desired parameter is executed with highly accurate measurement equipment.

To obtain a high measurement resolution, the temperature needs to be controlled. First, the measurement procedure is developed in order to minimise the time that a current flows through the channel and thus the time that the gate voltage is on. Then, there are two ways to control the temperature:

- Correction of the degradation measurement for the room temperature fluctuations This is done in two steps: first the determination of the TC from a characterisation measurement and then the correction of the degradation measurement for the temperature fluctuations with this TC.
- Stabilisation of the temperature in the DUT-environment.

In this work, the second method will be used. Therefore, the DUT will be placed in a protective chamber and the temperature in this chamber will be stabilised at 29.6 °C with a stability of 0.03 °C.

With this HRMT, the calculated resolution of 0.5 % for the "classical" method can be improved down to less than 200 ppm.

3. The Hot-Carrier Degradation of Conventional nMOSFETs.

3.1. Introduction

In this chapter, the HRMT will be used for the study of the hot-carrier degradation of conventional nMOSFETs. This is a rather old MOSFET technology which has been studied intensively during several years. Today, it is hardly used anymore in submicron technologies because desired lifetimes are not reached anymore with these conventional MOSFETs. In other applications, such as power MOSFETs, this technology is still used today. In the next chapter, a more recent technology for submicron MOSFETs will be studied.

The hot-carrier degradation of conventional nMOSFETs has been studied intensively for several years. Therefore, this chapter will start with an overview of the physical degradation mechanisms. Then, high resolution measurements, performed on a conventional 2.4 μm wafer technology, will be shown. Next, a description of two widely used models, the model of Hu and Takeda, will be given and these models will be applied to the measurements. The chapter will end with an overview of the advantages of the high-resolution measurements when measuring conventional nMOSFETs.

3.2. The hot-carrier degradation mechanisms of conventional nMOSFETs

In this section, the different mechanisms of how hot carriers can be injected into the SiO_2 will be described. Then, the possible damages that can be created by these hot carriers, are explained. The major part of these two sections are based on Leblebici et al. [Lebl93] and Groeseneken et al. [Groe99]. Finally the dependence of this damage on the V_g during stress will be shown.

In general, hot carriers in a semiconductor material are defined as those carriers (electrons and holes) that have a much higher kinetic energy than the average carrier population. The concept of hot carriers can be illustrated by comparing the kinetic energies and the corresponding carrier temperatures with those for carriers in thermal equilibrium. The electrons in a semiconductor material in thermal equilibrium have energies E slightly higher than the bottom of the conduction band E_c and $E-E_c \sim kT$

where T is the device temperature and k is Boltzmann's constant.

Under nonequilibrium conditions, carriers possessing kinetic energies larger than the thermal equilibrium contribute to a current flow. However, carriers moving in quasi-neutral regions gain only a small amount of kinetic energy, so that their energy does not deviate significantly from kT. If the carriers encounter a large electric field, on the other hand, such as the electrons moving along the channel of a nMOSFET, their kinetic energies increase in a relatively short distance. The kinetic energy of an accelerated electron can be expressed by $E-E_c = kT_e > kT$, where T_e is the effective electron temperature.

Thus, high-energy electrons and holes are described as "hot" carriers, referring to their effective temperature T_e, which is significantly higher than the temperature of the semiconductor.

3.2.1. Channel hot-carrier injection into the SiO_2

In this section, it will be described how carriers are injected into the SiO_2. Only the injection of hot carriers from the channel will be described, because this is the dominant mechanism when a high V_d is applied. Injection of carriers through Fowler-Nordheim tunnelling or direct tunnelling as well as the substrate hot carrier injection will not be described in this section. More information about these last three injection techniques can be found in Groeseneken et al. [Groes99].

Electrons, constituting the I_d, can become injected into the oxide through quasi-elastic scattering. It is also possible that electrons first create an electron-hole pair in the silicon by impact ionisation. Then, these generated carriers can become injected. Although the difference between these two mechanisms is disputable, they will be treated separately.

3.2.1.1. Scattering of channel hot-electrons into the oxide

Quasi-elastic scattering of electrons into the oxide can be described using the lucky-electron concept as follows. A certain percentage of the electrons moving along the channel from the source to the drain may attain high kinetic energies that enable these hot electrons to overcome the interface potential barrier and enter the gate oxide. In order for channel hot electrons to reach the gate oxide, these electrons must not only gain sufficient energy from the channel electric field, it is also necessary to redirect their momentums towards the $Si-SiO_2$ interface.

To quantify the probability that a hot electron could be injected into the gate oxide, several types of scattering events have to be considered. The first event is the acceleration of the electron by the lateral electric field along the channel. When this hot electron reaches the drain end of the channel, its momentum has to be redirected toward the interface by a collision. This should not be an energy-robbing collision, so that the "lucky" electron will retain the kinetic energy required to surmount the Si-SiO_2 potential barrier. Following the redirecting collision, the electron must travel from the point of collision to the oxide interface without suffering further collisions that would redirect its momentum or diminish its kinetic energy. If the electron, reaching the oxide interface, has a sufficient kinetic energy to overcome the oxide potential barrier, it is injected into the gate oxide. Since these events are assumed to be statistically independent, the injection probability can be obtained as the product of the probabilities of each event [Hu79].

3.2.1.2. Impact ionisation by hot-electrons

A certain percentage of the electrons moving horizontally along the channel from source to drain create electron-hole pairs by impact ionisation near the drain end of the channel. This impact ionisation process creates an avalanche plasma, consisting of generated electrons and holes, in the pinch-off region. The created holes are collected by the substrate while most of the created electrons are attracted toward the drain junction. Some electrons and holes in the avalanche plasma can gain sufficient energy to surmount the Si-SiO_2 potential barrier and are injected into the gate oxide [Ning79].

It has been shown that avalanche hot-carrier injection due to impact ionisation at the drain, rather than channel hot-electron injection composed of "lucky" electrons, imposes the severest constraints on the reliability of MOSFETs [Take83a]. Therefore, device degradation has a strong correlation with impact ionisation induced substrate current I_{sub}: the gate bias condition which causes the most stringent device degradation, corresponds to that at which the bell-shaped substrate current peaks. This value is usually around $(V_d-1)/2$.

The amount of impact ionisation at the drain end of the channel under given operating conditions can be evaluated by using the lucky-electron concept as in the previous section. To create an electron-hole pair by impact ionisation, the hot electrons travelling along the channel must have a kinetic energy greater than the impact ionisation energy φ_i. The term φ_i/E_m gives the distance that an electron must travel in the electric field E_m to gain the energy φ_i. Thus, the probability of an electron travelling a sufficient distance

to gain the kinetic energy φ_i or more without suffering a collision is:

$$P_i = e^{-\varphi_i / q\lambda E_m} \tag{3-1}$$

where λ is the hot-electron mean-free path in the channel. Since I_d is the rate of total electron flow in the channel, the rate of supply of hot electrons possessing energies greater than φ_i can be expressed as $(I_d.P_i)$. Thus, a general expression for the substrate current is found as:

$$I_{sub} = C_1 I_d e^{-\varphi_i / q\lambda E_m} \tag{3-2}$$

where C_1 is a weak function of the maximum channel electric field E_m.

3.2.2. Oxide degradation due to injected carriers

Once the hot carrier is injected into the SiO_2, several damaging mechanisms can occur.

3.2.2.1. Oxide defects and charge trapping

The physical properties of the silicon-oxide interface and the gate oxide layer and the gradual changes in these properties by operating conditions ultimately determine the long-term hot-carrier reliability of the MOS transistor.

There are four charges associated with the Si-SiO_2 system: the fixed oxide charge, the mobile oxide charge, the oxide trapped charge and the interface trapped charge. The fixed oxide charge is primarily due to structural defects in the oxide layer, located relatively close to the interface. The density of this charge is not influenced by the electrical operating conditions of the MOS transistor. The mobile charge is primarily due to ionic impurities in the oxide. The oxide trapped charge and the interface trapped charge play an important role in the gradual degradation of the oxide characteristics.

The charge distribution and charge density in the gate oxide are altered when the existing traps in the oxide capture excess electrons or holes. The possible oxide defects are impurities and dangling bonds. The impurities in the oxide are mainly hydrogen in the bonded forms, group-III impurities and group-V impurities. The hydrogenated bonds are electrically inactive, they can not trap electrons and holes. The ability of group-III and group-V impurities to trap electrons or holes has not been demonstrated. Thus, mainly the dangling bonds give rise to electron and hole traps. The probability of injected carriers to be captured by an empty trap in the oxide ultimately depends on the available trap density and on the trapping cross-section. Since the lateral electric field in

the channel, which accelerates the electrons, reaches its maximum near the drain end of the channel, a majority of the carriers is injected into the gate oxide within a relatively narrow region in the near vicinity of the drain junction. The oxide charge density, due to trap charging by hot electrons or hot holes, is thus also localised in this region [Lebl93].

Charge trapping can account for some of the observed degradation effects in nMOS transistors, such as the threshold voltage shifts, but attempts to explain other effects (e.g. the transconductance degradation) using charge trapping only have been less successful. It was recognised that not only charge trapping, but also interface trap generation, contribute to the degradation of device characteristics and the influence of each mechanism is determined by the V_g during the stress.

3.2.2.2. Interface trap generation

Interface traps are allowed energy states that are localised in the vicinity of the Si-SiO_2 surface. New interface traps are generated in nMOS transistors by hot electrons as well as hot holes. The most important mechanism for the creation of interface traps involves hot carriers breaking the hydrogen bonds at the interface, releasing the hydrogen atom, and leaving behind dangling Si- or O- bonds [Sah87]. These may easily acquire an electron when the device is in strong inversion, and become negatively charged.

It has to be noticed that there is an important difference between the interface-trapped charge and the oxide charge components discussed in the previous section. Interface traps are in electrical communication with the conduction and valence bands of the underlying silicon, and thus can be charged and discharged, depending on the surface potential. The influence of the interface-trapped charge upon the electrical characteristics of the MOS transistors depends on the bias conditions.

Finally, it must be recognised that the hot-carrier induced interface traps are localised in a narrow region near the drain end of the channel, because the lateral electric field accelerating the electrons and the holes (created by impact ionisation) in the channel attains its maximum near or in the drain region, leading to localised carrier injection into the Si-SiO_2 interface.

3.2.3. Dependence of the oxide degradation on the V_g during stress.

As already described in the introduction, the degradation induced by hot-carrier injection leads to a shift of the threshold voltage V_t, the drain current I_d and the maximum transconductance $g_{m,max}$. This degradation of the transistor performances is

due to charge trapping in the oxide and to interface state creation. The V_t shifts and the relative $g_{m,max}$ and I_d degradation ($\Delta g_{m,max}/g_{m,max}$, $\Delta I_d/I_d$) usually follow a time power law At^n, where t is the stress duration and A is a parameter which depends on V_d and on the technology [Hu85]. The exact nature of the oxide degradation depends on the V_g during stress.

The induced damage is maximum when hot-carrier injections are done at the maximum of I_{sub}, i.e. for $V_g \approx (V_d - 1)/2$. The slope $n \approx 0.5$-0.7 of the power law is due to the creation of the fast interface traps [Vuil98]. Several attempts have been made to explain the microscopic nature and the creation mechanisms of the defects induced by hot-carrier injections. The oldest model, the model of Hu [Hu85], relates this slope to the creation of interface traps by electrons having energies of 3.9 eV and above. A hot electron that breaks a silicon-hydrogen bond has explained the threshold energy and the observed time dependence. The energy needed to overcome the Si-SiO_2 potential barrier is 3.1 eV and the minimum binding energy of the Si-H bond was found to be 0.8 eV. If the resultant trivalent silicon atom recombine with hydrogen, no interface trap is generated. If the hydrogen atom diffuses away from the interface (the diffusion process leads to the $t^{0.5}$ dependence), a new interface trap is generated. Because this model of Hu is one of the most important lifetime prediction models, it will be fully explained in the next section. The second approach to explain the time power law exponent of 0.5 suggests a process in which holes and electrons are both successively involved, via the so-called "two-step process". In this model, the holes are trapped very close to the interface and the subsequent electron trapping on previously trapped holes triggers the generation of interface states [Lai81]. However, this "two-step" model was never clearly validated from hot-carrier experiments in MOSFETs. The conclusion is that a physical model to explain the time power law exponent is not firmly established [Vuil98].

At low V_g, hot electrons and hot holes are injected together in the oxide. The slope $n \approx 0.2$-0.3 of the power law is due to a combination of interface state creation, hole trapping and electron trapping [Here88]. This complicates the interpretation of measurements done at this stress condition and they are not discussed in this work.

At high V_g, only electrons are injected into the oxide. This degradation is also characterised by a time power law At^n where n is typically equal to 0.2-0.3 and the degradation comes from electron trapping on oxide defects which either pre-existed or which are created by the hot electron injection itself [Schw87]. This stress condition will also be no part of this work.

3.3. Hot-carrier degradation measurements on conventional nMOSFETs

A wafer of conventional nMOSFETs of a 2.4 μm technology with L=3.2 μm, W=20 μm and t_{ox}= 42.5 nm was fabricated. The MOSFETs were stressed at worst condition, this is at the maximum of I_{sub}. The left part of Figure 3-1 shows the I_{sub}-V_g curves at the different stress conditions that were used in this experiment and at the normal operating conditions.

3 degradation measurements were performed, one at V_d = 8 V, one at V_d = 7 V and one at V_d = 6 V. The gate voltages have been set such that I_{sub} was maximum. The degradation of $I_{d,lin}$ as a function of stress time is shown in the right part of Figure 3-1.

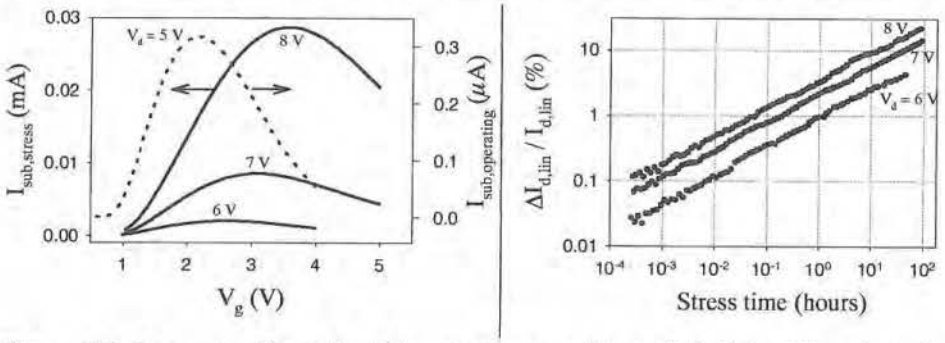

Figure 3-1: I_{sub} versus V_g at the different stress conditions (left; left axis) and at the normal operating conditions (left, right axis); Degradation of $I_{d,lin}$ versus stress time at the different stress conditions (right).

3.4. Degradation models for conventional nMOSFETs

The hot-carrier degradation of conventional nMOSFETs has been studied during several decades. Different papers have been published about the physical degradation mechanisms, the modelling of the degradation curves and the determination of the lifetime at normal operating conditions. The model of Hu and the model of Takeda are well accepted and widely used. They will be discussed now.

3.4.1. Model of Hu

The lifetime of the MOSFET is related to I_{sub}, which is generated by impact ionisation and thus can be written as:

$$I_{sub} = C_1 I_d e^{-\varphi_i / q\lambda E_m} \qquad (3\text{-}3)$$

as already discussed in 3.2.1.2.

In the model of Hu, the worst-case degradation of nMOSFETs is dominated by the generation of interface traps. A possible microscopic mechanism is explained in section 3.2.3: a hot electron breaks a silicon-hydrogen bond. If the resultant trivalent silicon atom recombines with hydrogen, no interface trap is generated. If the hydrogen atom diffuses away from the interface (the diffusion process leads to the t^n dependence), a new interface trap is generated.

The rate of bond breakage may be expressed as $K(I_d/W)e^{-\varphi_{it}/q\lambda E_m}$ where K is proportional to the density of Si-H bonds, W is the channel width so that I_d/W is proportional to the electron density. φ_{it} is the minimum energy (3.7 eV) that an electron must have in order to create an interface trap so that $e^{-\varphi_{it}/q\lambda E_m}$ is the probability of an electron travelling a sufficient distance in the electric field E_m to gain an energy φ_{it} or more.

The rate of recombination between silicon and hydrogen may be expressed as $BN_{it}n_H(0)$ where $n_H(0)$ is the concentration of interstitial hydrogen atoms H_i at the interface. The net rate of interface trap generation is:

$$\frac{dN_{it}}{dt} = K\frac{I_d}{W}e^{-\varphi_{it}/q\lambda E_m} - BN_{it}n_H(0) \qquad (3\text{-}4)$$

Also, the rate of interface trap generation is equal to the rate of H_i diffusing away from the interface, which may be approximated with:

$$\frac{dN_{it}}{dt} = D_H n_H(0)/X_H \qquad (3\text{-}5)$$

Here, D_H and X_H are the effective diffusion constant and an effective length of diffusion of hydrogen. Eliminating the $n_H(0)$ term between (3-4) and (3-5) one obtains:

$$\frac{dN_{it}}{dt}(1+BX_H N_{it}/D_H) = K\frac{I_d}{W}e^{-\varphi_{it}/q\lambda E_m} \qquad (3\text{-}6)$$

Multiplying both sides by dt and integrating once:

$$\frac{BX_H}{2D_H}N_{it}^2 + N_{it} = K\,t\frac{I_d}{W}e^{-\varphi_{it}/q\lambda E_m} \qquad (3\text{-}7)$$

At small N_{it}, $N_{it} \sim t$ (assuming negligible initial trap density). At large N_{it}, $N_{it} \sim t^{1/2}$. In general:

$$N_{it} = C_2 \left(t \frac{I_d}{W} e^{-\varphi_{it}/q\lambda E_m} \right)^n \tag{3-8}$$

with n in the range between 0.5 and 1.

In [Take83a], it has been shown that the following relationship is well satisfied:

$$\Delta P / P_0 \propto N_{it} \tag{3-9}$$

were P can be $g_{m,max}$ or $I_{d,lin}$. By inserting (3-3) into (3-8), the percentage degradation of $I_{d,lin}$ can be written as:

$$\frac{\Delta I_{d,lin}}{I_{d,lin0}} = C_3 \left[t \frac{I_d}{W} \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right]^n \tag{3-10}$$

This equation will be used to model the degradation of $I_{d,lin}$ as a function of stress time as shown in the right part of Figure 3-1.

When defining the lifetime of the device as the time when $\Delta I_{d,lin}/I_{d,lin0}$ reaches a chosen value (failure criterion FC), (3-10) can be written as:

$$\tau \frac{I_d}{W} = \left(\frac{FC}{C_3} \right)^{1/n} \left(\frac{I_{sub}}{I_d} \right)^{-\varphi_{it}/\varphi_i} \tag{3-11}$$

or:

$$\log\left(\tau \frac{I_d}{W} \right) = \frac{1}{n} \log\left(\frac{FC}{C_3} \right) - \frac{\varphi_{it}}{\varphi_i} \log\left(\frac{I_{sub}}{I_d} \right) \tag{3-12}$$

which is the well-known lifetime model of Hu.

3.4.2. Model of Takeda

In [Take83b], an empirical model for device degradation due to hot-carrier injection in nMOSFETs is presented. It was found that the V_t shift, ΔV_t or the $g_{m,max}$ degradation, $\Delta g_{m,max}/g_{m,max}$ can be experimentally expressed as:

$$\Delta V_t \,(\text{or} \Delta g_{m,max}/g_{m,max}) = A\, e^{-\alpha/V_d} t^n \tag{3-13}$$

This equation has the same shape as (3-10) and can be used to model the degradation behaviour of the characteristic parameter as a function of stress time.

From (3-13), the lifetime of the MOSFET under a certain FC can be expressed as:

$$\tau = \left(\frac{FC}{A}\right)^{1/n} e^{B/V_d} \tag{3-14}$$

or:

$$\ln\tau = \frac{1}{n}\ln\frac{FC}{A} + \frac{B}{V_d} \tag{3-15}$$

where FC is the chosen failure criterion and $B = \alpha/n$. Thus:

$$\ln\tau \propto \frac{1}{V_d} \tag{3-16}$$

and this is the lifetime model of Takeda.

Although in the original publication [Take83b] the model of Takeda is described as an empirical model, it can be easy calculated from the model of Hu, described in the previous section. Replacing I_{sub} in (3-11) by (3-3) one obtains:

$$\tau\frac{I_d}{W} = C_4\left(C_1 e^{\varphi_{it}/q\lambda E_m}\right) \tag{3-17}$$

Since:

$$E_m \approx \frac{V_d - V_{d,sat}}{l} \tag{3-18}$$

were $V_{d,sat} \approx V_g - V_t$ and l is the effective length of the velocity saturation region, equation (3-17) can be written as:

$$\tau = C_1 C_4 \frac{W}{I_d} e^{\varphi_{it} l / q\lambda\left(V_d - V_{d,sat}\right)} \tag{3-19}$$

and thus:

$$\ln\tau = \ln\left(C_1 C_4\right) + \frac{\varphi_{it}.l}{q\lambda\left(V_d - V_{d,sat}\right)} - \ln\left(\frac{I_d}{W}\right) \tag{3-20}$$

From this equation, the lifetime model of Takeda can be calculated if 2 assumptions can be made:

- $V_{d,sat} << V_d$ and can thus be neglected
- $\ln(I_d) \sim 1/(V_d - V_{d,sat})$ or $\ln(I_d) \sim 1/V_d$ if the first assumption is acceptable

Figure 3-2 shows that the last assumption can be made in the interval we are measuring. The dots in the left part of Figure 3-2 represent the natural logarithm of I_d versus $1/(V_d-V_{d,sat})$ for 4 different V_d's: 5, 6, 7 and 8 V. The full line represents the least-square linear fit of the measurement points. The right part of Figure 3-2 shows the same result for $\ln(I_d)$ versus $1/V_d$. In both cases, a straight line is obtained.

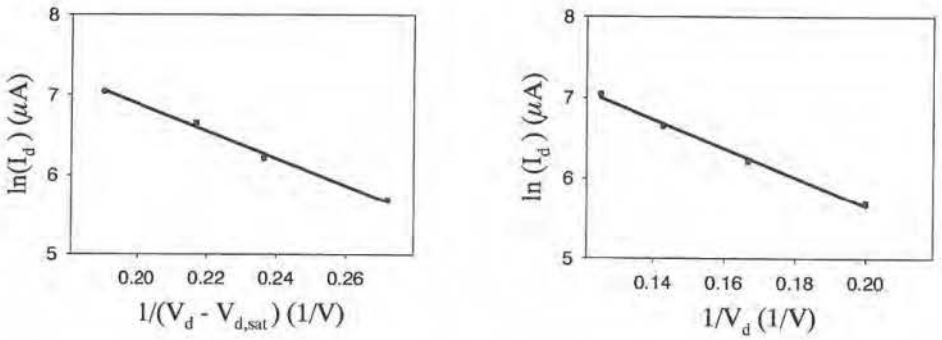

Figure 3-2: $ln(I_d)$ versus $1/(V_d-V_{d,sat})$ at four different V_d's: 5,6,7 and 8 V (left); $ln(I_d)$ versus $1/V_d$ at four different V_d's: 5,6,7 and 8 V (right).

With these 2 assumptions, equation (3-20) can be written as:

$$\ln \tau = \ln A + \frac{\alpha}{V_d} \tag{3-21}$$

with A and α two constants. This equation represents the lifetime model of Takeda.

Suppose now that the first assumption is not made, instead of equation (3-21), a refined model of Takeda is obtained:

$$\ln \tau = \ln A + \frac{\alpha}{V_d - V_{d,sat}} \tag{3-22}$$

Notice that in comparison with (3-16), the parameter $V_{d,sat}$ is an extra factor in the lifetime equation. Both equations will be used in the next section to calculate the lifetime of nMOSFETs under normal operating conditions.

3.5. Application of the models to the degradation measurements

3.5.1. Introduction

The right part of Figure 3-1 indicates that the degradation behaviour of the conventional MOSFETs follows a straight line on a logarithmic scale. Fitting the model of Hu or Takeda on these degradation curves has, in this work, been done using the method of LSE. This method minimises the root-mean-square of the errors [Nete90]. Such an error is defined as the vertical distance between the measurement point and the fit. The following number is thus minimised:

$$\sqrt{\frac{1}{n}\sum_{i=1}^{n}\left(y_i-\overline{y_i}\right)^2} \qquad (3\text{-}23)$$

where n is the number of measurement points, y_i is the measured value and $\overline{y_i}$ is the fitted value. The method of LSE will now be applied to fit the degradation behaviour of the conventional MOSFETs with the models of Hu and Takeda.

3.5.2. Lifetime determination with the model of Hu

The model of Hu is mostly used to describe the degradation behaviour and to extrapolate the lifetime of nMOSFETs at normal operating conditions. From equation (3-10), it is known that, for each stress condition:

$$\frac{\Delta I_{d,lin}}{I_{d,lin0}} = C\,t^{n} \qquad (3\text{-}24)$$

with C a constant depending on the technology and on the chosen stress condition. In the left part of Figure 3-3, each degradation curve is fitted separately with equation (3-24). The results of these fits are summarised in table 3-1. As can be observed, n remains constant and C(*) depends highly on the chosen stress conditions.

Finally, equation (3-12) can be used for extrapolating the lifetime at the normal operating conditions, which is V_d=5V. In the right part of Figure 3-3, log ($\tau.I_d/W$) is plotted versus log (I_{sub}/I_d) for three different failure criteria: 0.1 %, 1 % and 10 %. The slope of this curve represents $-\varphi_{it}/\varphi_i$. According to Hu et al. [Hu85], φ_{it} is slightly larger

(*) The unit of C is $\%/s^n$, n has no unit.

V_d (V)	C	n
6	0.912	0.445
7	2.070	0.424
8	3.368	0.425

Table 3-1: Result of the fit of the degradation curves of Figure 3-3 with (3-24)

than the Si-SiO_2 energy barrier (3.2 eV), but the minimum value ever reported is 2 eV [DiMa89]. The value of φ_i is reported to be around 1.6 eV (1.5 times the Si bandgap) [Groe99]. Thus the theoretical value of $-\varphi_{it}/\varphi_i$ can vary from –1.25 down to –3. For the failure criterion of 10 %, the slope is –1.392. Because only three stress conditions have been measured, the error on this slope will be very large. By using standard linear regression procedures [Nete90], it has been found that the 95% confidence interval equals [-3.176,0.392]. Thus, there is an agreement between the confidence interval of the experimental slope and the expected theoretical slope. A similar result is found for the other failure criteria.

The estimated lifetimes are given in the second column of Table 3-2 given at the end of section 3.5.4. The non-optimised technology results in a very low lifetime at normal operating conditions. A similar linear regression procedure can be used to determine the 95% confidence interval on the predicted lifetime. For example for a failure criterion of 10 %, the predicted lifetime is 62.93 days but the confidence interval equals [14.42 days,274.60 days]. A similar result is found for the other failure criteria.

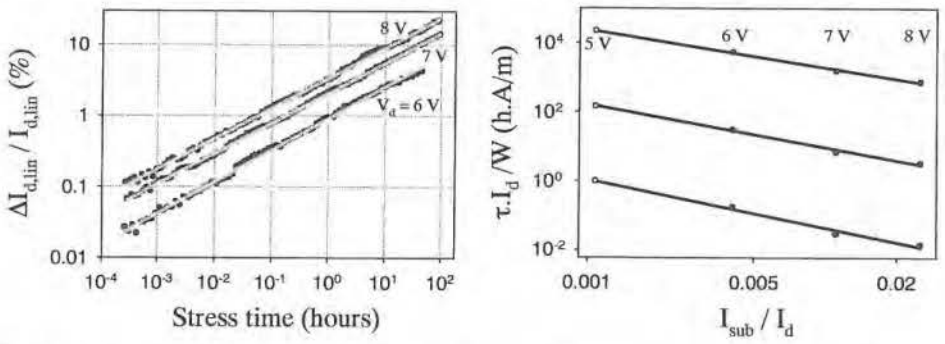

Figure 3-3: Measured percentage degradation of $I_{d,lin}$ as a function of stress time (left, dots); Least-square linear fit with the model of Hu (left, lines); Lifetime extrapolation method of Hu: plot of I_{sub}/I_d as a function of $\tau.I_d/W$ at three different FC: 0.1 % (lower line), 1 % (middle line) and 10 % (upper line) (right).

3.5.3. Lifetime determination with the model of Takeda

The model of Takeda is also widely used to determine the lifetime of conventional MOSFETs at normal operating conditions.

To determine the lifetime, at a given FC, for the different stress conditions, the same procedure as in the previous section is used: fit each degradation curve separately with equation (3-24) and with the aid of the fit coefficients C and n the lifetime can be calculated. This is allowed since the time dependence of equation (3-24) is the same as the time dependence of equation (3-13). Finally, equation (3-15) can be used for extrapolating the lifetime at the operating conditions. The left part of Figure 3-4 shows ln τ versus $1/V_d$ for different failure criteria: 0.1 %, 1 % and 10 %. According to equation (3-15), these points should lay on a straight line. The third column of Table 3-2 summarises the estimated lifetimes. The confidence bounds are similar than those found in the previous section with the model of Hu.

It was shown in section 3.4.2 that equation (3-15) is only correct when $V_{d,sat}$ can be neglected in comparison with V_d. This model is commonly used but a more correct model is given by equation (3-22). The right part of Figure 3-4 shows the result of the lifetime extrapolation with this equation. The estimated lifetimes can be found in the fourth column of Table 3-2. Again, the confidence bounds are similar than those found in the previous section with the model of Hu.

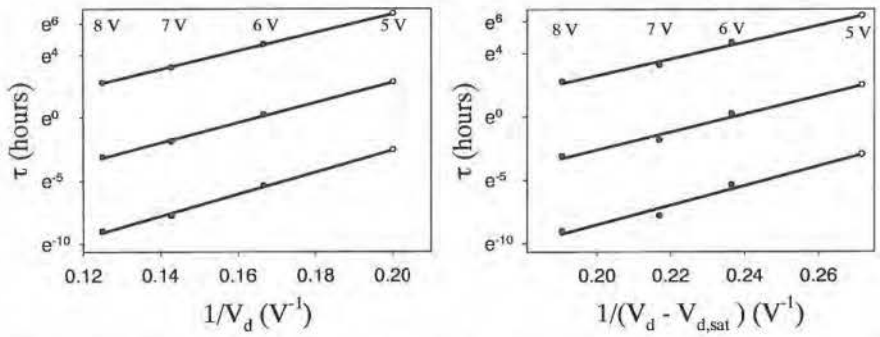

Figure 3-4: Lifetime extrapolation method of Takeda: plot of the lifetime as a function of $1/V_d$ for 3 different FC: 0.1% (lower line), 1% (middle line) and 10% (upper line) (left); Refined lifetime extrapolation method of Takeda: plot of the lifetime as a function of $1/(V_d - V_{d,sat})$ for 3 different FC: 0.1% (lower line), 1% (middle line) and 10% (upper line) (right).

3.5.4. New lifetime prediction procedure

Instead of fitting each degradation curve separately and using a lifetime plot to predict the lifetime at normal operating conditions, it is now proposed to perform a simultaneous least-square linear fit on all the degradation curves. For the model of Hu, the result of this fit is shown in Figure 3-5. The dots represent the measured percentage degradation of $I_{d,lin}$ as a function of stress time. The full lines give the result of the simultaneous least-square linear fit with equation (3-10).The estimated fit coefficients are C_3=4.653(*), n=0.431 and φ_{it}/φ_i=1.265. The determination of the confidence bounds on these coefficients, from the simultaneous fit, is complicated because the different points on a degradation curve are not statistically independent. Some methods can be found in Lu et al. [Lu93 and Lu97] but this is beyond the scope of this work.

The lifetimes estimated using this new procedure are summarised in the fifth column of Table 3-2. For the same reason as stated above, the determination of the confidence bounds on these predicted lifetimes is complicated and beyond the scope of this work.

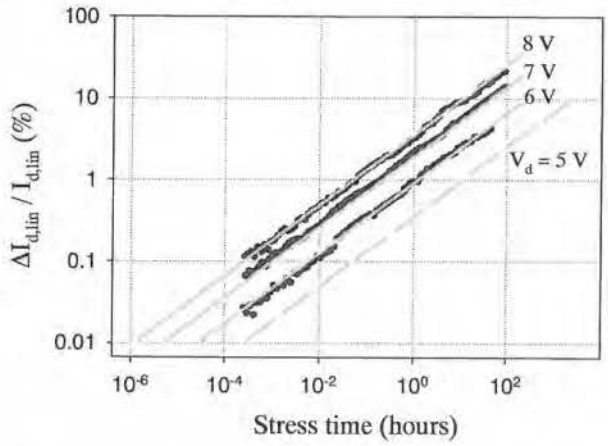

Figure 3-5: Measured percentage degradation of $I_{d,lin}$ as a function of stress time (dots);. Simultaneous least-square linear fit with Hu (lines) and prediction of the degradation behaviour at normal operating conditions (dotted line).

The same procedure can be used to predict the lifetime of the conventional MOSFET technology with the model of Takeda. Purely based on visual inspection, the result of the simultaneous least-square linear fit of the degradation measurements with equation (3-13), with $I_{d,lin}$ as degradation parameter instead of V_t, looks the same as in

(*)The unit of C_3 is $\%/(s.A/m)^n$, n has no unit

Figure 3-5. The estimated fit coefficients are now: A= 206.091(*), α= 32.546 V and n=0.431. The estimated lifetimes are summarised in the sixth column of Table 3-2.

As already discussed before, it is better to predict the lifetime with the refined model of Takeda given by equation (3-22). The simultaneous least-square fit is now performed with the following equation:

$$\frac{\Delta I_{d,lin}}{I_{d,lin}} = A e^{-\alpha/\left(V_d - V_{d,sat}\right)_t{}^n} \tag{3-25}$$

The estimated fit coefficients are now: A= 979.000, α= 29.520 V and n= 0.431. The estimated lifetimes are summarised in the last column of Table 3-2.

As a conclusion, without given any proof, the simultaneous least-square linear fit with the model of Hu is proposed as the best method for predicting the lifetime of a conventional MOSFET technology at operating conditions when high-resolution measurements are performed. The model of Hu is proposed because it is physically well-founded and the simultaneous least-square fit is proposed as the best fitting procedure. It is believed that the advantage of this simultaneous fitting procedure is that, using appropriate statistical theory, the confidence bounds on the estimated lifetimes will be much lower than those obtained by the procedure used in 3.5.2 and 3.5.3. This is due to the fact that all measurement points are used "at once" for obtaining such confidence bounds. As a suggestion for further work, it is recommended to calculate these confidence bounds. This however requires an advanced statistical background.

In practice, the model of Takeda is often used. In this work, it is proposed to use the refined model of Takeda given by equation (3-25).

FC (%)	Hu 1	Takeda 1a	Takeda 1b	Hu 2	Takeda 2a	Takeda 2b
0.1	2.75e-3 d	3.95e-3 d	2.64e-3 d	2.18e-3 d	3.08e-3 d	1.96e-3 d
1	0.41 d	0.57 d	0.41 d	0.46 d	0.65 d	0.41 d
10	62.93 d	85.85 d	64.16 d	95.11 d	135.14 d	85.80 d

Table 3-2: Estimated lifetimes (V_{dd}=5 V) in days at three different FC with different degradation models and fitting methods: 1: separate fit of each degradation curve, 2: simultaneous fit, a: original model of Takeda and b: refined model of Takeda.

(*)The unit of A is $\%/s^n$, n has no unit.

3.6. Advantages of the HRMT

In this section, the main advantages of the HRMT will be discussed. Section 3.6.1 discusses the advantages of the HRMT with respect to the physical degradation mechanisms in the initial degradation area. In section 3.6.2, Monte Carlo simulations are performed for finding out whether the lifetime prediction is more accurate with the HRMT. Finally, in section 3.6.3, the possibility of test time reduction with the HRMT will be discussed.

3.6.1. Physical degradation mechanisms

Before the HRMT was developed, several questions concerning the physical degradation mechanisms of MOSFETs could not be answered:

- What are the degradation mechanisms in the initial degradation phase ?
- How is the behaviour of the initial degradation as a function of time ?
- Are new failure mechanisms introduced when high stress levels are applied ?

A typical degradation measurement performed with the HRMT is shown in the right part of Figure 3-1. It can be observed that from 0.01 % up to more than 10 %, the degradation behaviour of conventional nMOSFETs can be described by a straight line on a logarithmic scale. This means that only one degradation mechanism is active in the full degradation area, namely the creation of traps in the Si-SiO_2 interface. The complete degradation behaviour can be described by the model of Hu and the model of Takeda. The degradation behaviour at V_d=8 V is not different from the behaviour at V_d=6 V, therefore it can be concluded that no new failure mechanisms are introduced when high stress levels are applied.

3.6.2. Lifetime prediction

In order to compare the classical, low resolution, degradation measurement techniques with the high-resolution technique with respect to the accuracy on the lifetime prediction, a large number of degradation curves have been simulated using Monte Carlo simulations [Kalo86]. For these simulations, it is assumed that the degradation follows the model of Hu given in equation (3-10). The model parameters C_3, n and φ_{it}/φ_i were set to their values estimated in section 3.5.4. The stress conditions for V_d were, like in the experiment, chosen to be 6, 7 and 8 V. For each simulated experiment, the

degradation curves were fitted with a simultaneous least-square linear fit using the assumed model of Hu and the lifetime was estimated for V_d = 5 V.

Two different measurement resolutions were assumed: 0.5% (classical techniques) and 0.02% (high-resolution technique). The simulated measurements were stopped when the highest stress condition reached the 10 % degradation level. At V_d = 8V, this degradation level is reached after approximately 10 hours of stress.

3.6.2.1. Only measurement noise

In a first, simplified case, all the measured samples are supposed to be identical and equal to the "theoretical" sample. The only deviations between the "theoretical" and the measured degradation curve are caused by measurement noise. In order to simulate this measurement noise, a normal distributed noise with a standard deviation of the measurement resolution divided by 6 was added to the theoretical curve. By doing this, it is guaranteed that 99% of the simulated degradation points fall within the theoretical value plus or minus the measurement resolution. The normal distribution is chosen because it is the most representative for the real measurements.

Figure 3-6 shows an example of one simulated experiment. The left part shows an experiment simulated with a measurement resolution of 0.02 %, the right part shows the same for a measurement resolution of 0.5 %. The results of the simultaneous least-square linear fits are shown by the full lines on the figures.

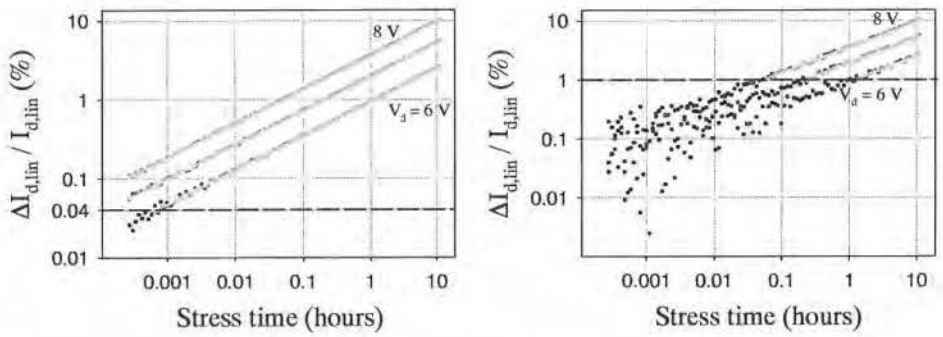

Figure 3-6: Simulated degradation of $I_{d,lin}$ as a function of stress time, measurement resolution=0.02% (left, dots); Simultaneous least-square linear fit with the model of Hu (left, lines); Simulated degradation of $I_{d,lin}$ as a function of stress time, measurement resolution=0.5% (right, dots); Simultaneous least-square linear fit with the model of Hu (right, lines).

Since the measurement noise is assumed to be symmetric on a linear scale of $\Delta I_{d,lin} / I_{d,lin}$, this noise becomes asymmetric on a logarithmic scale. When using least-square fitting, this is dangerous because it leads to biased estimates. That's why it is decided not to use the measurement points lower than twice the measurement resolution, because these points are most susceptible to the introduced asymmetry.

4000 datasets, like those shown in Figure 3-6, were performed and the lifetime for a FC of 10 % was estimated. The result of the simulations is shown in Figure 3-7 on a density plot(*). From section 3.5.4, it is known that the "theoretical lifetime" is 95.11 days and it is represented by the full line. The median of the 4000 predicted lifetimes is represented by the dashed line. For the measurement resolution of 0.5 %, the median is 98.37 days and for the measurement resolution of 0.02 %, the median is 95.10 days. In order to compare the intervals of the predicted lifetimes, it is advisable that the medians more or less coincide. The deviation of the median lifetime from the theoretical, in case of a low measurement resolution, can be explained by the fact that the LSE supposes a symmetric noise and on the logarithmic scale, this is not the case. Therefore, we will switch to maximum likelihood fitting, which accounts for the correct distribution of the noise.

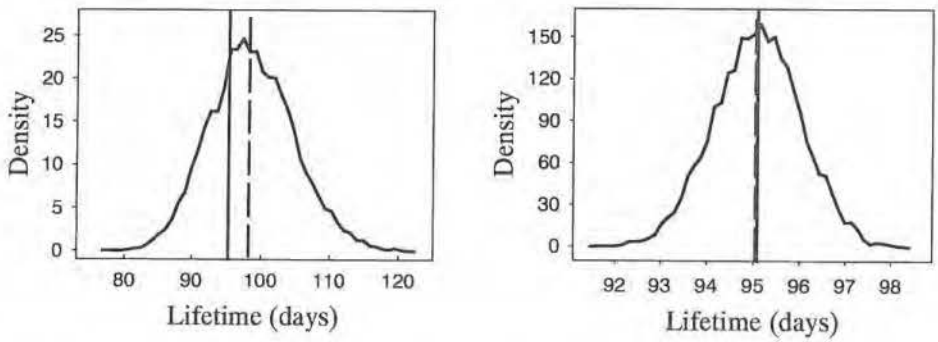

Figure 3-7: Density plot of the predicted lifetimes after LSE for a measurement resolution of 0.5 % (left); Density plot of the predicted lifetimes after LSE for a measurement resolution of 0.02 % (right).

Although the medians of the two measurement resolutions do not coincide, the standard deviation gives us some information of the accuracy on the lifetime prediction. For the measurement resolution of 0.5 %, the standard deviation is 6.16 days and for the measurement resolution of 0.02 %, the standard deviation is 0.94 days. The accuracy on

(*)On a density plot, the quantity density $(\tau)\delta\tau$ is, for a small $\delta\tau$, the unconditional probability for a lifetime in $[\tau,\tau+\delta\tau]$.

the lifetime prediction can thus be improved by more than a factor 6 by using the HRMT.

Maximum likelihood fitting

Switching from LSE to maximum likelihood estimation (MLE) should solve the deviation of the median from the theoretical value in case of a low measurement resolution because it takes into account the correct distribution of the measurement noise. This noise is normal distributed on a linear scale, thus the density function is given by:

$$f_{noise}(\Delta) = \frac{1}{\sqrt{2\Pi}\sigma} e^{-\frac{1}{2}\left(\frac{\mu-\Delta}{\sigma}\right)^2} \tag{3-26}$$

where $f_{noise}(\Delta)d\Delta$ describes the probability for a certain Δ to be in the small interval $d\Delta$, given the "theoretical" drift μ and a resolution of $6*\sigma$. The drift μ depends on the time and on the coefficients C_3, n and φ_{it} / φ_i. On a logarithmic scale, it can be calculated that the distribution of the noise is given by:

$$f_Y(y) = \frac{10^y}{\sqrt{2\Pi}\sigma} e^{-\frac{1}{2}\left(\frac{\mu-10^y}{\sigma}\right)^2} \ln 10 \tag{3-27}$$

where $Y=\log_{10}(\text{noise})$ and $y=\log_{10}(\Delta)$. The likelihood function L is defined as:

$$L = \prod_{i=1}^{N} f_Y(y_i;\mu_i,\sigma) \tag{3-28}$$

It gives a measure for the total probability or the likelihood of the experiment. N is the total number of measurement points in the experiment. The product goes thus over all measurement points i.

The ML-method searches for those values of the parameters C_3, n and φ_{it} / φ_i that maximise the probability of the experiment and thus L. These maximums are defined as the MLE's of C_3, n and φ_{it} / φ_i.

The density plots for the two measurement resolutions, obtained by fitting the simulated datasets with MLE, are shown in Figure 3-8. The theoretical lifetime remains unchanged and is represented by the full line. The median of the 4000 predicted lifetimes is represented by the dotted line. For the measurement resolution of 0.5 %, the

median is 95.79 days and for the measurement resolution of 0.02 %, the median is 95.11 days. The medians of the predicted lifetimes for both measurement resolutions nearly coincide and thus the prediction intervals can be compared. For the measurement resolution of 0.5 %, the standard deviation is 4.18 days and for the measurement resolution of 0.02 %, the standard deviation is 0.13 days. The accuracy on the lifetime prediction can thus be improved by more than a factor 32 by using the HRMT.

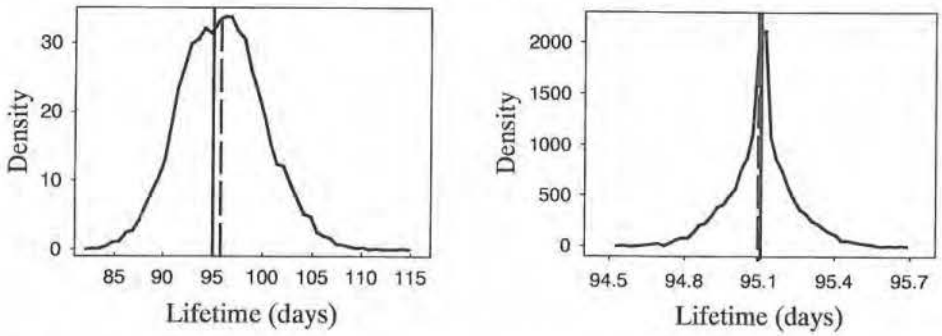

Figure 3-8: Density plot of the predicted lifetimes after MLE for a measurement resolution of 0.5 % (left); Density plot of the predicted lifetimes after MLE for a measurement resolution of 0.02 % (right).

3.6.2.2. Measurement noise and realistic samples

The simulations performed in the previous section are not realistic. The measurement noise is not the only factor which influences the lifetime prediction. In any manufacturing process, transistor parameters will vary from lot to lot, wafer to wafer, IC to IC and transistor to transistor within IC's due to physical defects and normal process variations. In Snyder et al. [Snyd92], the variation in device "lifetime" is studied. Large samples of identically designed transistors were stressed at the same condition and $I_{d,lin}$ was measured as a function of stress time. It is shown that the lognormal distribution adequately describes the variation in accelerated lifetimes. The dispersion parameter, σ_S was found to independent of the stress voltage and around 0.04.

The same simulations as in the previous section will now be performed, except that the variation in accelerated lifetimes is now incorporated. The lognormal distribution, which adequately describes this variation, is incorporated as a shift of the x-scale of each individual degradation curve.

Figure 3-9 shows an example of one simulated experiment. The left part shows an experiment simulated with a measurement resolution of 0.02 %, the right part shows the

same for a measurement resolution of 0.5 %. The results of the simultaneous least-square linear fit is shown by the full line. In this figure, only a zoom-in between 1 and 2 % of degradation is shown.

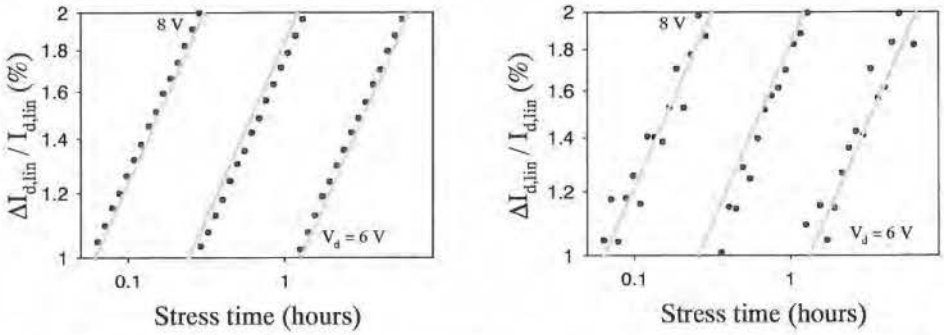

Figure 3-9: Simulated degradation of $I_{d,lin}$ as a function of stress time, measurement resolution=0.02% (left, dots); Simultaneous least-square linear fit with the model of Hu (left, lines); Simulated degradation of $I_{d,lin}$ as a function of stress time, measurement resolution=0.5% (right, dots); Simultaneous least square linear fit with the model of Hu (right, lines).

It is clear form the simulation with a low measurement resolution that, due to σ_S, the fit and the simulated degradation curves do not coincide perfectly. On the right part of the figure, the deviation is not so clear because of the low measurement resolution. Like in the previous section, it is again decided not to use the measurement points lower than twice the measurement resolution, because these points are most susceptible to the introduced asymmetry introduced by fitting on a logarithmic scale.

Again, 4000 datasets, like those shown in Figure 3-9 were performed, the datasets were fitted with LSE and the lifetime was estimated. Density plots of these simulations are depicted in Figure 3-10. The theoretical lifetime is 95.11 days and is represented by the full line. The median of the 4000 predicted lifetimes is represented by the dotted line. For the measurement resolution of 0.5 %, the median is 99.54 days and for the measurement resolution of 0.02 %, the median is 95.65 days. Again, the medians of the two measurement resolutions do not coincide, but the standard deviation gives us some information of the accuracy on the lifetime prediction. For the measurement resolution of 0.5 %, the standard deviation is 19.15 days and for the measurement resolution of 0.02 %, the standard deviation is 16.44 days. When taking into account σ_S, the accuracy on the lifetime prediction can not be significantly improved by using the HRMT.

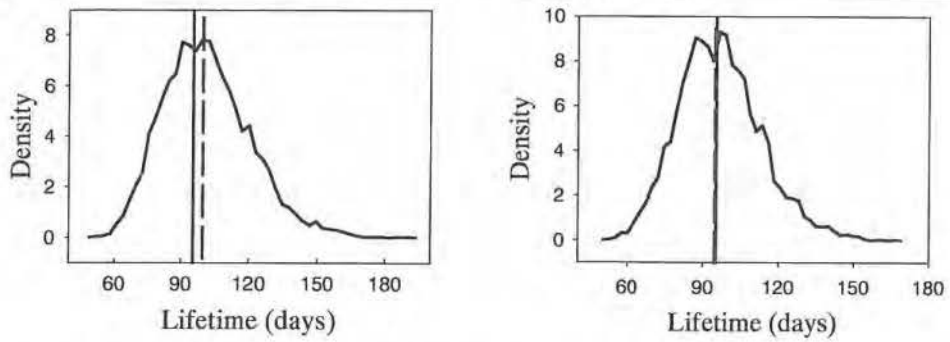

Figure 3-10: Density plot of the predicted lifetimes after LSE for a measurement resolution of 0.5 % (left); Density plot of the predicted lifetimes after LSE for a measurement resolution of 0.02 % (right).

In Figure 3-11, the same datasets were fitted with MLE. The result is a tailed distribution. The theoretical lifetime remains unchanged and is again represented by the full line. The median of the 4000 predicted lifetimes is represented by the dotted line. For the measurement resolution of 0.5 %, the median is 97.15 days and the standard deviation is 26.34 days. For the measurement resolution of 0.02 %, the median is 95.84 days and the standard deviation is 24.06 days. The conclusion stays the same as with the LSE fit: the accuracy on the lifetime prediction can not be improved significantly by using the HRMT.

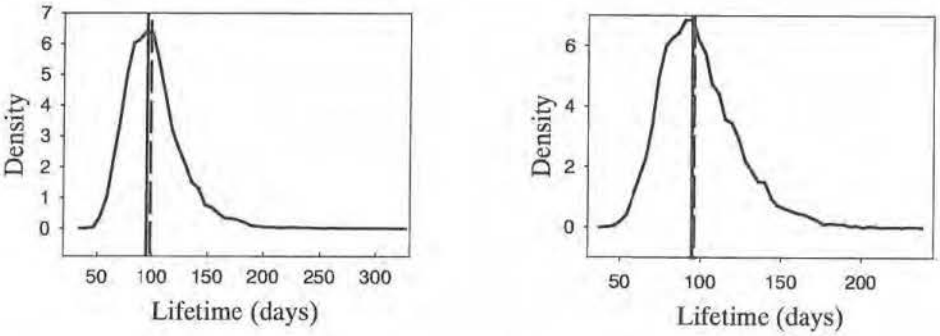

Figure 3-11: Density plot of the predicted lifetimes after MLE for a measurement resolution of 0.5 % (left); Density plot of the predicted lifetimes after MLE for a measurement resolution of 0.02 % (right).

3.6.2.3. Conclusion

A summary of the simulations performed in this section is given in Table 3-3:

- when a model exists to take into account σ_S (it looks as if it is 0 in the simulations), the ideal measurement-fit method is: high-resolution measurements and fit with MLE. This results in the lowest standard deviation as shown in the fifth row of the table. With this method, it can be concluded from the simulations that the accuracy on the lifetime predictions can be improved by a factor 30 by using the HRMT
- when no model exist to take into account σ_S, the ideal measurement-fit method is: high-resolution measurements and fit with LSE:
    1. when low-resolution measurements are performed, the median lifetime deviates from the theoretical and the standard deviation is higher as shown in the sixth and eight row of the table
    2. when MLE is used, a tailed distribution occurs with a very high standard deviation as shown in the last row of the table

  However, in this case, the accuracy on the lifetime prediction can not be improved by using the HRMT.

Fit method	Measurement Resolution	σ_S	Median (days) "theoretical"=95.11 days	Standard Deviation (days)
LSE	0.5	0	98.37	6.16
LSE	0.02	0	95.10	0.94
MLE	0.5	0	95.79	4.18
MLE	0.02	0	95.11	0.13
LSE	0.5	0.04	99.54	19.15
LSE	0.02	0.04	95.65	16.44
MLE	0.5	0.04	97.15	26.34
MLE	0.02	0.04	95.84	24.06

Table 3-3: Comparison of the median lifetime and the standard deviation for the different fit methods, the different measurement resolutions and for the different values σ_S.

In this work, no model is available to account for σ_S. Therefore, from now on, only least-square fits will be used. For the high measurement resolution, this is justified by comparing the right part of Figure 3-11 with the right part of Figure 3-10. For the low measurement resolution, the deviation of the median of the predicted lifetimes from the theoretical in case of the LSE is a much lower effect than the increase of the standard deviation from LSE to MLE.

3.6.3. Test time reduction

When it can be assumed that the model of Hu is correct, the high-resolution measurements can be stopped earlier than the classical measurements and thus the test times can be reduced. When testing conventional MOSFETs, such as power MOSFETs, this is an important advantage of the HRMT.

Again, simulations have been performed in order to prove that the accuracy on the lifetime prediction is the same when measurements are done with a classical measurement technique and long test times or measurements done with the HRMT and short test times. The simulated measurements with a measurement resolution of 0.5% are shown in the previous section. The density plot is shown in the left part of Figure 3-10, the median of the predicted lifetimes was 99.54 days and the standard deviation was equal to 19.145 days.

The same simulations will now be done with the HRMT, but instead of stopping the measurements when the highest stress condition reaches the 10 % degradation level, the measurement will now be stopped when the 1 % degradation level is reached. In the previous section, the total test time was around 11 hours, now this test time is reduced to approximately 3 minutes with the HRMT which results in a test time reduction of a factor 200. Figure 3-12 shows an example of one simulated dataset with a total test time of 3 minutes. The right part of the figure shows the density plot of the 4000 simulated datasets.

The theoretical lifetime is again is 95.11 days, the median of the predicted lifetimes is 97.92 days and the standard deviation is 18.06 days. This standard deviation is comparable to the standard deviation of the simulations with a measurement resolution of 0.5 % and long test times as they were performed in the previous section.

In conclusion, it can be stated that the total test time can be drastically reduced by using the HRMT which is due to the fact that the measurements can be stopped earlier.

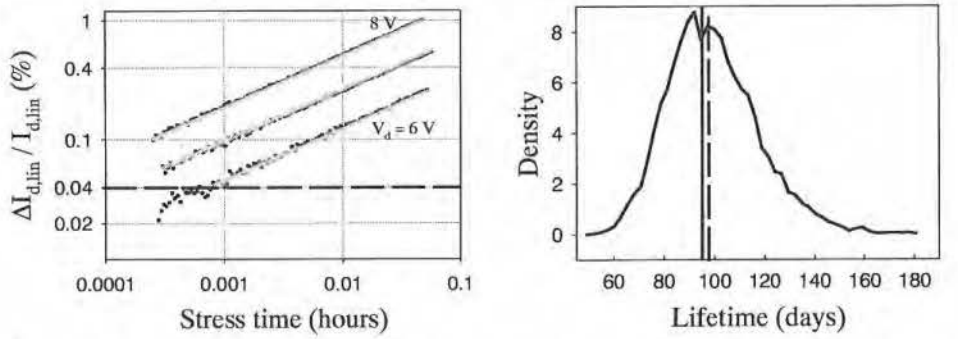

Figure 3-12: Simulated degradation of $I_{d,lin}$ as a function of stress time, measurement resolution=0.02% (left, dots); Simultaneous least-square linear fit with the model of Hu (left, lines); Density plot of the predicted lifetimes after LSE for a measurement resolution of 0.02 % (right).

3.7. Conclusions

In this chapter, the hot-carrier degradation of conventional nMOSFETs is studied. The degradation mechanisms, as they are described in the literature, were discussed and measurements on a 2.4 μm technology were performed. The models of Hu and Takeda were discussed and the model of Takeda has been extracted from the model of Hu by using two approximations. The model of Hu and Takeda have been fitted on the degradation measurements by using the least-square estimation. It has been shown that a more correct lifetime model of Takeda is obtained when $V_{d,sat}$ is not neglected in comparison to V_d (first approximation). Instead of fitting each degradation curve separately and using a lifetime plot to predict the lifetime at normal operating conditions, it is proposed to perform a simultaneous least-square linear fit on all the degradation curves. The chapter ends with an investigation of the advantages of the HRMT on three different subjects: physical degradation mechanisms, lifetime prediction and test time reduction. It is concluded that only one degradation mechanism is active in the full degradation area, that the lifetime prediction can not be significantly improved by using the HRMT and that the test times can be seriously reduced because the measurements can be stopped earlier.

4. The Hot-Carrier Degradation of Lightly Doped Drain nMOSFETs.

4.1. Introduction

Since hot-carrier degradation was recognised as an obstacle for device scaling, many attempts have been made for reducing its impact and for making devices more resistant to it. Most of this work has focussed on tailoring source/drain junctions by modifying the ion implantation and annealing steps. This field has been termed "drain engineering".

The key to hot-carrier optimisation using drain engineering is the reduction of the electric field peak. As already discussed in chapter 1, in conventional MOSFETs, arsenic is implanted in the source and drain regions. Figure 4-1 (a) shows the device structure and the doping profile. Arsenic is a slowly diffusing dopant, yielding shallow junctions with low resistivity. The doping gradient between drain and substrate is very high. The depletion region between drain and substrate does not extend into the drain and the drain potential is unchanged almost up to the metallurgical p-n junction. When the MOSFET is in saturation, the separation between this junction and the pinch-off point is the critical distance over which most of the potential drop occurs. This is the worst possible situation for hot-carrier generation [Moss93].

If the doping concentration in the drain is somewhat reduced, the depletion layer spreads into the drain region and the distance over which the potential drops is lengthened, leading to lower electric fields. By scaling down the dimensions of the MOSFET, more complicated drain/source structures are necessary. In Miko et al. [Miko86], it is shown that when the supply voltage is 5 V, the conventional arsenic drain can be used until the channel length is shrinked down to 2 μm. When the channel length is further reduced, the arsenic is replaced by phosphorus. Phosphorus has a higher diffusion coefficient than arsenic. The doping profile has a much more gradual slope, making the junction less abrupt. The device structure and doping profile are shown in Figure 4-1 (b). The disadvantage of the phosphorus drain structure is that the resistivity increases. Once the channel length is decreased below 1.7μm, the phosphorus drain is replaced by the double diffused drain (DDD) (Figure 4-1 (c)). Here, both As and P are implanted. A high-dose As-implantation assures low resistivity while the low-dose P-implantation reduces the field peak [Moss93]. This structure has been found to be

effective in technologies with gate lengths of 1.2 μm and longer. At shorter gate lengths, the difference between the diffusion fronts of P and As is insufficient. In this case, the DDD-structure is replaced by a lightly doped drain (LDD) (Figure 4-1 (d)). Here, additional field lowering is provided by offsetting the As-implantation (n^+ region) laterally against the P-implantation (n^- region). This can be done using a spacer as implantation mask. The n^- region acts as a resistance in series with the channel.

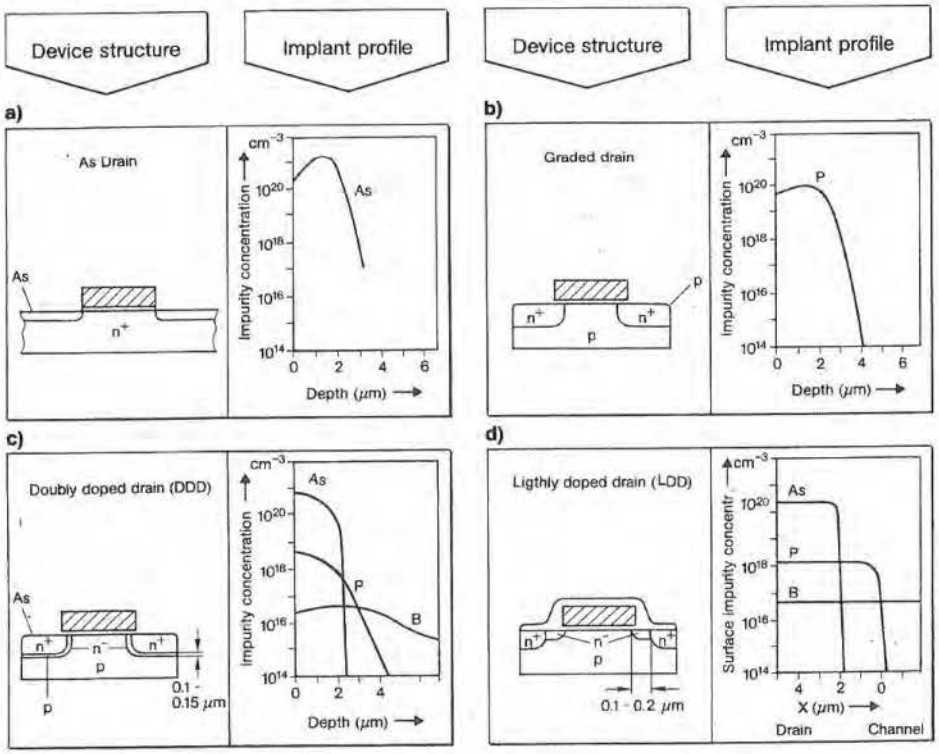

Figure 4-1: Different drain structures used in VLSI nMOS transistors

According to Miko et al., the LDD-structure can be used until the channel length is reduced below 0.8 μm, but lately, the 5 V power supply is replaced by 3.3 V and even lower. Therefore the LDD structure can even be used in the 0.5 μm technology and below. In the next section, the LDD structure is discussed in more detail and the need for this new structure is explained.

4.1.1. The LDD structure

In the LDD structure, narrow, self-aligned n^- regions are introduced between the channel and the n^+ regions as can be observed in Figure 4-2. This structure reduces impact ionisation (and thus hot-carrier emission) by spreading the high electric field at the drain pinchoff region into the n^- region. This allows a constant power supply voltage at reduced channel length to achieve a performance enhancement.

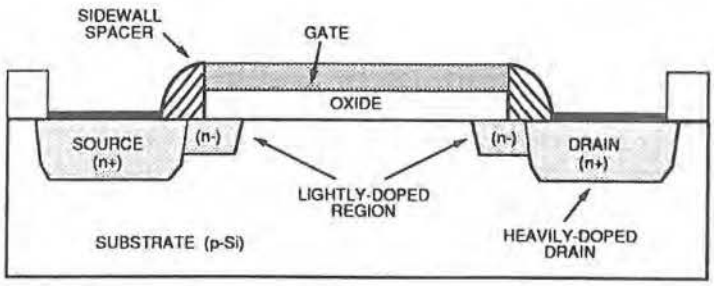

Figure 4-2: Schematic cross-section of a typically lightly doped drain (LDD) MOSFET

Although the diffusion coefficient of the n^- dopant (usually phosphorus) is higher than the diffusion coefficient of the n^+ dopant, the diffusion of n^- in the Si substrate is less in Figure 4-2 because only a low dose is implanted. In some technologies which will discussed in this work, n^- diffuses more than n^+ in the Si substrate.

The reduction in electric-field intensity due to the LDD structure is shown in Figure 4-3. This figure is taken from Ogura et al. [Ogur80] and is the result of a two-dimensional simulation. The electric field at the Si-SiO_2 interface as a function of distance along the channel near the drain is plotted for a conventional and an LDD device. Physical dimensions corresponding to the horizontal scale are shown on top of the figure. The electric field in the conventional device peaks approximately at the metallurgical junction and drops quickly to zero in the drain because no field can exist in the highly conductive n^+ region. On the other hand, the electric field in the LDD device extends across the n^- region before dropping to zero at the drain. For a given voltage drop, the area under the two curves are equal because:

$$V_{ds} = -\int_{S}^{D} \vec{E}.d\vec{r} \qquad (4\text{-}1)$$

Since the areas under the two field curves are equal for a given V_{ds}, the peak field in the LDD device must be lower than in the conventional device.

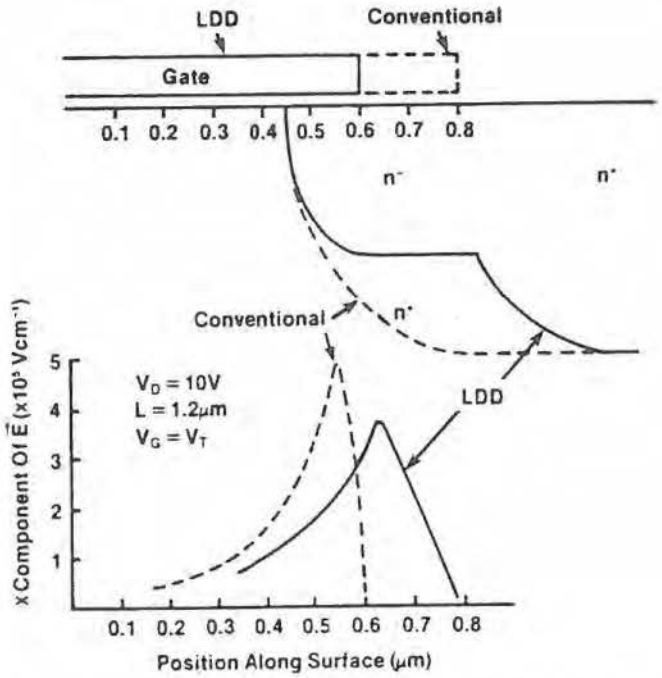

Figure 4-3:Magnitude of the electric field at the Si-SiO_2 interface as a function of distance. The physical geometries for both devices are shown above the plot.

As a consequence of the reduction in the maximum field intensity, an LDD nMOSFET shows a significantly reduced degradation. Thus, a shorter channel length can be used for a given supply voltage. That is why the LDD structure is widely used in today's short-channel MOSFETs.

As stated in chapter 3, the hot-carrier degradation in conventional nMOSFETs is largely due to interface state generation. The degradation results mainly from carrier mobility reduction. Interface state generation follows a simple time power-law relationship, and correlates closely with the time-dependent degradation of transistor parameters such as linear drain current and transconductance. LDD nMOSFETs, however, suffer additional degradation associated with the spacer oxide region. In this region, interface states can be generated and electrons can be trapped in the initial degradation phase. The n^- region

acts as a resistance in series with the channel and the degradation of this region increases the series resistance. This increase in series resistance saturates. After extensive stress times, the interface state generation moves to the channel region and causes a carrier mobility reduction.

The physical degradation mechanisms of LDD nMOSFETs are well accepted. Many models have been published to describe the degradation behaviour as a function of time and to extrapolate the lifetime under normal operating conditions. An overview of the existing models is given in section 4.3.2. A new degradation model will be proposed in section 4.3.3. Before this, degradation measurements on different wafer technologies will be shown in section 4.2.

Throughout this work, only the parameter $I_{d,lin}$ (and V_t for one technology) will be discussed. For most technologies, $g_{m,max}$ is also measured. The results of the measurement and the modelling of $g_{m,max}$ is shown in appendix B.

4.2. Hot-carrier degradation measurements on LDD nMOSFETs

Hot-carrier degradation measurements were performed on 3 different wafer technologies. All measurements were done at worst case conditions, this is at maximum I_{sub}. Usually, this maximum occurs at $V_g \sim (V_d-1)/2$, but it will be shown that deviations can occur. Therefore, I_{sub} will always be measured as a function of V_g to obtain the correct $V_g(I_{sub,max})$. These different technologies will be referred to as technology A, B and C respectively.

4.2.1. Technology A

A wafer of LDD nMOSFETs of a 0.5 μm technology with L=1μm, W=2 μm and t_{ox}=10 nm was fabricated. 250 nm oxide side-wall spacers are formed after P-implantation and before high-dose As implant. The MOSFETs were stressed at worst condition, this is at the peak of I_{sub}. Figure 4-4 shows the I_{sub}-V_g curves at the normal operating conditions and at the different stress conditions that have been applied.

Nine degradation measurements were performed at 8 different stress conditions. An overview of the different stress conditions is given in Table 4-1.

Number of measurements	V_d (V) during stress	V_g (V) during stress
1	4.5	1.75
1	4.75	1.81
2	5	1.87
1	5.25	2.03
1	5.5	2.17
1	5.75	2.24
1	6	2.34
1	6.25	2.46

Table 4-1:Overview of the degradation measurements on technology A

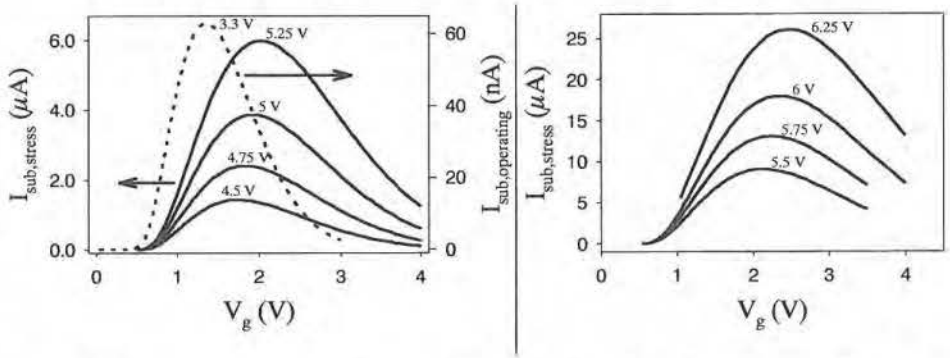

Figure 4-4: I_{sub} versus V_g at the lower stress conditions (left, left axis) and at the normal operating conditions (left, right axis); I_{sub} versus V_g at the higher stress conditions (right).

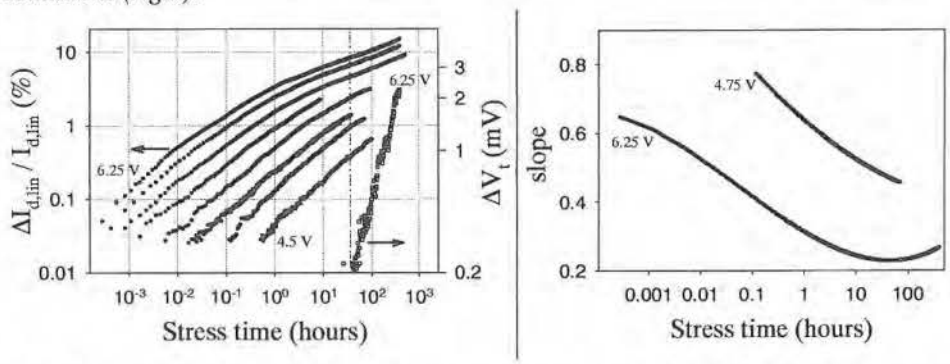

Figure 4-5: Degradation of $I_{d,lin}$ (left, left axis) and V_t (left, right axis) versus stress time at the different stress conditions; Calculated slope of the degradation curve versus stress time at V_d=6.25 V and V_d=4.75 V (right).

The degradation curves of $I_{d,lin}$ and V_t are depicted in Figure 4-5. In contrast with the hot-carrier degradation of conventional nMOSFETs, described in chapter 3, the degradation of $I_{d,lin}$ cannot be described by a straight line. At lower degradation levels, in this case below 1 %, the degradation of $I_{d,lin}$ follows a straight line but then, a saturating time dependence occurs. Many authors have described the saturating time dependence of the degradation behaviour of LDD nMOSFETs. The models, developed to describe this behaviour, will be discussed in the next section.

At the highest stress conditions, V_d= 5.75 V, 6 V and 6.25 V, the degradation behaviour increases from saturation to again a straight line after extensive stress times. This becomes clear in the right part of Figure 4-5 where the slope of the degradation curve is plotted versus the stress time for two different stress conditions: V_d=4.75 V and V_d=6.25 V. The continuously decreasing slope of the degradation curve at 4.75 V indicates the saturating time dependence. The slope of the degradation curve at 6.25 V increases again after extensive stress times. In conclusion, it can be stated that the degradation behaviour of $I_{d,lin}$ contains two different regions: in the first region, the time dependence of the degradation behaviour saturates while in the second region only a linear time dependence is measured.

Interesting to mention is the degradation of V_t which is also shown on Figure 4-5. For the lower stress conditions, V_t shows no change. Only in the transition from the first degradation region to the second, V_t starts to increase as is shown here for the highest stress condition: V_d = 6.25 V.

4.2.2. Technology B

A wafer of LDD nMOSFETs of a 0.25 μm technology with L=0.25μm, W=10 μm and t_{ox}= 5 nm was fabricated. The MOSFETs were again stressed at worst condition. The left part of Figure 4-6 shows the I_{sub}-V_g curves at the different stress conditions that were used in this experiment and at the normal operating conditions. Here, the peak of the substrate current is not around $(V_d-1)/2$ but appears at a V_g which is approximately equal to $V_d/2$. Four degradation measurements were performed. An overview of the different stress conditions is shown in Table 4-2.

The right part of Figure 4-6 shows the degradation of $I_{d,lin}$ as a function of stress time. The degradation behaviour is less complicated than it was the case in technology A. Only the first degradation region can be recognised: the degradation behaviour shows a saturating time dependence. The second region, which can be clearly recognised in the

degradation behaviour of technology A, is hardly visible here. In Figure 4-7, it can be seen that the slope starts to increase only in the last part of the degradation measurement. The figure at the top of Figure 4-7 is a zoom-in of the framed part of the slope versus stress time. In the last few hours of the measurement, the slope starts to increase but this is a small effect in comparison with the right part of Figure 4-5.

Number of measurements	V_d (V) during stress	V_g (V) during stress
1	2.8	1.45
1	3	1.51
1	3.4	1.63
1	3.6	1.69

Table 4-2: Overview of the degradation measurements on technology B

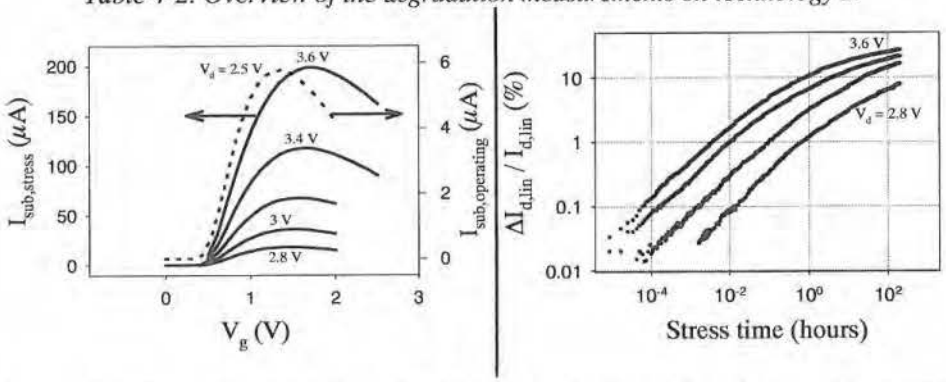

Figure 4-6: I_{sub} versus V_g at the different stress conditions (left, left axis) and at the normal operating conditions (left, right axis); Degradation of $I_{d,lin}$ versus stress time at the different stress conditions (right).

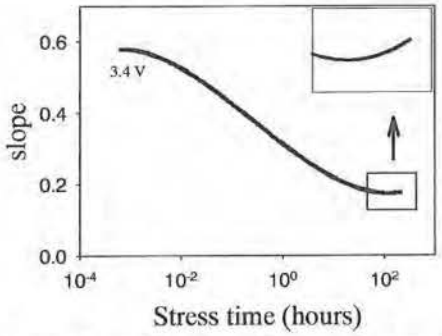

Figure 4-7: Slope of the degradation curve versus stress time at V_d=3.6 V

4.2.3. Technology C

For the third technology, measurements on a 0.18 μm technology of IMEC were performed on a measurement system with a low measurement resolution. L = 0.18 μm and W = 1 μm. 8 degradation measurements were performed at worst case condition and the V_d's during stress were 2.4, 2.6, 2.7, 2.85, 3, 3.1, 3.2 and 3.3 V respectively.

The left part of Figure 4-8 shows the degradation of $I_{d,lin}$ as a function of stress time. In this case, even the saturation behaviour is not very clear. The slope of the degradation curve versus the stress time, indicated in the right part of Figure 4-8 shows a limited but continuous decrease.

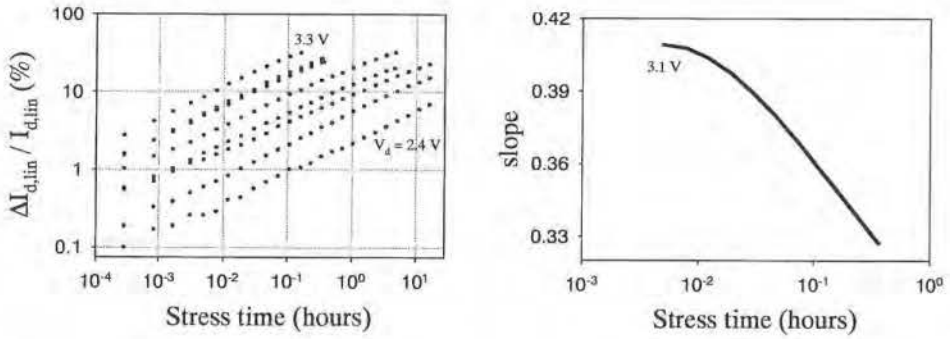

Figure 4-8: Degradation of $I_{d,lin}$ versus stress time at the different stress conditions (left); Slope of the degradation curve versus stress time at V_d=3.1 V (right).

The rest of this chapter focuses mainly on two parts. First, an analytical model which describes the two regions of the degradation behaviour will be derived, and then the lifetime at operating conditions of these three technologies will be estimated.

4.3. Modelling of the degradation behaviour

In this section, the degradation behaviour of LDD nMOSFETs will be modelled. First, it will be shown that the model of Hu does not describe the degradation behaviour. Then, an overview of the existing degradation models will be given. Finally, a new model will be developed and the lifetime predictions with the different degradation models will be compared.

4.3.1. Describing the degradation using the model of Hu

In a first attempt to model the degradation curves, the model of Hu is used. A simultaneous least-square linear fit of the degradation behaviour at the different stress conditions is performed with the following equation:

$$\frac{\Delta I_{d,lin}}{I_{d,lin}} = C\left[t\frac{I_d}{W}\left(\frac{I_{sub}}{I_d}\right)^{\varphi_{it}/\varphi_i}\right]^n \qquad (4\text{-}2)$$

Figure 4-9 and Figure 4-10 again shows the measurement of $I_{d,lin}$ for the three technologies A, B and C. The lines show the simultaneous least-square linear fit of the degradation curves, together with the predicted behaviour at normal operating conditions (represented by the dotted line).

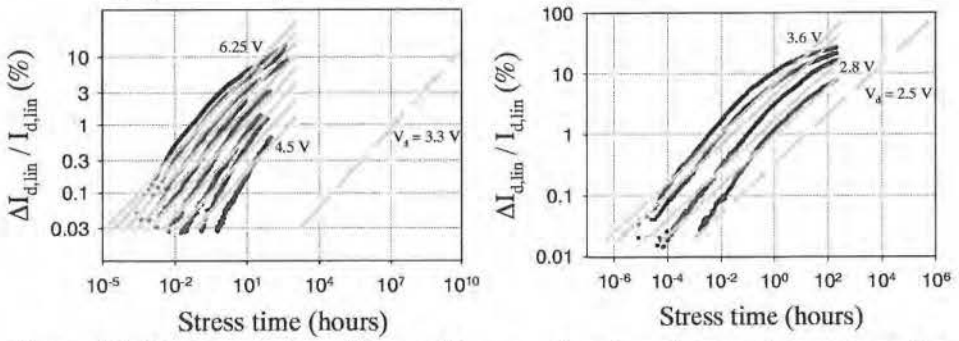

Figure 4-9: Percentage degradation of $I_{d,lin}$ as a function of stress time measured on technology A (left, dots) and on technology B (right, dots); Simultaneous Least-Square Linear Fit of the degradation curves at the different stress conditions with the model of Hu (lines) and the predicted behaviour at normal operating conditions (dotted line).

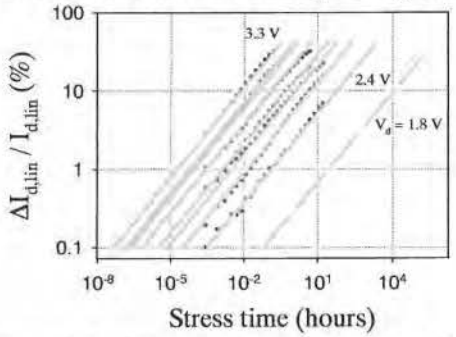

Figure 4-10: Percentage degradation of $I_{d,lin}$ as a function of stress time measured on technology C (dots); Simultaneous Least-Square Linear Fit of the degradation curves at the different stress conditions with the model of Hu (lines) and the predicted behaviour at normal operating conditions (dotted line).

The result of these fits are summarised in Table 4-3 and Table 4-4. The estimated fit parameters of the simultaneous least-square linear fit with the model of Hu for the three different technologies are shown in Table 4-3. The calculated lifetimes are shown in Table 4-4.

Although a lifetime prediction can be done, it is clear from Figure 4-9 and Figure 4-10 that the model of Hu can not be used to describe the degradation of LDD nMOSFETs properly. The degradation can not be described by a straight line on a logarithmic scale as is assumed by Hu's model. Nevertheless, the model of Hu is still widely used today. The next section describes a few attempts that have been made to model the hot-carrier degradation of LDD nMOSFETs. On the base of these models, a new degradation model will be developed in section 4.3.3.

Fit parameters	Technology A	Technology B	Technology C
C(*)	13.873	8.990	212.690
n	0.386	0.406	0.380
φ_{it}/φ_i	3.864	2.196	2.860

Table 4-3: Estimated fit parameters of the simultaneous least-square linear fit with the model of Hu for the three different technologies.

FC (%)	τ(Technology A) V_{dd}=3.3 V	τ(Technology B) V_{dd}=2.5 V	τ(Technology C) V_{dd}=1.8 V
0.1	1511.10 d	2.16e-3 d	2.63e-3 d
1	5.87e+5 d	0.63 d	1.13 d
10	2.28e+8 d	181.30 d	485.45 d

Table 4-4: Calculated lifetime in days of the parameter $I_{d,lin}$ for the three different technologies at the three different failure criteria.

4.3.2. Degradation models for LDD nMOSFETs: the history

Modelling the degradation behaviour of LDD nMOSFETs has been the subject of many studies since the end of the eighties. Many authors tried to explain the degradation

(*)The unit of C is %/(s.A/m) ^{n} , n has no unit

behaviour of the characteristic parameters. A consistent physical picture of the degradation mechanisms was developed. However, understanding these mechanisms is not enough. A model still needs to be developed in order to be able to fit the degradation behaviour of a characteristic parameter as a function of stress time. If possible, this model should be analytically determined instead of empirical. Also, the model should contain an acceleration factor. For example, in the model of Hu, described by equation (4-2), the acceleration factor is $I_d / W\left(I_{sub} / I_d\right)^{\varphi_{it}/\varphi_i}$. With the aid of this acceleration factor, a simultaneous fit of the degradation curves at all the stress conditions can be executed. Finally, it should be possible to extrapolate the lifetime of the DUT from the model. In conclusion, the model should fulfil the following conditions:

- Physically supported
- Analytically determined
- Contain a lifetime extrapolation method

An overview of the existing degradation models will now be given and the fulfilment of the above conditions will be examined. This overview is not complete. The most important papers have been selected on the base of how they fulfil the above conditions.

4.3.2.1. Cham et al. 1987

Literature: [Cham87]: The first observation in this paper is that the slope of the degradation curve is not a constant. The initial value of the slope is always greater than or equal to the final slope. The change in the slope is not very large, but an extrapolation in time using the initial slope can cause a very large error on a logarithmic scale. The second observation is that the initial slopes are dependent on the stress bias voltage. The slope is reduced with increasing stress voltage. This is also accompanied by a larger degradation for the higher stress bias voltage, as expected.

The dependence of the degradation on the total accumulated negative interface charge near the drain region was studied by performing a two-dimensional device simulation. This simulation showed that the degradation can exhibit a saturation behaviour. One possible explanation for this behaviour is that the negative interface charges accumulate above the LDD region, which form a depletion layer and increase the series resistance of the device. Assuming that the interface state charges are accumulating with a "block" distribution (constant density in a fixed region), the degradation stops when enough

negative charges have been accumulated to cause inversion at the silicon interface of the LDD region. However, a more realistic assumption would be to assume a "growing Gaussian" distribution, where the area of interface charge formation increases with time. Although some areas may be inverted and cause no further increase in the series resistance, the spread of the interface charge distribution increases the series resistance of other non-inverted areas as stress continues. Thus the degradation continues, but at a slower rate.

Discussion: This is one of the first papers which describes the time dependence of the hot-carrier degradation of LDD nMOSFETs. The paper lists experimental observations and some simulations. It contains no model for the description of the degradation behaviour as a function of time. Although the simulation provides no information on the time dependence, the slow-down of the degradation rate is qualitatively explained.

The fact that the initial slopes are dependent on the stress bias voltage is disputable. It is true when looking in a certain time window. For example when looking between 1 and 100 s of stress time, the slope of the lowest stress condition is much higher than the slope of the highest stress condition. Looking in a certain degradation window, the difference in slope is not that convincing anymore.

4.3.2.2. Liang et al. 1992

Literature: [Lian92]: In this paper, it is stated that the generally used power-law model [Hu85]:

$$\Delta(t) = A\left[t\frac{I_d}{W}e^{-\varphi_{it}/q\lambda E_m}\right]^n \qquad (4\text{-}3)$$

which has been discussed in chapter 3, holds true only for degradation below a certain threshold value. By extending the stress time further, the degradation exceeds the threshold value and starts to deviate from the power-law dependence. The degradation behaviour saturates.

During a degradation measurement, the hot electrons create trapped charges inside the gate oxide and generate defect states at the Si/SiO_2 interface. These charges and interface states form an electrical potential that repels subsequent incoming hot electrons away from the interface. Therefore, the energy barrier which the hot electron has to overcome to cause further damage is enhanced by the oxide trapped charges and interface states. By taking this barrier enhancement mechanism into consideration, the

rate equation for hot-electron degradation can be written as:

$$\frac{d\Delta}{dt} = A\, f(\Delta)\left(\frac{I_d}{W}\right)\exp\left[-\frac{\varphi_{it} + B\left(\Delta/\Delta_0\right)}{q\lambda E_m}\right] \tag{4-4}$$

where B and Δ_0 are model parameters for the barrier enhancement to the intrinsic barrier φ_{it} due to the existing damage. Parameter Δ_0 represents the threshold value of degradation above which the contribution of Δ to the energy barrier becomes significant. The physical explanation for the existence of such a threshold is that, for $\Delta < \Delta_0$, the high-field region of the channel is only partially damaged and there are still sites available for the incoming hot carrier to create damage by just overcoming a barrier φ_{it}. For $\Delta > \Delta_0$, the oxide trapped charge and interface states from hot-carrier stressing distribute along the whole high-field region and the enhanced barrier begins to influence the degradation behaviour. Function $f(\Delta)$ is introduced to be consistent with the power-law model at low Δ, and it can be approximated using the empirical expression:

$$f(\Delta) = \frac{1}{\tanh\left[\left(\Delta/\Delta_0\right)^k\right]\Delta_0{}^k} \tag{4-5}$$

where k is a constant. For $\Delta < \Delta_0$, the function can be approximated by its first-order Taylor expansion:

$$f(\Delta) \approx \Delta^{-k} \tag{4-6}$$

and placing equation (4-6) into (4-4) and solve for Δ, a power-law dependence of Δ on the stress time is obtained:

$$\Delta \approx A\, t^{1/k+1} \tag{4-7}$$

where A and k can be extracted from the slope and intercept of the linear plot of log (Δ) versus log (t) for $\Delta < \Delta_0$. For $\Delta > \Delta_0$, $f(\Delta)$ approaches a constant value of $\frac{1}{\Delta_0{}^k}$ and thus:

$$\Delta \approx \ln t \tag{4-8}$$

The last result shows that when the hot-carrier damage reaches and exceeds the threshold value, Δ shows a logarithmic dependence on stress time t and starts to saturate.

Discussion: The model of Liang is physically well supported and forms a good representation of the degradation measurements. The derivation of the model is based on the physical insight of barrier enhancement and on the empirical formula for the function f(Δ). For the derivation of (4-7) and (4-8), many approximations need to be done. The model contains no acceleration factor, which means that a simultaneous fit of all the stress conditions is not possible. Lifetime extrapolation to normal operating conditions is not possible with the proposed model.

4.3.2.3. Chan et al. 1995

Literature: [Chan95]: In this paper, a two-stage degradation mechanism for oxide-spacer LDD nMOSFET devices is identified. The device degradation starts with the trapping of electrons in the oxide spacers which results in an increase in the series resistance of the LDD region. The increase in series resistance saturates. After extensive stress times, the carrier mobility in the channel region decreases. This two-stage degradation process is evident from the relation between the linear-current degradation and charge-pumping current depicted in the left part of Figure 4-11. This relation exhibits two distinct regions: in region I, the linear-current degradation will be shown to be dominated by the increase in the series resistance in the LDD region. In region II, the degradation will be shown to be mostly due to mobility reduction, as in the case of conventional devices.

During the stress, the observed changes of substrate current are also a result of the two-stage degradation process. The substrate current first decreases, then increases. This variation is the result of the changes in the channel electric field near the drain:

$$E_D \approx \frac{V_{D,eff} - V_G + V_t}{l_C} \qquad (4\text{-}9)$$

At low stress times, due to the increase in the series resistance, the effective drain voltage $V_{D,eff} = V_D - I_D.R_D$ is reduced, and thus the channel electric field decreases. As a result, the substrate current decreases at first. As the stress proceeds, however, the substrate current increases due to the stress-induced increase in the threshold voltage which now results in a larger electric field according to (4-9). The variation of the substrate current as a function of the stress time is shown in the right part of Figure 4-11.

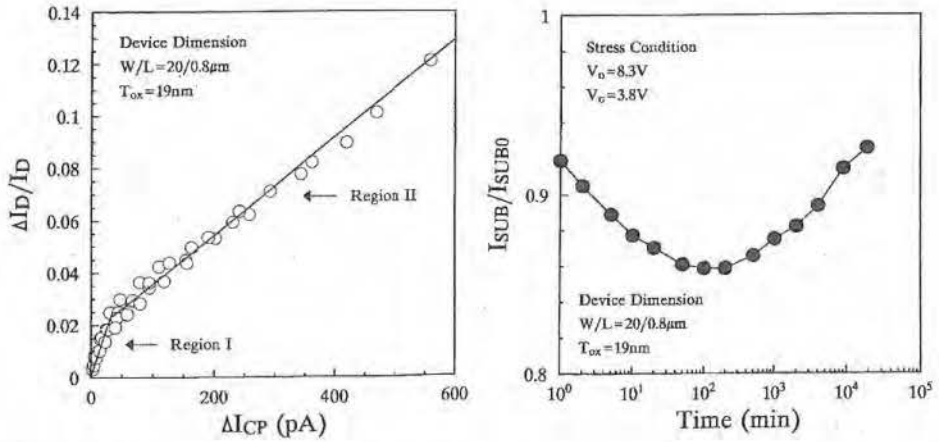

Figure 4-11: Relation between the linear-current degradation and charge-pumping current for several stressed devices (left); Substrate current variation during hot-carrier stress (right).

In order to understand this two-stage degradation process, interface states have been spatially profiled by charge-pumping experiments, and their extracted lateral spatial distribution is shown in the left part of Figure 4-12. It shows that the peak interface-state damage occurs inside the LDD region. This result is expected since the peak electric field exists inside the LDD region. Nonnegligible interface-state generation also occurs in the channel. Therefore, as stress proceeds and more negative charge accumulates outside the LDD region, threshold voltage will start to increase.

By combining the effects of series-resistance increase and mobility reduction, the linear-current degradation for LDD nMOSFETs can be expressed as:

$$\frac{\Delta I_D}{I_D}(t) = f(R_D(t)) + C\left[t\frac{I_D}{W}\left(\frac{I_{sub}}{I_D}\right)^{\varphi_{it}/\varphi_i}\right]^n \qquad (4\text{-}10)$$

The first term represents the current reduction due to the increase in series resistance, and the second term represents the contribution of mobility reduction which follows the same model as in conventional devices [Hu85]. The exact functional form of $f(R_D(t))$ is unknown. However, it is not important in lifetime extrapolation, as $f(R_D(t))$ will eventually saturate and this saturation level is usually much lower than typical failure criterions. By using the asymptotic value of the degradation rate coefficient n, the model of Hu can still be used to project the device lifetime for LDD nMOSFETs.

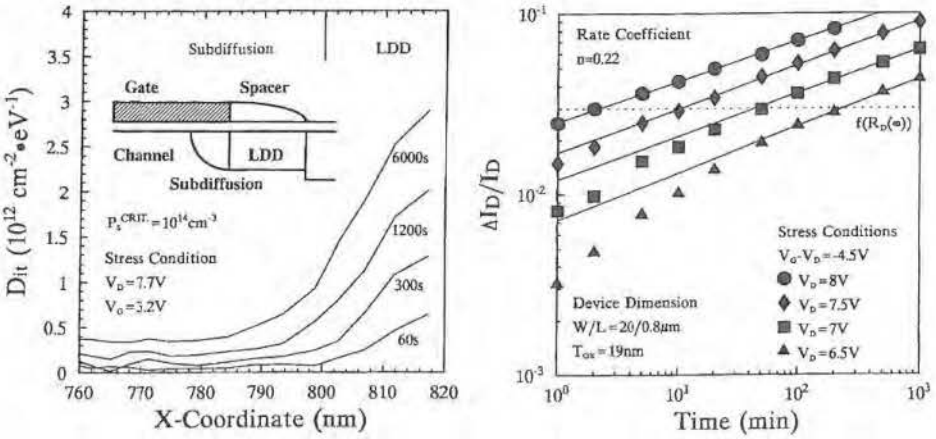

Figure 4-12: Extracted lateral interface-state distribution along the MOSFET (left); Time dependence of the linear-current degradation. The solid lines are asymptotes of the degradation time dependence (right).

By subtracting the degradation due to the saturated increase in series resistance and by using the asymptotic degradation rate coefficient, the hot-carrier lifetime correlation can be expressed as:

$$\tau\frac{I_D}{W}=C'\left[FC-f\left(R_D(\infty)\right)\right]^{1/n}\left(\frac{I_{sub}}{I_D}\right)^{-\varphi_{it}/\varphi_i} \qquad (4\text{-}11)$$

where FC is the failure criterion and $f(R_D(\infty))$ is the maximum amount of current reduction due to the saturated series resistance increase. The right part of Figure 4-12 illustrates how to use the asymptotic value of the rate coefficients to extract the correct lifetime.

Discussion: The model of Chan is physically well founded. Unfortunately, the empirical formula, for describing the degradation behaviour in time, contains an unknown function $f(R_D(t))$, thus fitting the degradation curves completely is not possible. Although lifetime prediction is possible, it is limited to the case that the FC > $f(R_D(\infty))$ and this lower limit is technology dependent. For technology A, this saturation value is around 6 %. Figure 4-13 shows the result of the simultaneous least-square linear fit of the degradation curves above saturation value with the model of Hu. The values for the coefficients obtained from the fit are C=18.90, n=0.24 and φ_{it}/φ_i=4.80. With the aid of these fit coefficients and with the measured I_{sub} and I_d at operating conditions (V_{dd}=3.3 V), the lifetime at the desired FC can be calculated. For a FC of 0.1 %,

τ=0.36 years, if FC=1 %, τ=4899 years and if FC=10 %, τ=67 120 048 years.

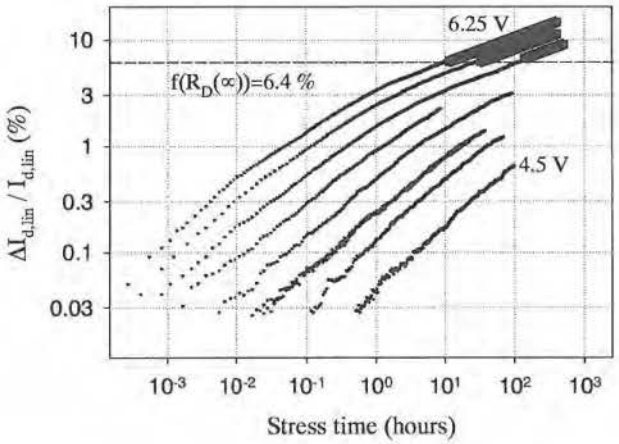

Figure 4-13: Simultaneous least-square linear fit of the degradation curves above the saturation value with the model of Hu.

For technology B, the transition from the first to the second region is not so obvious. It is hard to tell from which percentage of degradation the damage has shifted towards the channel region and therefore the model of Chan can not be used on this technology. For technology C, the saturation value is never reached and thus the model of Chan can not be used here.

4.3.2.4. Goo et al. 1995

Literature: [Goo95]: Goo et al. suggested a three-MOSFET-equivalent circuit, which is comprised of an enhancement-mode MOSFET and two depletion-mode MOSFETs, to explain the degradation of LDD nMOSFETs and reproduce successfully the saturation of the degradation of the LDD region. In that equivalent circuit, each depletion-mode MOSFET acts as a bias-dependent-series resistance.

However, the effect of the source-side resistance as a part of intrinsic channel characteristic does not need to be regarded because the n^- region of the source side is not degraded during maximum I_{sub} condition. Therefore, a three-MOSFET circuit can be simplified to a two-MOSFET circuit shown in Figure 4-14.

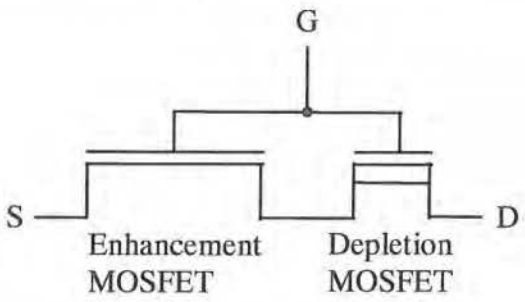

Figure 4-14: Schematic diagram of the equivalent circuit for LDD nMOSFETs after hot-carrier stress.

In the linear region, where V_d = 0.1 V, the drain current in reverse mode (source and drain were exchanged) is given by:

$$I_{d_{without}} \approx \beta\left(V_g - V_t\right)V_d \tag{4-12}$$

$$I_{d_{with}} \approx \beta\left(V_g - R_S I_{d_{with}} - V_t\right)\left(V_d - R_S I_{d_{with}}\right) \tag{4-13}$$

where $I_{d_{without}}$ and $I_{d_{with}}$ are respectively the currents for without and with a source-side series resistance which represents the n^- region of the drain side in forward mode stress, $\beta = \mu C_{ox}\left(W_{eff}/L_{eff}\right)$, μ is the channel mobility, C_{ox} is the gate oxide capacitance, W_{eff} is the effective channel width, L_{eff} is the effective channel length and R_S is the source-side series resistance. Equation (4-13) can be written as:

$$\begin{aligned} I_{d_{with}} &\approx \beta\left(V_g - V_t\right)V_d \\ &-\beta\left(V_g - V_t\right)R_S I_{d_{with}} \\ &-\beta R_S I_{d_{with}}\left(V_d - R_S I_{d_{with}}\right) \end{aligned} \tag{4-14}$$

By combining equation (4-12) and (4-14), the current with a series resistance can be described as:

$$I_{d_{with}} \approx \frac{I_{d_{without}}}{1+\beta R_S\left(V_g - V_t\right)} \tag{4-15}$$

for $V_d >> R_S I_{d_{with}}$ and $\left(V_g - V_t\right) >> V_d$ The n^- region is represented by a depletion mode MOSFET. The current in a depletion MOSFET can also be described as:

$$I_{d_{n^-}} \approx \beta_{n^-} \left(V_g - V_{t_{n^-}} \right) V_d \tag{4-16}$$

where $\beta_{n^-} = \mu_{n^-} C_{ox} \left(W_{eff_{n^-}} / L_{eff_{n^-}} \right)$, μ_{n^-} is the n^- region mobility, $W_{eff_{n^-}}$ is the effective channel width, $L_{eff_{n^-}}$ is the effective channel length of the n^- region and $V_{t_{n^-}}$ is the threshold voltage in the n^- region. Using Ohm's law, equation (4-16) leads to:

$$\frac{V_d}{I_{d_{n^-}}} = R_S \approx \frac{1}{\beta_{n^-} \left(V_g - V_{t_{n^-}} \right)} \tag{4-17}$$

Equation (4-15) can then be written as:

$$I_{d_{with}} \approx \frac{I_{d_{without}}}{1+K} \tag{4-18}$$

where:

$$K = \frac{\beta \left(V_g - V_t \right)}{\beta_{n^-} \left(V_g - V_{t_{n^-}} \right)} \tag{4-19}$$

is the conductance ratio of the channel region to the n^- region.

An empirical model has been generally used to relate generated interface-state charge to a corresponding reduction in the inversion-layer mobility μ_1 [Sun80]:

$$\mu_1 = \frac{\mu_0}{1 + C_1 N_{it}} \tag{4-20}$$

where μ_0 is the inversion-layer mobility of the virgin device and C_1 is a fitting constant. Similar to the case of the inversion layer, higher interface-state charge densities result in lower electron mobility in the accumulation layer. Therefore, this empirical relation may be available for the mobility reduction of the n^- region as well, but has to be converted to allow the saturation of mobility decrease of this region.

The generated interface-states in the gate oxide affect the surface scattering. But the carrier distribution in the n^- region accumulation layer can be further away from the Si/SiO_2 interface then in the channel inversion layer, and the negative charge due to the stress pushes the current path even deeper into the substrate. Thus after stress, the

electrons pass over through a deeper path. Therefore, the mobility degradation in the n^- region eventually saturates, even if the interface-state charge is continuously increased. Moreover, the generated interface-state charge in the LDD region exhibits a declined gradient at extensive stress because φ_{it}, the critical energy barrier for interface-state generation, is enhanced by interface state charge [Lian92]. Therefore, it is expected that the mobility degradation in the n^- region has a limit, which determines the saturation level of the hot-carrier induced current degradation. This behaviour can be described as:

$$\frac{\mu_{1,n^-}}{\mu_{0,n^-}} = \delta + \frac{1-\delta}{1+\gamma t^n} = F_1(t) \tag{4-21}$$

where μ_{0,n^-} and μ_{1,n^-} are mobilities of the n^- accumulation layer before and after stress respectively, γ is a stress-bias-dependent fitting constant, n is a process-dependent fitting constant, δ is the limit of mobility degradation and F_1 is a function. By combining (4-18)-(4-21), the drain currents before and after stress can be written as:

$$I_{d0} = \frac{I_{d,orig}}{1+K_0} \tag{4-22}$$

$$I_{d1} = \frac{I_{d,orig}}{1+K_1} = \frac{I_{d,orig}}{1+K_0/F_1(t)} \tag{4-23}$$

where $I_{d,orig}$ is the current through the MOSFET without n^- region, K_0 and K_1 are the conductance ratios before and after stress. Combining (4-21)- (4-23) yields the final form for the percentage reduction of current as:

$$\frac{\Delta I_d}{I_{d0}} = \frac{I_{d0}-I_{d1}}{I_{d0}} = \frac{C_1 t^n}{1+C_2 t^n} \tag{4-24}$$

where $C_1 = \frac{K_0(\gamma-\delta\gamma)}{1+K_0}$ and $C_2 = \frac{\delta\gamma+K_0\gamma}{1+K_0}$. In this model, n determines the initial degradation slope, K_0 determines the degradation level, γ determines the weighting factor $\left(I_d/W_{eff}\right)\left(I_{sub}/I_d\right)^{\varphi_{it}/\varphi_i}$ and δ determines the saturation level of degradation.

A new lifetime prediction method was proposed in [Goo94]. Here, it is shown that the degradation curves have a universal behaviour, even if different stress conditions were applied. This means that the curves at different stress conditions can coincide by shifting

them parallel in time as shown in the left part of Figure 4-15. In this figure, the degradation of $I_{d,lin}$ is shown as a function of normalised time at all the different stress conditions. The normalised time is a product of stress time and a normalised weighting factor chosen to be 1 for 5 V stress.

If the failure time at one of the accelerated stress conditions is measured, the failure time at other stress conditions can be accurately determined from the amount of shift required to lay one degradation curve on top of the other. If the failure times at all the different stress conditions are determined, the lifetime of the device at the operating conditions can be determined by using the conventional $\log(\tau.I_d)$ versus $\log(I_{sub}/I_d)$ method as shown in the right part of Figure 4-15 for two different failure criteria: 1 and 10 %.

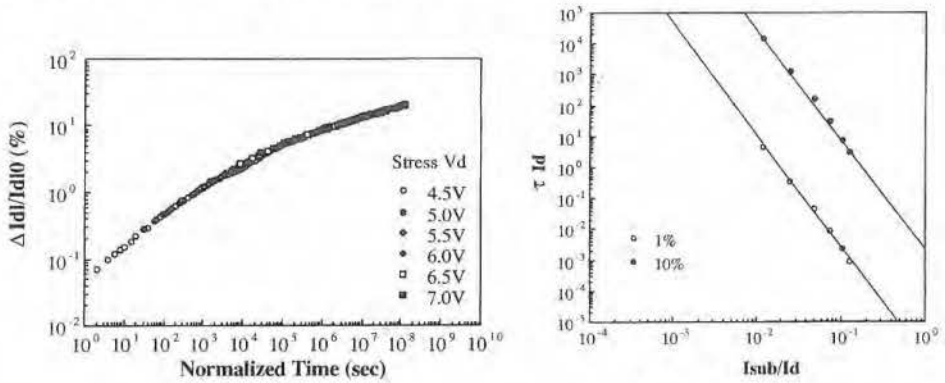

Figure 4-15: Degradation of $I_{d,lin}$ versus normalised stress time (left); Hu plot for two different failure criteria (right).

Discussion: The model of Goo is physically well founded and analytically determined. Only the parameter δ has no physical interpretation. It contains no acceleration factor, thus a simultaneous fit of all the stress conditions is not possible. The model is also limited to the description of the degradation of the LDD region. The transition to the mobility reduction in the channel is not enclosed. Thus, the model can not be applied above the saturation value. This is shown in the left part of Figure 4-16: The dots represent the degradation of $I_{d,lin}$, measured on Technology A, versus the normalised stress time. The normalised stress time is again the product of stress time and a normalised weighting factor chosen to be 1 for 4.75 V stress. The line represents the least-square non-linear fit of the universal curve. The three highest stress conditions are not included in the fit. The fit equation is given in (4-24) and the estimated fit parameters are shown in the second column of Table 4-5. It can be clearly observed that

above the saturation value, a deviation occurs between the measurement and the fit. The model of Goo can thus only be used below the saturation value and this value is technology and parameter dependent. In appendix B, it is demonstrated that the model of Goo works fine for modelling the degradation behaviour of $g_{m,max}$ of technology A, although the model is derived for the parameter $I_{d,lin}$. The degradation of $g_{m,max}$ did not reach the saturation level yet.

Although it is mathematically rather unfounded, a good lifetime prediction method is provided with the model of Goo. This is shown in the right part of Figure 4-16. In this figure, a Hu plot is shown for two different failure criteria. Goo did not prove that a Hu plot can be used, but as can be clearly seen in this figure, the different points fall on a straight line. The calculated lifetimes at the two failure criteria are given in the second column of Table 4-6.

The model of Goo is also applied to Technology B. The result is shown in Figure 4-17. Here, a deviation between the measurements and the model also occurs at high degradation levels but the determination of the saturation value is not so simple. The estimated fit coefficients and the calculated lifetimes at three different failure criteria are given in the third column of Table 4-5 and Table 4-6 respectively.

Finally, the model is also applied to technology C as shown in Figure 4-18. On this technology, the saturation value is not reached and thus no deviation occurs between the measurements and the fit with the model of Goo. The estimated fit coefficients and the calculated lifetimes at three different failure criteria are given in the last column of Table 4-5 and Table 4-6 respectively.

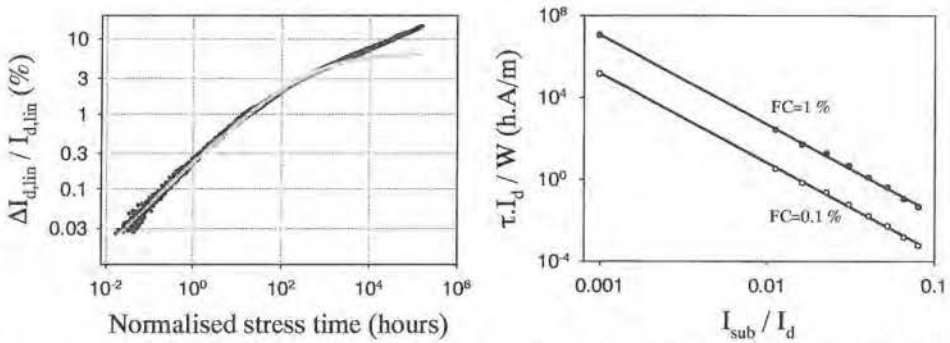

Figure 4-16: Degradation of $I_{d,lin}$, measured on technology A, versus normalised stress time (left, dots);. Least-square non-linear fit of the degradation curves with the model of Goo (left, line); Hu plot for two different failure criteria (right).

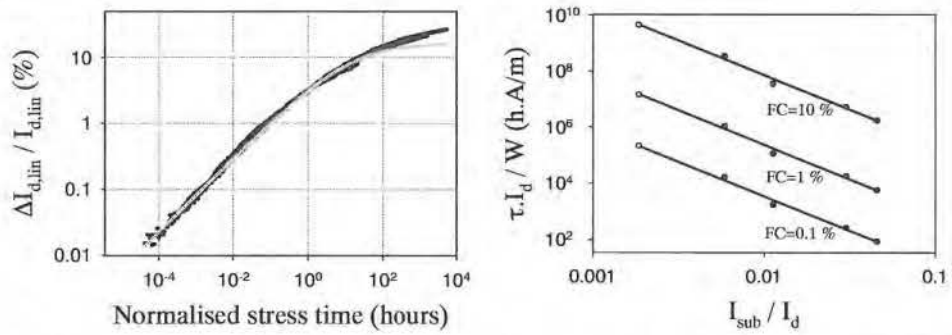

Figure 4-17: Degradation of $I_{d,lin}$, measured on technology B, versus normalised stress time (left, dots); Least-square non-linear fit of the degradation curves with the model of Goo (left, line); Hu plot for three different failure criteria (right).

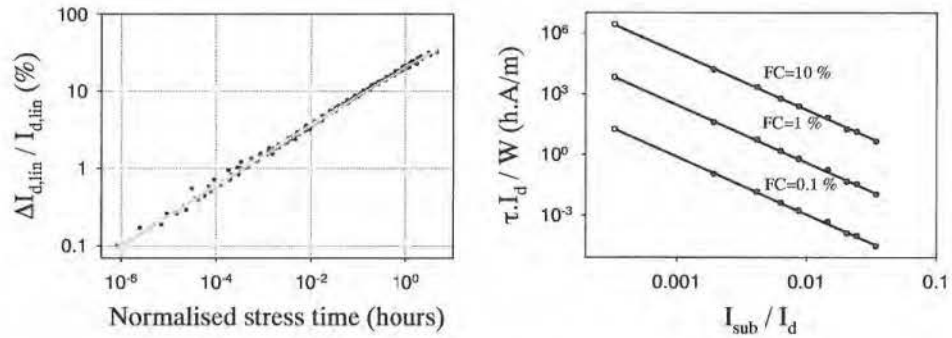

Figure 4-18: Degradation of $I_{d,lin}$, measured on technology C, versus normalised stress time (left, dots); Least-square non-linear fit of the degradation curves with the model of Goo (left, line); Hu plot for three different failure criteria (right).

Fit parameters	Technology A	Technology B	Technology C
C_1(*)	0.233	3.813	22.500
C_2(*)	0.0353	0.233	0.0970
n	0.565	0.556	0.391

Table 4-5: Estimated fit parameters of the simultaneous least-square linear fit with the model of Goo for the three different technologies.

(*) The unit of C_1 is $\%/s^n$ and of C_2 $1/s^n$, n has no unit

FC (%)	τ(Technology A) V_{dd}=3.3 V	τ(Technology B) V_{dd}=2.5 V	τ(Technology C) V_{dd}= 1.8 V
0.1	5.87e+3 d	8.37e-3 d	3.10e-3 d
1	4.51e+5 d	0.58 d	1.13 d
10	x	177.09 d	448.95 d

Table 4-6: Calculated lifetime in days of the parameter $I_{d,lin}$ for the three different technologies at the three different failure criteria

4.3.3. New degradation model

The new model will be based on Goo et al. and this for two reasons. First, because it is a physically well founded and an analytically determined model. Second, because it can be observed that this model represents our degradation measurements well. The model has to be refined, also for two reasons. First, the limit of mobility degradation should be more physically founded. Second, an advanced lifetime prediction method needs to be calculated. The lifetime prediction method proposed in the previous section is based on the determination of the acceleration factor after a manual shift of each individual curve. In this section, the more advanced fit technique, proposed in the previous chapter is used, allowing a simultaneous fit of all curves. Thus, this section will contain three subsections. First, a refined model of Goo will be presented. This model describes only the degradation of the spacer oxide. After extensive stress times, the degradation extends to the gate oxide. This second term is added to the model in the second subsection where the new model is generalised to the complete degradation area from 0.02 % up to more than 10 %. In the third subsection, the new lifetime extrapolation technique, proposed in chapter 3 will be used to predict the lifetimes of the three different technologies for different FC.

4.3.3.1. Refined model of Goo

The same equivalent circuit will be used as proposed by Goo and shown in Figure 4-14: a two-MOSFET circuit with one enhancement and one depletion mode MOSFET. Again, the depletion-mode MOSFET acts as a bias-dependent-series resistance. The starting equations, proposed by Goo in (4-12) and (4-13) will be changed because all degradation measurements are performed in forward mode, thus source and drain are not exchanged during the measurement. In the linear region the drain current in forward

mode is given by:

$$I_{d_{without}} \approx \beta\left(V_g - V_t\right)V_d \tag{4-25}$$

$$I_{d_{with}} \approx \beta\left(V_g - V_t\right)\left(V_d - R_D\, I_{d_{with}}\right) \tag{4-26}$$

where $I_{d_{without}}$ and $I_{d_{with}}$ are respectively the currents for without and with a drain-side series resistance which represents the n^- region of the drain, $\beta = \mu C_{ox}\left(W_{eff}/L_{eff}\right)$ and R_D is the drain-side series resistance. Equation (4-26) can be written as:

$$I_{d_{with}} \approx \beta\left(V_g - V_t\right)V_d - \beta R_D\, I_{d_{with}}\left(V_g - V_t\right) \tag{4-27}$$

By combining equation (4-25) and (4-27), the current with a series resistance can be described as:

$$I_{d_{with}} \approx \frac{I_{d_{without}}}{1+\beta R_D\left(V_g - V_t\right)} \tag{4-28}$$

The difference with the model of Goo is that this equation is obtained without making any approximations. The n^- region is represented by a depletion mode MOSFET. The current in a depletion MOSFET can again be described as:

$$I_{d_{n^-}} \approx \beta_{n^-}\left(V_g - V_{t_{n^-}}\right)V_d \tag{4-29}$$

where $\beta_{n^-} = \mu_{n^-} C_{ox}\left(W_{eff_{n^-}}/L_{eff_{n^-}}\right)$. Using Ohm's law, equation (4-29) leads to:

$$\frac{V_d}{I_{d_{n^-}}} = R_D \approx \frac{1}{\beta_{n^-}\left(V_g - V_{t_{n^-}}\right)} \tag{4-30}$$

Equation (4-28) can again then be written as:

$$I_{d_{with}} = \frac{I_{d_{without}}}{1+K} \tag{4-31}$$

where:

$$K = \frac{\beta\left(V_g - V_t\right)}{\beta_{n^-}\left(V_g - V_{t_{n^-}}\right)} \tag{4-32}$$

is the conductance ratio of the channel region to the n^- region.

The model of Sun, given in (4-20), needs to be adjusted to describe the saturation of the

degradation. In contrast to Goo, a more physical picture will be shown to explain the saturation behaviour. This is done with the aid of Figure 4-19. After the electrons have travelled through the channel resistance R_{ch} they reach a parallel connection of resistances R_1 to R_n in the n^- region. For the virgin device, R_1 is the smallest of all resistors and thus the main part of the electrons flows close to the surface into the drain. When damage is created in the SiO_2 or in the Si-SiO_2 interface, R_1 increases and thus electrons will choose a lower path. After an extensive stress period, all resistances reach a very high value because of the damage created by hot-carriers, except R_n, which is unaffected by the damage because the distance to the surface of the LDD region is too high. In reality, current is not flowing through a single resistance R_n but through the equivalent resistance R_{eq} of the parallel resistance circuit. Thus finally, all electrons flow through R_{eq} and even if the damage is still increased, the current is unaffected. This describes the saturation behaviour of the mobility degradation.

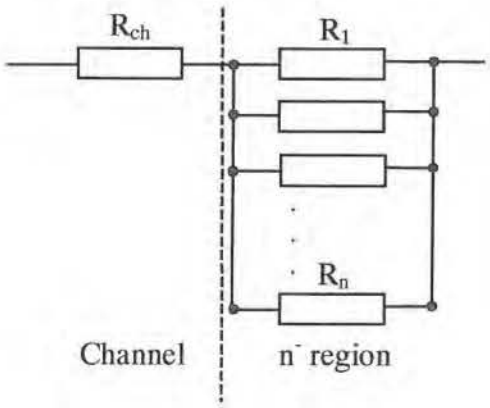

Figure 4-19: Schematic circuit for the channel and the n^- region in an LDD nMOSFET subjected to hot-carrier stress at maximum I_{sub} condition.

Sun's model has to be adjusted so that it takes into account the above description:

$$\frac{\mu_{1_{n^-}}}{\mu_{0_{n^-}}} = \frac{R_{eq}(t=0)}{R_{eq}(t=\infty)} + \frac{1 - R_{eq}(t=0)/R_{eq}(t=\infty)}{1 + C_2 D} \qquad (4\text{-}33)$$

where $\mu_{0_{n^-}}$ and $\mu_{1_{n^-}}$ are the mobilities of the n^- accumulation layer before and after stress respectively, the ratio of the equivalent resistance at t=0 and infinity is the upper limit of mobility degradation, C_2 is a fitting constant and D is the damage created in the SiO_2 or in the Si-SiO_2 interface.

If we suppose that the mechanism for damage creation is the same in the spacer oxide than in the SiO_2, the model of Hu can be used to evaluate D:

$$D = A'\left[t\frac{I_d}{W}\left(\frac{I_{sub}}{I_d}\right)^{\varphi_{it}/\varphi_i}\right]^n \tag{4-34}$$

Inserting (4-34) into (4-33) yields:

$$\frac{\mu_{1_{n^-}}}{\mu_{0_{n^-}}} = \frac{R_{eq}(t=0)}{R_{eq}(t=\infty)} + \frac{1 - R_{eq}(t=0)/R_{eq}(t=\infty)}{1 + C_3\left[t\frac{I_d}{W}\left(\frac{I_{sub}}{I_d}\right)^{\varphi_{it}/\varphi_i}\right]^n} = F(t) \tag{4-35}$$

After stress, equation (4-31) can be written as:

$$I_{d,with1} = \frac{I_{d,without1}}{1+K_1} \tag{4-36}$$

The degradation occurs in the spacer oxide above the LDD region. The mobility in the channel shows no degradation and thus: $\mu_1 = \mu_0$. As a consequence: $K \propto 1/\mu_{n^-}$ and with the aid of equation (4-35) follows:

$$K_1 = \frac{K_0}{F(t)} \tag{4-37}$$

Inserting (4-37) into (4-36) leads to:

$$I_{d,with1} = \frac{I_{d,without1}}{1 + K_0/F(t)} \tag{4-38}$$

and without stress:

$$I_{d,with0} = \frac{I_{d,without0}}{1+K_0} \tag{4-39}$$

Because the degradation only occurs in the n- region: $I_{d,without1} = I_{d,without0}$ and thus the degradation of the linear drain current can be written as:

$$\frac{\Delta I_d}{I_{d0}} = \frac{I_{d,with1} - I_{d,with0}}{I_{d,with0}} \tag{4-40}$$

After some calculation, it can be found that:

$$\frac{\Delta I_d}{I_{d0}} = \frac{C_4 \left(t \frac{I_d}{W} \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right)^n}{1 + C_5 \left(t \frac{I_d}{W} \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right)^n} \qquad (4\text{-}41)$$

where: $C_4 = \frac{C_3 K_0 \left(R_{eq}(t=0)/R_{eq}(t=\infty) - 1 \right)}{1+K_0}$, $C_5 = \frac{C_3 \left(R_{eq}(t=0)/R_{eq}(t=\infty) + K_0 \right)}{1+K_0}$

Equation (4-41) has the same shape as equation (4-24) and forms a good description of the degradation of the current in the linear region of an LDD nMOSFET at relatively low degradation levels. As long as the degradation is restricted to the spacer oxide region, the model forms a good description of the measurements. Once the damage reaches the gate oxide, the model deviates from the measurements. This is demonstrated in Figure 4-20 on Technology A en B. The dots represent the percentage degradation of $I_{d,lin}$ as a function of stress time. The lines represent the simultaneous least-square non-linear fit of the degradation curves at the different stress conditions with the refined model of Goo given by equation (4-41). The estimated fit coefficients are shown in the second and third column of Table 4-7 for technology A and B respectively.

At low degradation levels, this model forms a good description of the degradation measurements for both technologies. For technology A, the limit of degradation is 6 %. The degradation of the spacer oxide saturates at 6 %. The extension of the degradation to the gate oxide is not included in the model and therefore, the simultaneous least-square fit deviates from the degradation measurements above 6 %. For technology B, the determination of the saturation value is not simple, deviation between the measurements and the model occur around 15 %.

For the degradation of technology C, the saturation value is not reached and thus the model of Goo is a good description of the complete degradation area from 0.02 up to more than 10 %. This is shown in Figure 4-21. The estimated fit coefficients are shown in the last column of Table 4-7.

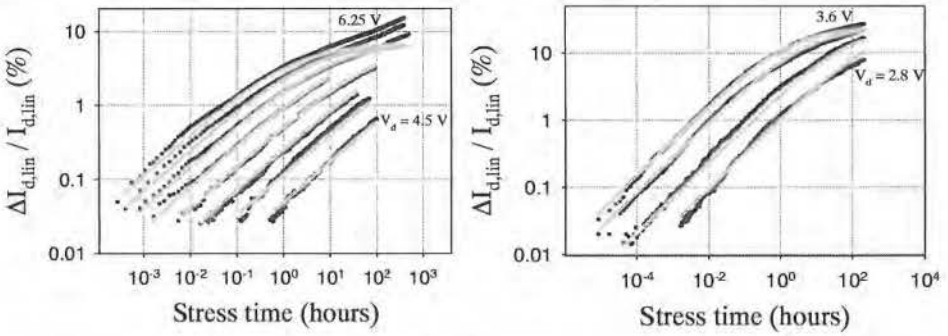

Figure 4-20: Percentage degradation of $I_{d,lin}$ as a function of stress time measured on technology A (left, dots) and technology B (right, dots); Simultaneous Least-Square Non-Linear Fit of the degradation curves at the different stress conditions with the refined model of Goo (lines).

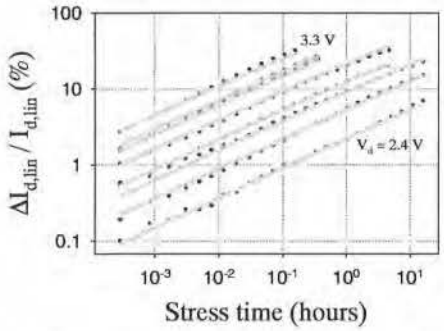

Figure 4-21: Percentage degradation of $I_{d,lin}$ as a function of stress time measured on technology C (dots); Simultaneous Least-Square Non-Linear Fit of the degradation curves at the different stress conditions with the refined model of Goo (lines).

The refined model of Goo will now be generalised in order to describe the degradation of technology A and B in the complete degradation area, from 0.02 up to more than 10%.

Fit parameters	Technology A	Technology B	Technology C
C_1(*)	71.093	44.888	241.329
C_2(*)	10.194	1.838	1.054
n	0.559	0.523	0.389
φ_{it}/φ_i	3.838	2.502	3.344

Table 4-7: Estimated fit parameters of the simultaneous least-square linear fit with the refined model of Goo for the three different technologies.

4.3.3.2. Generalisation of the model to the complete degradation area

The deviation of the model from the degradation measurements can be explained by the fact that the model only describes the degradation of the spacer oxide above the LDD region. Another term should be added which describes the degradation of the gate oxide. The solution was proposed by Chan in equation (4-10). According to Chan, the hot-carrier degradation of LDD nMOSFETs at maximum substrate condition can be described by a sum of two terms. The first term, represented by $f(R_D)$ represents the degradation of the spacer oxide. The refined model of Goo can be used to describe this degradation. The second term represents the degradation of the gate oxide. The model of Hu can be used to describe this degradation. Thus, for one stress condition, the time dependence of the linear drain current degradation can be described as:

$$\frac{\Delta I_d}{I_{d0}} = \frac{C_1 t^n}{1 + C_2 t^n} + C_3 t^n \qquad (4\text{-}42)$$

This model forms a good description of the complete degradation behaviour of Technology A and technology B from 0.02 up to more than 10 %. When generalising to all the stress conditions, equation (4-42) needs to be extended to:

(*)The unit of C_1 is $\%/(s.A/m)^n$ and of C_2 $1/(s.A/m)^n$, n has no unit

$$\frac{\Delta I_d}{I_{d0}} = \frac{C_1\left(t\frac{I_d}{W}\left(\frac{I_{sub}}{I_d}\right)^{\varphi_{it}/\varphi_i}\right)^n}{1+C_2\left(t\frac{I_d}{W}\left(\frac{I_{sub}}{I_d}\right)^{\varphi_{it}/\varphi_i}\right)^n} + C_3\left(t\frac{I_d}{W}\left(\frac{I_{sub}}{I_d}\right)^{\varphi_{it}/\varphi_i}\right)^n \qquad (4\text{-}43)$$

Equation (4-43) is the new degradation model for LDD nMOSFETs under hot-carrier stress at maximum I_{sub} condition. Figure 4-22 shows that this equation describes well the degradation measurements of Technology A and B. The fit parameters are n=0.564, C_1=72.652, C_2=13.871, C_3=5.310 and φ_{it}/φ_i=3.853 for technology A and n=0.542, C_1=49.981, C_2=3.020, C_3=1.614 and φ_{it}/φ_i=2.473 for technology B.

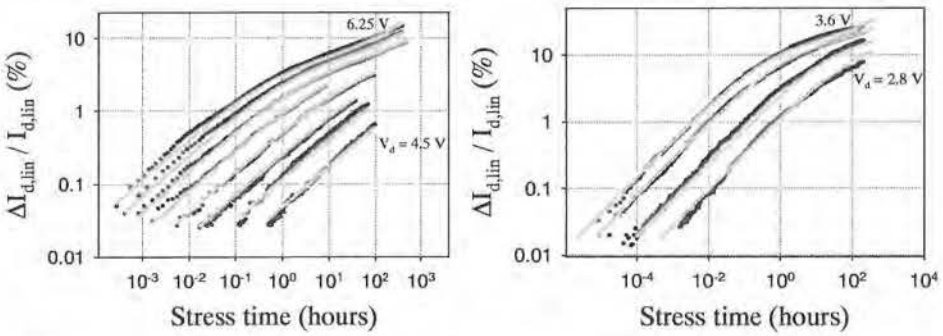

Figure 4-22: Percentage degradation of $I_{d,lin}$ as a function of stress time measured on technology A (left, dots) and technology B (right, dots); Simultaneous Least-Square Non-Linear Fit of the degradation curves at the different stress conditions with the new degradation model (lines).

4.3.3.3. Lifetime prediction of the different technologies

With the aid of the fit parameters and the measurement of I_{sub} and I_d at the different stress conditions and at the normal operating conditions, the degradation behaviour, in the full range from 0.02 up to more than 10 %, at the stress conditions and at the normal operating conditions can be calculated. This is shown in Figure 4-23 and Figure 4-24 for the three technologies A, B and C. The dots represent the degradation measurements at the different stress conditions. The lines give the calculated degradation behaviour at the different stress conditions and the dotted lines show the calculated behaviour at the normal operating conditions. The calculated lifetimes at three different failure criteria

are summarised in Table 4-8.

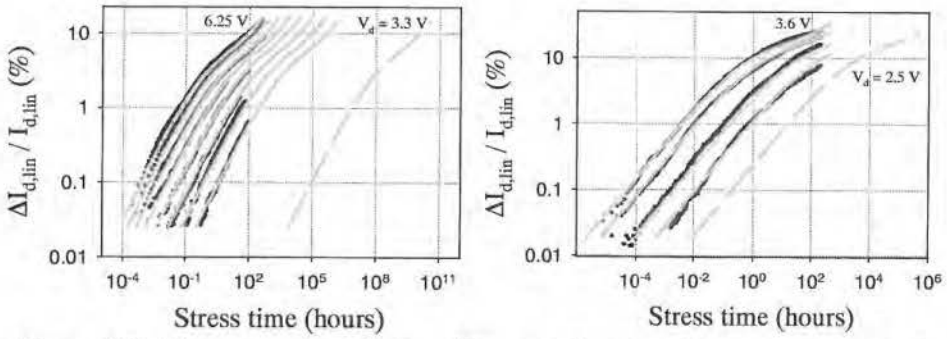

Figure 4-23: Percentage degradation of $I_{d,lin}$ as a function of stress time measured on technology A (left, dots) and technology B (right, dots); Simultaneous Least-Square Non-Linear Fit of the degradation curves at the different stress conditions (lines) and the prediction of the degradation behaviour at normal operating conditions (dotted line).

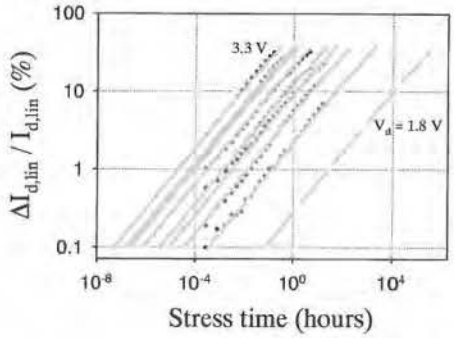

Figure 4-24: Percentage degradation of $I_{d,lin}$ as a function of stress time measured on technology C (dots); Simultaneous Least-Square Non-Linear Fit of the degradation curves at the different stress conditions (lines) and the prediction of the degradation behaviour at normal operating conditions (dotted line).

FC (%)	τ(Technology A) V_{dd}=3.3 V	τ(Technology B) V_{dd}=2.5 V	τ(Technology C) V_{dd}=1.8 V
0.1	3.80e+3 d	7.36e-3 d	3.01e-3 d
1	3.00e+5 d	0.56 d	1.14 d
10	4.64e+8 d	119.94 d	463.55 d

Table 4-8: Calculated lifetime in days of the parameter $I_{d,lin}$ for the three different technologies at the three different failure criteria

4.3.4. Summary of the lifetime prediction with the different models

Table 4-9, Table 4-10 and Table 4-11 summarises the lifetime prediction of LDD nMOSFETs with the different degradation models for Technology A, B and C respectively.

FC - Model	τ(Hu)	τ(Chan)	τ(Goo)	τ(New)
0.1 %	1511.10 d	131.40 d	5.87e+3 d	3.80e+3 d
1 %	5.87e+5 d	1.79e+6 d	4.51e+5 d	3.00e+5 d
10 %	2.28e+8 d	2.45e+10 d	x	4.64e+8 d

Table 4-9: Summary of the predicted lifetimes in days with the different degradation models for Technology A (V_{dd}=3.3 V).

FC- Model	τ(Hu)	τ(Chan)	τ(Goo)	τ(New)
0.1 %	2.16e-3 d	x	8.37e-3 d	7.36e-3 d
1 %	0.63 d	x	0.58 d	0.56 d
10 %	181.30 d	x	177.09 d	119.94 d

Table 4-10: Summary of the predicted lifetimes in days with the different degradation models for Technology B (V_{dd}=2.5 V).

FC - Model	τ(Hu)	τ(Chan)	τ(Goo)	τ(New)
0.1 %	2.63e-3 d	x	3.10e-3 d	3.01e-3 d
1 %	1.13 d	x	1.13 d	1.14 d
10 %	485.45 d	x	448.95 d	463.55 d

Table 4-11: Summary of the predicted lifetimes in days with the different degradation models for Technology C (V_{dd}=1.8 V).

From the modelling of the degradation curves with Hu, it must be remembered that this model does not describe the measurements of technology A and B well and therefore should not be used. The model of Chan and Goo can be used to model the degradation behaviour and to predict the lifetime at normal operating conditions, but they are restricted to certain degradation levels and certain technologies. The model of Chan can only be used for technology A and the model of Goo can not be used for technology A if

the FC is above 6 %. The new degradation model has no restrictions and can thus be used for all the technologies and all the different FC.

4.4. Conclusions

In this chapter, the hot-carrier degradation of LDD nMOSFETs is studied. Degradation measurements, performed on three different technologies, show that the degradation behaviour can be described by a two-stage mechanism. First, the series resistance increases and this increase saturates. Second, the mobility of the channel is reduced. This degradation behaviour can not be described by the model of Hu. Until now, no degradation model existed to perform a simultaneous least-square fit of all the degradation curves. With the aid of the model of Chan et al. [Chan95] and Goo et al. [Goo95], such a model has been developed. The new model has been used to fit the degradation behaviour and to predict the lifetime at normal operating conditions for the three different technologies.

5. Conclusions

This work deals with the study of the reliability of one specific type of electronic component, the Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET). The urge for faster and more complex circuits (more functions per chip) as well as requirements of smaller power consumption have driven this MOSFET since its invention to ever smaller dimensions. The energy of the carriers, moving horizontally along the channel from the nMOSFET in the high internal fields, increases continuously. High-energetic carriers are also called hot-carriers. These hot-carriers can gain sufficient energy to surmount the $Si\text{-}SiO_2$ potential barrier and become injected into the gate oxide. The oxide damage caused by the injected carriers leads to a deformation of the electrical characteristics of the MOSFET which has a negative influence on its function in the IC.

During the last 20 years, hot-carrier phenomena in nMOSFETs have been studied intensively. In the beginning, attention was focussed on conventional nMOSFETs, with a highly doped drain structure. Today, the degradation of these conventional nMOSFETs is quite well understood and some good models for describing the degradation behaviour and for determining the lifetime of the device at the normal operating conditions have been developed. Lightly Doped Drain (LDD) nMOSFETs introduced new degradation mechanisms that are associated with the spacer oxide above the n^- region. Although a generally accepted picture of the physical degradation mechanisms exists, a lot of work needs to be done concerning the development of a generally accepted model for these devices.

Until now, hot-carrier degradation measurements have been performed with a measurement resolution of about 0.5 %. So, the MOSFET parameter needs to drift more than 0.5 % in order to be detectable. Consequently, the degradation behaviour at small stress times and at small degradation levels can not be studied with commercial available test systems. Because a relatively high degradation level is required, the stress conditions need to be much higher than the operating conditions. These high stress conditions can generate degradation mechanisms which do not occur at the normal operating conditions.

This work contains three main parts. In the first part (chapter 2), a high-resolution measurement technique (HRMT) is proposed to perform hot-carrier degradation measurements on packaged or wafer-level nMOSFETs. In the last two parts (chapter 3

and 4), this HRMT is tested on different wafer technologies.

In the HRMT, the degradation parameters are extracted from the MOSFET I-V characteristics. In order to determine a parameter, the I-V characteristic is not measured completely but only a dense measurement in a restricted region around the desired parameter is performed with highly accurate measurement equipment. To obtain a high measurement resolution, the temperature needs to be controlled. First, the measurement procedure is developed in order to minimise the time that a current flows through the channel and thus the time that the gate voltage is on. Then, there are two ways to control the temperature:

- Correction of the degradation measurement for the room temperature fluctuations. This is done in two steps: first the determination of the TC from a characterisation measurement and then the correction of the degradation measurement for the temperature fluctuations with this TC.
- Stabilisation of the temperature in the DUT-environment.

In this work, the second method is used. Therefore, the DUT will be placed in a protective chamber and the temperature in this chamber will be stabilised at 29.6 °C with a stability of 0.03 °C. With this HRMT, the calculated resolution of 0.5 % for the "classical" method can be improved down to less than 200 ppm.

In chapter 3, the hot-carrier degradation of conventional nMOSFETs is studied with the HRMT. The degradation mechanisms, as they are described in the literature, were discussed and measurements on a 2.4 μm technology were performed. The models of Hu and Takeda were discussed and the model of Takeda has been extracted from the model of Hu by using two approximations. The model of Hu and Takeda have been fitted on the degradation measurements by using the least-square estimation. It has been shown that a more correct lifetime model of Takeda is obtained when $V_{d,sat}$ is not neglected in comparison to V_d (first approximation). Instead of fitting each degradation curve separately and using a lifetime plot to predict the lifetime at normal operating conditions, it is proposed to perform a simultaneous least-square linear fit on all the degradation curves. The chapter ends with an investigation of the advantages of the HRMT on three different subjects: physical degradation mechanisms, lifetime prediction and test time reduction. It is concluded that only one degradation mechanism is active in the full degradation area (from 0.02 up to more than 10%), that the lifetime prediction can not be significantly improved by using the HRMT and that the test times can be seriously reduced because the measurements can be stopped earlier.

In the last chapter, the hot-carrier degradation of LDD nMOSFETs is studied. Degradation measurements, performed on three different technologies, show that the degradation behaviour can be described by a two-stage mechanism. First, the series resistance increases and this increase saturates. Second, the mobility of the channel is reduced. This degradation behaviour can not be described by the model of Hu. Until now, no degradation model existed to perform a simultaneous least-square fit of all the degradation curves. With the aid of the model of Chan et al. [Chan95] and Goo et al. [Goo95], such a model has been developed. The new model has been used to fit the degradation behaviour and to predict the lifetime at normal operating conditions of the three different technologies.

Publication list

Regular journals

R. Dreesen, W. De Ceuninck, L. De Schepper, G. Groeseneken, "A high resolution method for measuring hot carrier degradation in matched transistor pairs", Microelectron. Reliab., Vol. 37, No. 10/11, pp. 1533-1536, 1997.

Dreesen R., Croes K., Manca J., De Ceuninck W., De Schepper L., Pergoot A. and Groeseneken G., "Modeling hot-carrier degradation of LDD NMOSFETs by using a high-resolution measurement technique", Microelectron. Reliab., Vol. 39, pp. 785-790, 1999.

Conference papers

R. Dreesen, W. De Ceuninck, L. De Schepper, G. Groeseneken, "A high resolution method for measuring hot carrier degradation in matched transistor pairs", Proceedings of the 8th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis., pp. 1533-1536, 1997.

Dreesen R., Croes K., Manca J., De Ceuninck W., De Schepper L., Pergoot A., Groeseneken G., "A New Lifetime Extrapolation Technique for LDD NMOSFETS under Hot-Carrier Degradation", Proceedings of the 29th European Solid-State Device Research Conference, pp. 584-587, 1999.

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Submitted

Dreesen R., Croes K., Manca J., De Ceuninck W., De Schepper L., Pergoot A. and Groeseneken G., "A new degradation model and lifetime extrapolation technique for LDD nMOSFETs under hot-carrier degradation.", submitted for publication to Microelectron. Reliab.

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Appendix A: Build-in safeties

Performing high-resolution measurements on nMOSFETs is not straight forward. During this work, the total testbench has to be protected from environmental influences. During the development of the new measurement methodology certain inabilities of the measurement equipment have been detected. These inabilities, and the build-in safeties to eliminate them are described in this appendix.

A.1 The Keithley 6517 current meter

Figure A.1 shows the I_d-V_g characteristic of an n-MOSFET on wafer, measured at the source in autoscale.

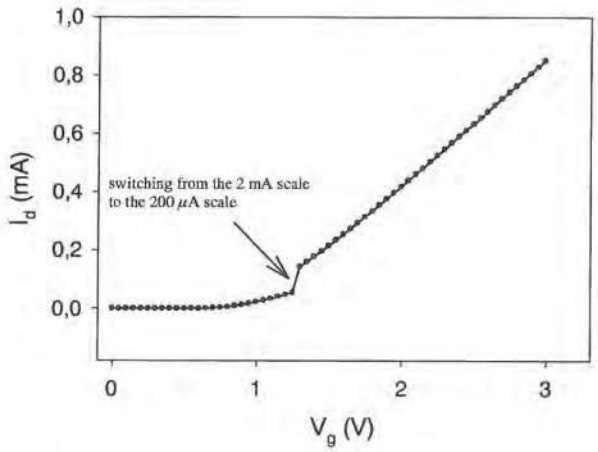

Figure A.1: I_d-V_g characteristic of an n-MOSFET on wafer, measured at the source in autoscale

Two different problems occur. First, when switching from the 2 mA scale to the 200 μA scale, a sudden shift of the I_d-V_g characteristic is observed. This shift can be explained by the burden voltage of the Keithley 6517. The burden voltage is the voltage loss over the terminals of the Keithley. Because this burden voltage is different in the different scales of the current meter, the applied V_g (which is the voltage from gate to source) is different in the two scales and this can have a large influence on the measured current

The second problem is illustrated in Figure A.2. Once measurements are done in the 200 μA scale, certain oscillations occur which disturb the measurement of the I_d-V_g

characteristic. Figure A.2 shows the burden voltage over the terminals of the Keithley 6517 when measuring the characteristic of Figure A.1. When switching from the 2 mA scale to the 200 μA scale, the voltage over the terminals of the Keithley increases suddenly.

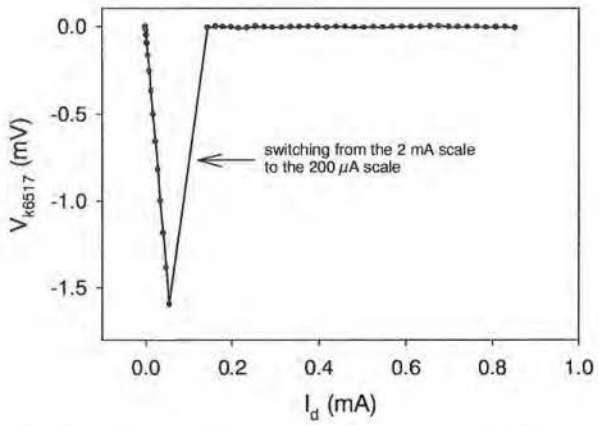

Figure A.2: Burden voltage over the terminals of the Keithley 6517 when measuring the characteristic of Figure A.1.

To solve this problem, the channel current should be measured at the drain instead of the source. Figure A.3 and Figure A.4 indicate that the problem is solved.

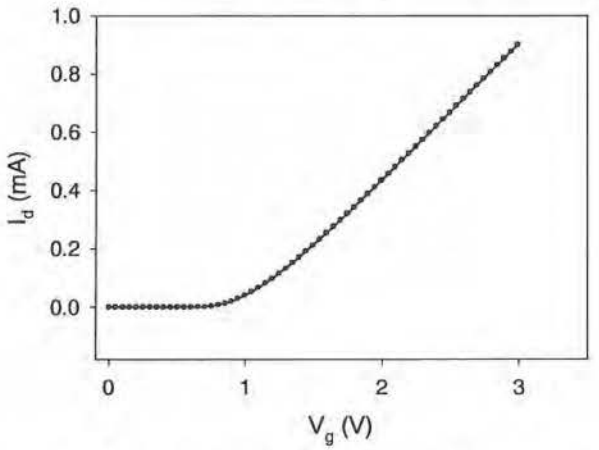

Figure A.3: I_d-V_g characteristic of an n-MOSFET on wafer, measured at the drain in autoscale

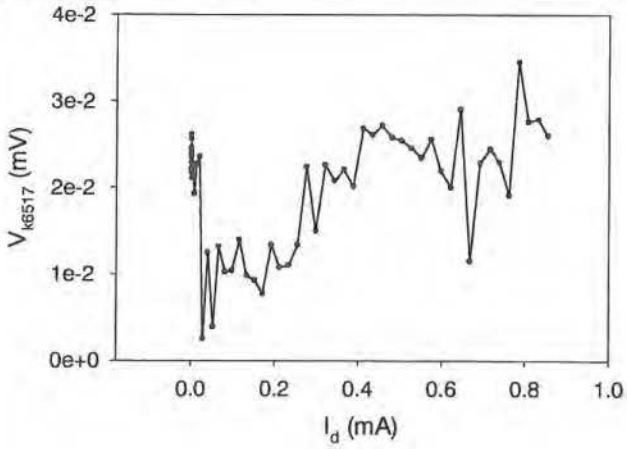

Figure A.4: Burden voltage over the terminals of the Keithley 6517 when measuring the characteristic of Figure A.3.

Figure A.3 shows the I_d-V_g characteristic of an n-MOSFET on wafer, measured at the drain in autoscale. The shift in this characteristic, illustrated in Figure A.1, has now disappeared. Figure A.4 shows the burden voltage over the terminals of the Keithley 6517 when measuring the characteristic of Figure A.3. The oscillations, shown in Figure A.2, are also disappeared.

Another problem with the Keithley 6517 is that an overflow is measured when the current meter is switched to the lowest scale (20 pA). Figure A.5 gives a schematic overview of this problem. Figure A.5 (a) shows the Keithley configuration of the traditional measurement equipment. It can be observed that the plus terminal of the current meter is connected to the voltage source at the drain and the minus terminal is connected to the drain of the sample. With this configuration, two problems occur:

- Because there is always a small leakage path from the minus terminal to the earth, the measured current will consist of two parts: first the measurement of the current I_R through the sample and second the leakage current I_L to the earth. This leakage current can be in the order of 10 nA so it is impossible to perform measurements in the 20 pA range.
- The high-impedant drain is connected to the shield of the coax cable. This way, extern fields can cause all kinds of problems.

The solution for this problem is the following: change the plus by the minus terminal of the Keithley and vice versa. Figure A.5 (b) shows this new configuration. The leakage

current will now flow from the minus terminal to the earth without passing through the current meter so this current is not measured. Also, the high-impedant drain is protected from the environment.

Finally, the DUT is protected when the Keithley switches from one range to another. This is done because the current meter can generate voltage spikes when switching from range.

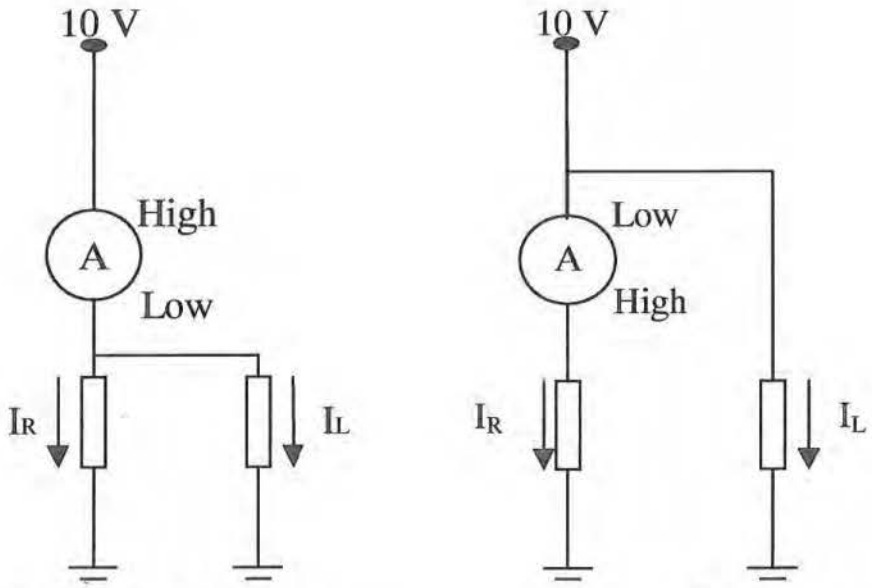

Figure A.5: a)Incorrect configuration *b) Correct configuration*

Conclusion: The main build-in safeties for the Keithley 6517 current meter are:

- *The channel current is measured at the drain instead of the source.*
- *The minus terminal of the current meter is connected to the voltage source and the plus terminal is connected to the high-impedant drain.*
- *A shortcut is placed over the Keithley when it switches from one range to another.*

A.2 The HP 3245 voltage source

When measuring degradation parameters, the HP3245 voltage source at the gate is put

into a DC memory mode and all the desired gate voltages are stored in the memory of the voltage source. When applying a certain stress, on the other hand, a constant gate voltage is applied for a period of time. For applying this voltage, the voltage source is put into the DC voltage mode.

Figure A.6 shows the behaviour of the voltage source when switching from DC memory mode to DC voltage mode. A peak to peak voltage of almost 20 V appears at the gate for a short time period and this can seriously damage the device.

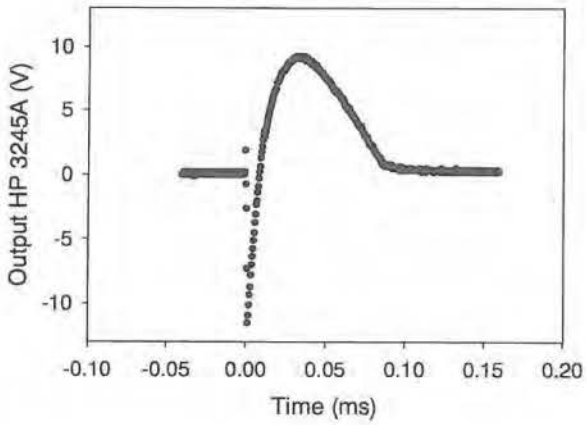

Figure A.6: Behaviour of the HP3245 voltage source when switching from DC memory mode to DC voltage mode

The solution for this problem is the following: when switching from DC memory mode to DCV mode, first shortcut the gate, then take the voltage source out of the circuit and first switch to 0 V DC, before applying a voltage different from 0.

Conclusion: the build-in safeties for the HP 3245 voltage source are a number of protective steps before the switching from DC memory mode to DC voltage mode.

1. *Shortcut the gate*
2. *Take the voltage source out of the circuit*
3. *Set the DC voltage first to 0 V*
4. *Open the shortcut*
5. Set the DC voltage to the desired value

Appendix B: The parameter $g_{m,max}$

During this work, $I_{d,lin}$ was not the only parameter which has been measured. Also $g_{m,max}$ has been studied intensively and the results are summarised in this appendix. Although most of the models are developed for the parameter $I_{d,lin}$, they will now be used to model the parameter $g_{m,max}$.

The degradation curves of $g_{m,max}$ are shown in Figure B.1 for technology A and C respectively.

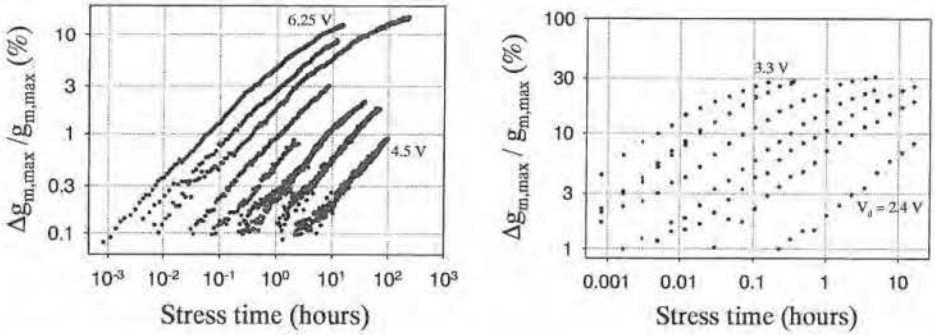

Figure B.1: Percentage degradation of $g_{m,max}$ as a function of stress time of technology A (left) and of technology C (right).

As in chapter 4, the measurements will be first modelled with Hu et al. [Hu 85]. Figure B.2 again shows the measurement of $g_{m,max}$ for the two technologies A and C. The lines show the simultaneous least-square linear fit of the degradation curves, together with the predicted behaviour at normal operating conditions. The estimated fit parameters of the simultaneous least-square linear fit with the model of Hu for the two technologies are given in Table B.1. The calculated lifetime of the parameter $g_{m,max}$ for the two technologies at three different failure criteria is shown in Table B.2.

The same conclusion as in chapter 4 can be taken from this modelling: although a lifetime prediction can be done, it is clear from Figure B.2 that the model of Hu can not be used to describe the degradation of $g_{m,max}$ properly. The degradation can not be described by a straight line on a logarithmic scale as is assumed by Hu's model. Another model is needed.

In a next step, the degradation measurements will be modelled with Goo et al. [Goo 95].

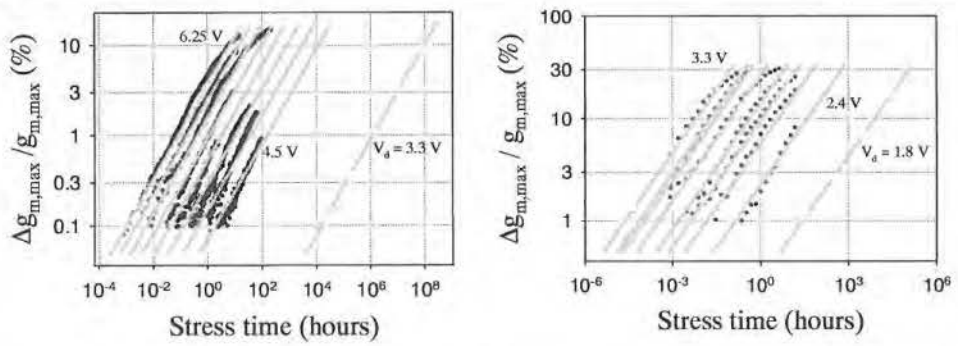

Figure B.2: Percentage degradation of $g_{m,max}$ as a function of stress time of technology A (left, dots) and technology C (right, dots); Simultaneous Least-Square Linear Fit of the degradation curves at the different stress conditions with the model of Hu (lines); Predicted degradation behaviour at normal operating conditions (dotted line).

Fit parameters	Technology A	Technology C
C	22.606	273.990
n	0.527	0.410
φ_{it}/φ_i	3.380	2.820

Table B.1: Estimated fit parameters of the simultaneous least-square linear fit with the model of Hu for two technologies.

FC (%)	τ(Technology A)	τ(Technology C)
0.1	635.10 d	4.07e-3 d
1	5.03e+4 d	1.15 d
10	3.98e+6 d	326.63 d

Table B.2: Calculated lifetime in days of the parameter $g_{m,max}$ for two technologies at the three different failure criteria.

The results of the application of the model of Goo is shown in Figure B.3 and B.4. In the left part of Figure B.3, the dots represent the degradation of $g_{m,max}$, measured on

Technology A, versus the normalised stress time. The normalised stress time is again the product of stress time and a normalised weighting factor as to be 1 for 4.75 V stress. The line represents the least-square non-linear fit of the universal curve. All stress conditions are included in the fit.

The estimated fit parameters are shown in the second column of Table B.3. Because the saturation level is not reached during this measurement, no deviation occurs between the measurement and the fit and thus can be concluded that the model of Goo is a good model to describe these measurements.

Although it is mathematically rather unfounded, a good lifetime prediction method is provided with the model of Goo. This is shown in the right part of Figure B.3. In this figure, a Hu plot is shown for three different failure criteria. Goo did not prove that a Hu plot can be used, but as can be clearly seen in this figure, the different points fall on a straight line. The calculated lifetimes at three different failure criteria are given in the second column of Table B.4.

The model of Goo is also applied on the measurement of $g_{m,max}$ of technology C. The result is shown in Figure B.4. The estimated fit parameters are shown in the last column of Table B.3 and the calculated lifetimes at three different failure criteria are shown in the last column of Table B.4.

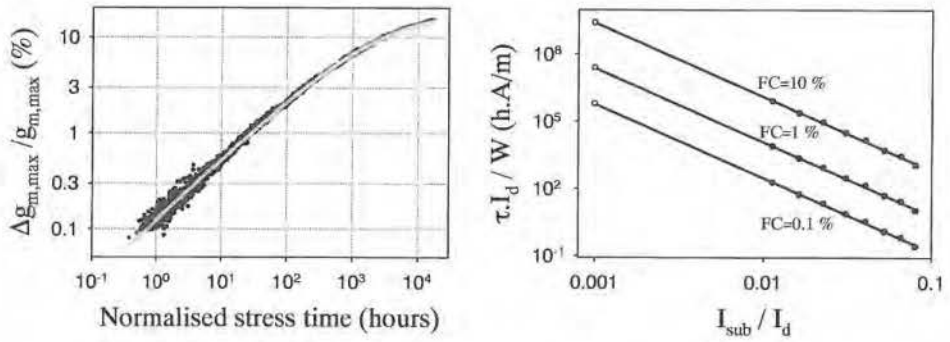

Figure B.3: Degradation of $g_{m,max}$, measured on technology A, versus normalised stress time (left, dots); Least-square non-linear fit of the degradation curves with the model of Goo (left, line); Hu plot for three different failure criteria (right).

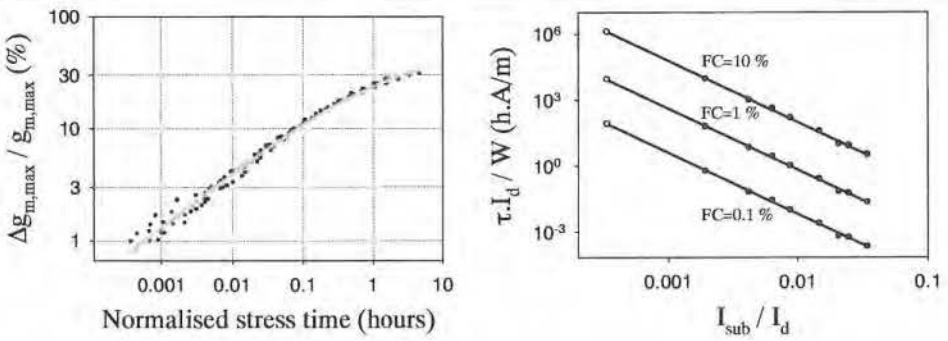

Figure B.4: Degradation of $g_{m,max}$, measured on technology C, versus normalised stress time (left, dots); Least-square non-linear fit of the degradation curves with the model of Goo (left, line); Hu plot for three different failure criteria (right).

Fit parameters	Technology A	Technology C
C_1	0.125	42.342
C_2	0.00644	0.788
n	0.636	0.499

Table B.3: Estimated fit parameters of the simultaneous least-square linear fit with the model of Goo for the two technologies.

FC (%)	τ(Technology A)	τ(Technology C)
0.1	824.90 d	1.47e-2 d
1	3.32e+4 d	1.53 d
10	3.54e+6 d	222.65 d

Table B.4: Calculated lifetime in days of the parameter $g_{m,max}$ for the two technologies at three different failure criteria.

Finally, the degradation of $g_{m,max}$ will be modelled with the refined model of Goo. The result of the simultaneous least-square non-linear fit is shown in Figure B.5 for technology A and C. The estimated fit coefficients are given in Table B.5.

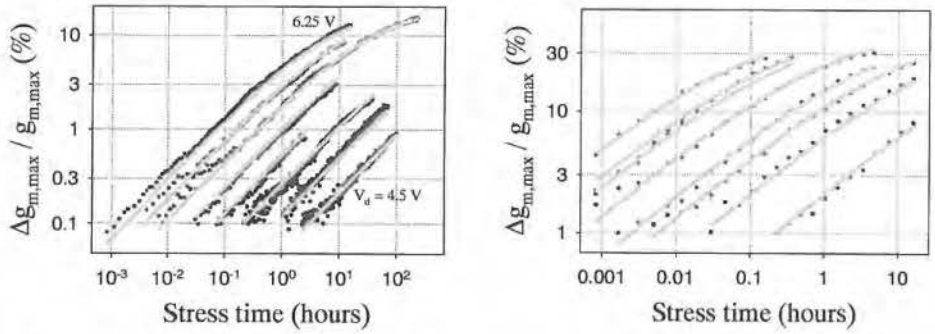

Figure B.5: Percentage degradation of $g_{m,max}$ as a function of stress time measured on technology A (left, dots) and on technology C (right, dots); Simultaneous Least-Square Non-Linear Fit of the degradation curves at the different stress conditions with the refined model of Goo (lines).

Fit parameters	Technology A	Technology C
C_1	0.259	855.587
C_2	0.0126	17.152
n	0.627	0.506
φ_{it}/φ_i	3.344	2.814

Table B.5: Estimated fit parameters of the simultaneous least-square linear fit with the refined model of Goo for the three different technologies.

With the aid of the fit parameters and the measurement of I_{sub} and I_d at the different stress conditions and at the normal operating conditions, the degradation behaviour, in the full range from 0.02 up to more than 10 %, at the stress conditions and at the normal operating conditions can be calculated. This is shown in Figure B.6 for technology A and C. The dots represent the degradation measurements at the different stress conditions. The lines give the calculated degradation behaviour at the different stress conditions and the dotted line shows the predicted degradation behaviour at the normal operating conditions. The calculated lifetimes at three different failure criteria are summarised in Table B.6.

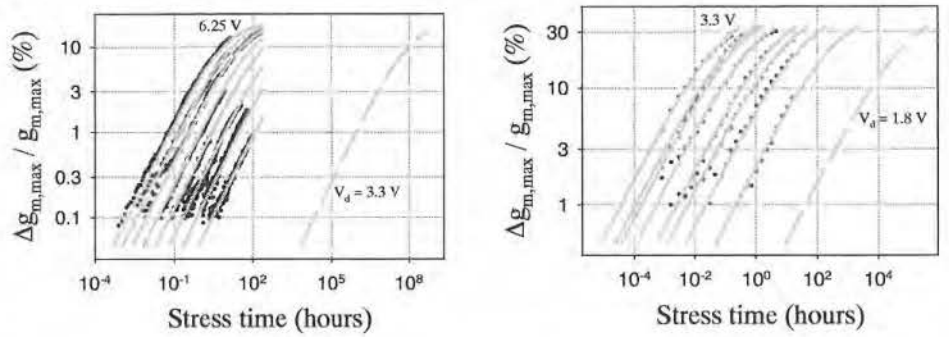

Figure B.6: Percentage degradation of $I_{d,lin}$ as a function of stress time measured on technology A (left, dots) and on technology C (right, dots); Simultaneous Least-Square Non-Linear Fit of the degradation curves at the different stress conditions (lines) and the prediction of the degradation behaviour at normal operating conditions (dotted lines).

FC (%)	τ(Technology A)	τ(Technology C)
0.1	4.49e+3 d	1.81e-2 d
1	1.90e+5 d	1.77 d
10	2.00e+7 d	251.85 d

Table B.6: Calculated lifetime in days of the parameter $g_{m,max}$ for the two technologies at three different failure criteria

Table B.7 and B.8 summarises the lifetime prediction of $g_{m,max}$ with the different degradation models for Technology A and C respectively.

FC - Model	τ(Hu)	τ(Goo)	τ(New) years
0.1 %	635.10 d	824.90 d	4.49e+3 d
1 %	5.03e+4 d	3.32e+4 d	1.90e+5 d
10 %	3.98e+6 d	3.54e+6 d	2.00e+7 d

Table B.7: Summary of the predicted lifetimes in days with the different degradation models for Technology A.

FC - Model	τ(Hu)	τ(Goo)	τ(New)
0.1 %	4.07e-3 d	1.47e-2 d	1.81e-2 d
1 %	1.15 d	1.53 d	1.77 d
10 %	332.15 d	222.65 d	251.85 d

Table B.8: Summary of the predicted lifetimes with the different degradation models for Technology C.