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Study of the behaviour of oxide related degradation mechanisms of smart power based transistors

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Nederlandse samenvatting

In vele “smart-power”-toepassingen moeten grote drainspanningen en grote stromen gecombineerd kunnen worden met standaard lage spanning-CMOS logische cellen. In de voorbije jaren is de keuze gevallen op laterale DMOS-transistors. In tegenstelling tot standaard CMOS-transistors vertonen hoge spanning-MOS-transistors een elektrisch veld en een ladingsdrager-temperatuurs distributie die een complexe functie zijn van V_{ds} en V_{gs}, het ontwerpproces en de lay-out parameters. Als gevolg hiervan zijn de fysische degradatiemechanismen in laterale DMOS-transistoren niet volledig begrepen. De modellering van de transistordegradatie te wijten aan hot-carrier-gevolgen is een vertaling van het begrip van de fysische mechanismen die tot degradatie van de transistorparameters leiden. Als de degradatiemechanismen niet volledig worden begrepen, zal een empirische beschrijving moeten voldoen. Het fysische begrip van degradatie in MOS-structuren, toe te schrijven aan hoog energetische ladingsdragers die dicht aan het silicium lopen, is dat, onder andere, interface-toestanden gegenereerd worden waarin de dragers die transistorparameters beïnvloeden kunnen worden opgesloten. Deze parameters kunnen zijn: kanaalmobiliteit, drempel spanning, de drain serieweerstand, saturatie spanning/stroom, enz.

De “hot-carrier” stress experimenten werden uitgevoerd op verpakte teststructuren in een speciaal ontworpen ovensysteem bij kamertemperatuur met een stabiliteit van 0.03 °C. Bij hoge gatespanning neemt de lineaire drainstroom af met de tijd en verzadigt. De saturatie drainstroom daarentegen vertoont een veel grotere drift, die zich ook weerspiegelt in een grote shift van de drempelspanning in de grootte-orde van 1 à 2V. Voor $I_{d,sat}$ en V_t wordt bovendien een grote statistische spreiding waargenomen. Uit experimenten blijkt dat er minstens drie verschillende degradatiemechanismen voorkomen in de LDMOS-transistor. De lineaire drainstroom degradatie, welke het gevoeligst is voor schade in het driftgebied, toont de exponentiële afhankelijkheid van de drainspanning zoals verwacht voor het normale “hot-carrier”-degradatie mechanisme (“Channel Mobility Reduction”). Anderzijds vertonen $I_{d,sat}$ en V_t een zeer hoge drift, relatief ongevoelig voor de drainspanning (“Source Side Injection”) . De verschuiving in V_t wordt daarentegen duidelijk bepaald door de gatespanning en het vertikaal elektrisch veld, wat typisch is voor een SSI-mechanisme. Bij lage gatespanning kan een initiële verhoging van de lineaire drainstroom waargenomen worden die veroorzaakt wordt door een derde degradatiemechanisme (“Hot Hole Injection”). In de laatste jaren zijn

verschillende modellen ontwikkeld om “hot-carrier”-degradatie op standaard veld-effect transistors te beschrijven. Er zal een overzicht van de meest gebruikte modellen gegeven worden en hieruit zal het meest geschikte model aangepast en gebruikt worden om het gedrag van laterale DMOS-transistors te beschrijven. Gedetailleerde TCAD simulaties, die het voorgestelde model ondersteunen, zullen uitgevoerd worden.

In het voorgestelde werk zal ook de hoge resolutie state-of-the-art TDDB-techniek worden ontwikkeld om kleine lekstromen te kunnen meten. Tijdens de laatste jaren is aangetoond dat, met het ononderbroken downscalen van de transistors, de “charge to breakdown” geen correcte betrouwbaarheidsvoorspelling voor uiterst dunne oxides kan geven. Slechts als de “charge to breakdown” gemeten wordt bij constante stress-spanning (Constant Voltage Stress) worden consistente betrouwbaarheidsgegevens verkregen. De nieuwe methode is gebaseerd op het meten van de “Stress Induced Leakage Current (SILC)” die de diëlektrische breakdown tijdens stress voorafgaat. Zoals reeds besproken, is TDDB zeer belangrijk in dunne oxides, afhankelijk van de verschillende toepassingen. De dikte van de oxidelaag is in recente CMOS-technologieën tot slechts een paar nanometers verminderd en de dunne CMOS-gate wordt ook binnen de DMOS-transistoren gebruikt. Anderzijds wordt de lekstroom door de gate zeer belangrijk bij vele toepassingen zoals geïntegreerde analoge capaciteiten en floating-gate niet-vluchtig geheugen. Elke ladingsoverdracht van/naar de floating-gate beïnvloedt de geheugentoestand. Mechanismen zoals SILC kunnen de essentieelste eigenschap van een niet-vluchtig geheugen beïnvloeden. Het is daarom zeer belangrijk om de betrouwbaarheid van het oxide op een nauwkeurige en correcte manier te voorspellen. Verscheidene modellen zijn voorgesteld om de fysische oorsprong van de karakteristieke veldafhankelijkheid van SILC te verklaren. Het model van Nigam beschrijft de verandering in de stroomdichtheid als functie van tijd:

$$\Delta J = N^{+}\left(V_g\right)\left[1 - e^{-t/\tau_{tr}}\right] + \alpha.t^{\nu} \qquad (1)$$

met ΔJ de verandering in stroomdichtheid, t de tijd, $N^{+}(V_g)$ de saturatiewaarde van positieve ladingstrapping, τ_{tr} de trapping tijdsconstante en α en ν de SILC gerelateerde parameters. De eerste term in de vergelijking beschrijft een exponentiële saturatietrapping van positieve lading, terwijl de tweede term de verhoging toe te schrijven aan SILC-generatie beschrijft. De state-of-the-art meettechniek verbetert duidelijk de resolutie van de SILC-meting zoals die nog nooit voor dergelijke lage lekstromen werd verkregen. Deze meetresultaten echter leiden tot een initiële

moeilijkheid om het model van Nigam toe te passen op de gemeten data en de bepaling van de initiële stroomdichtheidswaarde (J_0) in het bijzonder wordt zeer belangrijk. Diverse numerieke methodes zijn gebruikt om de waarde van J_0 te extrapoleren uit de meetdata. Geen van deze methodes is echter nauwkeurig genoeg. Om deze reden wordt een nieuwe fitprocedure gebaseerd op de onafhankelijke bepaling van τ_{tr} voorgesteld. De nieuwe procedure laat toe om een zeer nauwkeurige fitting van de data en bepaling van de modelparameters te doen.

List of symbols and abbreviations

α	leakage current caused by the traps generated after 1 sec
χ	statistical variable
ε	error for a generic measurement
ϕ_B	Barrier height at the cathode / oxide interface (eV)
φ_i	impact ionization energy (eV)
φ_{it}	energy for interface trap generation (eV)
λ	Lagrange multiplier
μ_n	electron mobility (cm^2/V-sec)
ν	trap generation rate (cm/sec)
ν_{th}	charge carrier thermal velocity (cm/sec)
τ	lifetime (sec)
τ_{tr}	trapping time (sec)
AHI	Anode Hole Injection
BBI	Burn-In Board
C_{ox}	gate oxide capacitance (F)
CVS	Constant Voltage Stress (V)
CCS	Constant Current Stress (A)
CP	Charge trapping
CHMR	Channel Mobility Reduction
CAT	Charge Assisted Tunneling
CMOS	Complementary Metal Oxide Semiconductor
DT	Direct tunneling

DMM	Digital multimeter
DUT	Device Under Test
DMOS	Double diffused Metal Oxide Semiconductor
E_{gain}	Energy gained by the incoming electrons (eV)
E_L	lateral electric field (V/cm)
EVBT	Elastic Valence Band Tunneling
EEPROM	Electrically Erasable Programmable Read-Only Memory
ESD	electrostatic discharge
EPROM	Erasable Programmable Read-Only Memory
f	frequency (Hz)
F	unknown degradation model
FC	failure criterion
FNT	Fowler Nordheim Tunneling
$g_{m,max}$	maximum transconductance (A/V)
HR	Hydrogen Release
HR-S-MT	High Resolution SILC Measurement Technique
HHI	Hot Hole Injection
HCI	Hot Carrier Interface
HC	Hot Carrier Injection
IMO	Instituut voor Materiaalonderzoek / Institute for Materials Research, Diepenbeek, Belgium
ICBT	Inelastic Conduction Band Tunneling
I_d	drain to source current (A)
$I_{d,lin}$	linear drain current (A)
$I_{d,sat}$	saturation drain current (A)

I_{sub}	substrate current (A)
IC	Integrate Circuit
J_{SILC}	SILC current density (A/cm^2)
J_{meas}	total current density measured (A/cm^2)
J_{DT}	direct tunneling current density (A/cm^2)
$J_{Leak}(0)$	leakage current density due to traps already present (A/cm^2)
J_0	current density at time 0 (A/cm^2)
J_i	generic measurement (A/cm^2)
J_i^{exp}	generic measurement known experimentally (A/cm^2)
J_{stress}	current density stress (A/cm^2)
L	channel length (μm)
LDD	Lightly Doped Drain
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOS	Metal-silicon Oxide-Silicon
N^+	saturation value of the positive charge trapping (A/cm^2)
N	number of measured points
n_h	density of holes (cm^{-3})
n_{max}	total number of defect precursors
n	number of precursors transformed in defects
n_{min}	number of defects already present
$N_{A,max}$	maximum doping concentration (cm^{-3})
NVM	Non-Volatile Memory
ppm	parts per million
PPS	Pulse Power Supply
P	property

PIC	Power Integrated Circuit
PF	Poole-Frenkel mechanism
P/E	programming / erase
Q_{it}	interface trapped charge (charges/cm^2)
Q_f	fixed oxide charge (charges/cm^2)
Q_{ot}	oxide trapped charge (charges/cm^2)
Q_m	mobile ionic charge (charges/cm^2)
R_{on}	on-resistance ($m\Omega*mm^2$)
R_{ch}	channel resistance (Ω)
R_{eq}	equivalent resistance (Ω)
R_{conv}	Resistance of the current / voltage converter (Ω)
Si	silicon
SHHI	Substrate Hot Hole Injection
SiO_2	oxide silicon
S_I	first arbitrary auxiliary function
SSI	Source Side Injection
S_{II}	second arbitrary auxiliary function
SILC	Stress Induced Leakage Current
T	temperature (°C)
Time	stress time (sec)
TAT	Trap Assisted Tunneling
T_{ox}	gate oxide thickness (nm)
TC	temperature coefficient (ppm/°C)
V_{gs}	gate-source voltage (V)
V_{ds}	drain-source voltage (V)

V_{bd}	voltage breakdown (V)
V_d	applied drain voltage (V)
V_g	applied gate voltage (V)
VLSI	Very Large Scale Integration
V_t	Threshold voltage (V)
V_{ref}	Reference voltage (V)
W_{eff}	effective channel width (μm)
W	channel width (μm)

1. General introduction

1.1. Introduction

Electronic devices are made of active circuit elements such as transistors, and passive elements such as resistors and capacitors. Before the advent of microelectronic technology, these basic functional units were manufactured separately and wired together with metal conductors to form electronic devices. Microelectronic technology has not, for the most part, changed the nature of these basic functional units. Rather, it has made these electronic functions more reproducible, more reliable, and less expensive by fabricating miniaturized versions of them on a single semiconducting substrate of silicon or gallium arsenide. As a result, a growing number of logic circuits have been implemented using the basic circuit elements that are most easily fabricated in silicon [Meindl77]. In microelectronics, the area of silicon the component occupies, measures its main cost. It's difficult, though, to shrink passive components like resistors, capacitors, and inductors. Although improvements in technology will lead to an increased selection of miniaturized passive components, simple -replacement- of passive components by active transistors has proven to be a far more effective strategy. So, over the past two decades, research in microelectronic technology has focused on producing miniaturized high-quality transistors. This trend is reflected in the evolution of digital logic circuits toward a state where transistors are now used for almost all functions. The fundamental units of electronic logic are logic gates, and at the heart of every gate is at least one active circuit element. Discrete bipolar transistors and integrated circuits were first produced using bipolar technologies. MOS technologies, employing MOS transistors, were developed later than bipolar ones, and for the most part have been built only in microelectronic form. The evolution of bipolar and MOS technologies reflect advances in processing technology. MOS technologies offer a reduction in the large space and high power consumption requirements of bipolar devices. The first MOS electronic circuits employed p-channel devices because they were the easiest to make. As MOS technology advanced, n-channel devices replaced p-channel devices because they offered higher speed performance for the same density, complexity, and cost. The need for reduced power consumption led to the development of the larger but more power efficient complementary MOS (CMOS). Three important measures of manufacturing efficiency are yield, cycle time and fabrication cost. The costs of the last two stages, chip assembly

and final testing, are often higher than wafer fabrication and testing because manufacturing costs are not shared among many dies. Each die must be separately packaged and tested. The evolution of IC technology illustrates the constant interaction between technology and economics, resulting in more reproducible, more reliable, and less expensive devices. Advances in IC technology are driven mainly by economic desires for high yield and cycle time, mass fabrication at low cost, and shares in high-volume electronics markets. Competition in international markets is high. In the past 30 years, chip packages have remained fairly constant in size and price (about $5 per chip), but the number of transistors per chip have increased by six orders of magnitude, doubling every year or two, to the point where today a typical chip contains 10^6 transistors. The most striking characteristic that separates the IC industry from other industries is in its annual doubling of output. This rapid growth has resulted in a greater rate of price reduction than in other industries. Yield is the percentage of good circuits that survive the manufacturing process to emerge as packaged chips. Twenty years ago, IC chip yields were at 20%, which left enormous leverage for profit potential. In the 1980's, a large percentage of the chip market share was taken over by Japanese IC manufacturers, who concentrated on yield. As fabrication technology matured, yields increased to the point where commercial yields for simple circuits are presently at a stable 75-80% at competitive IC manufacturing firms. Yield typically decreases with increasing circuit size and integration because bigger circuits have a higher probability of having a defect and because fewer die can fit on a single wafer. Thus, typical commercial yields currently vary from as low as 30% to as high as 80%, depending on the complexity of the circuit, the maturity of the process, and the efficiency of the fab [Meindl77].

Four emerging markets show potential for high growth and strong influence in determining future technologies used in several major products. These markets are consumer electronics, broadband communications, advanced display systems, and intelligent vehicles and highway systems. The last market refers to new technologies that will greatly increase highway and automobile efficiency and safety. Automotive application will require microprocessors, signal processors, and memories embedded in automotive controls and communications systems, as well as IC components for satellite receivers, sensors, radar-based collision-avoidance systems, and distributed highway control systems. These next-generation products will require new chips. Any IC manufacturer will have a leading position as long as it remains competitive by contributing to the advancement of chip design, packaging, software, and manufacturing technologies [Kassakian01].

1.2. Motivation of this work

The extension of existing smart power technologies towards higher current/power handling capabilities is a challenging and demanding task, subject of state-of-the art research in many companies (e.g. Philips. Toshiba, Motorola…). For applications requiring real power capabilities (>100 W), power transistors need to be made as discrete components, i.e. only one transistor per chip is available. The driving circuit of the power transistor is to be done on a separate chip, leading to expensive multi-chip solutions. However, there is also an increased interest from the market for so-called *Power Integrated Circuits (PIC)*, which integrates power handling capabilities and digital logic on the same chip [Kassakian01]. One of the strong motivations for research in this field is the large market segment for motor drivers, where these technologies are used to drive motors in an H-bridge configuration. The main features of the switches used in H-bridge drivers are current levels between 5 and 10A, reverse blocking voltage up to 80V for the upcoming 42V automotive battery and low on-resistance in forward conduction mode. The on-resistance needs to be as low as possible as it directly determines the power loss in the switch. Besides a low value of Ron, its temperature coefficient must be as low as possible in order to be effective for high temperature operation [Moens01].

For many smart-power applications, lateral DMOS transistors are used to implement devices with high drain voltages and high current levels. These devices are relatively easy to implement, but have the disadvantage of having a relatively high Ron. A first attempt in the reduction of the Ron came with the discovery of the reduced surface field. A more recent step in the Ron reduction came with the introduction of the super junction devices. However, super junction devices using the well-known multi-epitaxial approach are only feasible for devices with sufficiently high breakdown voltage (V_{bd} > 200V).

Understand the degradation mechanisms and model the ageing behavior of these novel devices will be fundamental in the reliability analysis of smart power technologies. This may give a tool and a model to the circuit designer to optimize together silicon area while still guaranteeing the reliability of the circuit. Competition demands that the maximum power handling is performed in the smallest silicon area. Multi-chip modules integrating different chips for different functions still suffer the drawback of long-term reliability issues, although substantial progress has been made in these fields. Therefore, the current trend is to increase the integration of all kind of functions (digital, analog, sensors, memory, drivers…) on one single chip. However, specific problems arise such as excessive self-heating due to the high power densities (up to 1MW/cm^2) and accelerated

hot carrier degradation of the transistors upon operation. Among other degradation mechanism, hot carrier injection is still the predominant effect that limits the safe operating area of the transistor. At these extreme conditions, TDDB and in particular SILC should also be taken in consideration in the dielectric reliability of the gate oxides. Nowadays, these degradation mechanisms are not considered of vital importance. However, the tendency is to continuously reduce the oxide thickness. Therefore, the quality of the gate oxide in the sub-micron technologies needs some special attention [Kassakian01]. New characterisation and measurement techniques will be developed and applied for smart power technologies. The standard CMOS characterisation techniques are not applicable any longer to the integrated power transistors, as the latter operate under different conditions (e.g. characterisation of lattice heating, heat distribution, switching of inductive, capacitive or resistive loads…). In this work mainly two state-of-the-art measurement systems will be used to analyse the hot carrier degradation on lateral DMOS transistors and leakage current in thin-oxides. Both systems are based on the in-situ accelerated ageing technique with electrical testing as developed by the Institute of Material Research (IMO) and IMEC vzw [In-situ90].

The multi-sample hot carrier test bench can handle the high voltages/power of the lateral DMOS transistor at elevated temperature with stability in the order of 0.03°C. 48 samples can be measured at four different stress conditions for statistical analysis. Lateral DMOS transistors processed in a 0.7 μm CMOS based smart power technology with oxide thickness of 42 nm will be used to investigate the impact of hot carrier degradation on smart power devices. High-resolution hot carrier measurements will be carried out on package level and the observed degradation effects will be investigated. The measured data will be used to develop a degradation model. Modelling of device degradation is a translation of the understanding of the physical mechanisms leading to degradation of device parameters. In the last few years, different models have been developed to describe hot-carrier degradation on standard field effect transistors (i.e.: MOSFETs, LDD MOSFETs…). Models of Hu [Hu85], Goo [Goo95] and Dreesen-Croes [Dreesen99] are the most used models to describe the shift on the degradation parameters due to hot carrier effects. The physical effects behind these models are well known. Recent works extend these models to describe the hot-carrier degradation on high power devices. The model of Goo [Goo95] will reveal to be most suitable.

On the other hand, new measurement equipment will be developed in this work to study SILC degradation mechanism. This high-resolution measurement system will be used to

monitor small current changes at high speed (less than 1ms). A *device under test (DUT)* can be submitted to a desired temperature profile (up to 900°C) and a constant voltage/current stress. The electrical property of interest can be continuously measured, i.e. in-situ. Oxide-breakdown can be a showstopper for the use of ultra-thin oxides in aggressively downscaled devices. Therefore, it's very important to predict the oxide reliability in an accurate and correct way. It has been demonstrated that charge-to-breakdown cannot give a correct reliability prediction for this ultra-thin oxides. Only if time-to-breakdown is measured using constant voltage stress (CVS), consistent reliability data are obtained [Nigam99]. Measuring Stress Induced Leakage Current (SILC) during stress will be fundamental to understand the precursor effects that lead to oxide breakdown. Increased leakage current under high gate voltage level for long period is a good monitor of the number of defects in ultra-thin oxide and should be analysed with care [Degraeve99]. SILC measurements will be carried out on planar MOS integrated capacitor, with oxide thickness of 2.4 nm, due to its simplicity of fabrication. The fabrication of the capacitor uses the same processing scheme as used for the fabrication of integrated circuits.

Reliability analysis will be performed on packaged devices, which can create more difficulties in the physical understanding of the device degradation behaviour. High voltage transistors are limited in power by electrical and thermal phenomena triggering their internal bipolars and leading in general to the destruction of the device. The electrical effect reflects the intrinsic capability of the device and constitutes its maximum physical limit. The thermal one depends on the conditions applied to the device and reduces the maximum power much below its intrinsic capability. This thermal effect is originating from the heat generated when for instance a high power is forced through the device. Indeed the temperature increases locally in the transistor reducing the built-in potential of the junctions. At the same time, the sheet resistance of the doped regions increases with increasing temperature. Small currents, due to thermal generation or impact ionisation, are able to polarise a junction in forward state, triggering internal parasitic bipolars. During switching between ON and OFF states, electrical transients occur forcing high power through the transistor. In the middle of the driver, the heat dissipation of the elementary cell device is limited to one dimension perpendicular to the device surface as the surrounding cells are also producing heat. It is then clear that in smart power technologies thermal effects acquire a special importance and should be taken in consideration. The use of a high-resolution measurement system with well-controlled temperature stability will be the key factor to achieve good results. It will be

shown that the development of the degradation model for the leakage current of thin oxides will strongly depend on the quality of the measured data. Insufficient measurement accuracy will lead to uncertainty with respect to the choice of the proper statistical distribution or badly defined failure distribution parameters.

1.3. Outline of the thesis

In chapter 2 some of the basic terms and definitions important for the oxide reliability study are listed. The chapter begins with an overview of different oxide defects. This is followed by a discussion of the mechanisms that determine these oxide defects and in particular the hot carrier degradation mechanism and stress induced leakage current in thin oxide. The basics of the last 20years of these two degradation mechanisms will be covered and the physical knowledge and the different test methodologies will be discussed. At the end some relevant oxide reliability models will be presented.

Chapter 3 describes the high-resolution SILC measurement system (HR-S-MT) developed to perform measurements on thin oxide at ultra-low voltages. First, the devices under study will be described. Second, the degradation parameters will be defined and the measurement set-up is presented. The use of the constant voltage stress and the measurement procedure will be explained in detail. Frequency analysis and the high temperature stability will contribute to the high-measurement resolution of the test system.

In chapter 4 a detailed description of the SILC degradation mechanisms and models will be given. The contribution due to SILC and the contribution due to charge trapping will be distinguished. Through the use of an appropriate model, SILC-related parameters and trapping-related parameters will be quantified. The extrapolation of high voltage measurements to operating conditions is still possible taking into account these new results, but should be performed with care. The refined model of Nigam and co-workers [Nigam99] will be used with some adaptations to describe the gate current behaviour. An alternative method for the determination of part of the fitting constants will be used, fitting the current's derivative instead of the actual current density. The derivative *dJ/dt* will show significant scattering particularly during the initial period of the measurement. Therefore, a smoothing method, based on least structure method of Cook [Cook63] will be applied to the original measured data before taking the derivative. At the end, the physical interpretation of the results and the voltage dependency will be discussed.

Chapter 5 describes the measurement technique developed to perform high-resolution hot-carrier degradation measurements on lateral DMOS transistors. Performing high-resolution hot-carrier measurements on high power devices is not straightforward. During this work, the test bench has to be protected from environmental influences. First, the devices under study will be described and the degradation parameters defined. Then the measurement set-up is presented and the measurement procedure will be explained in detail [In-situ90].

In chapter 6 a complete analysis on the hot carrier degradation of lateral DMOS transistors will be shown. First, the devices and experiments are described. It will be shown that upon hot carrier stress, two different and competing hot carrier degradation mechanisms occur. The mechanisms could be identified by analysis of the electrical data and by performing Charge Pumping (CP) experiments. The experimental results will be discussed giving a clear evidence for the existence of source-side injection degradation. An overview of the most used models will be proposed and among them the best suitable model will be adapted and used to describe the behaviour of the lateral DMOS transistors. Detailed TCAD simulations are also performed, supporting the proposed model.

The conclusions of this work will be presented in chapter 7.

1.4. Reference of the chapter

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2. Degradation of thin film oxide

2.1. Introduction

The metal-SiO_2-Si (MOS) system is by far the most important and the most used. However, oxide defects like interface traps and oxide charges are intrinsic in a practical MOS device and, in one way or another, affect the ideal characteristics. Moreover external factors can influence the normal behaviour of the device, which requires a trustful knowledge of the physical mechanisms involved in the generation of oxide defects [Sze81].

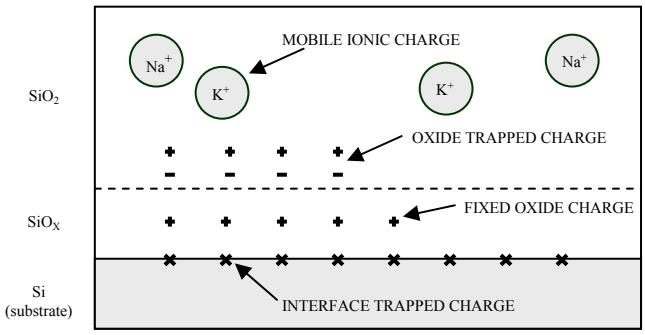

Figure 2.1: Four different types of charges in the Si-SiO_2 system [Sze81].

There are four basic types of traps and charges (fig. 2.1). *Interface trapped charges (Q_{it})* can possibly be produced by excess silicon (trivalent silicon), excess oxygen and impurities. Q_{it} are located at the Si-SiO_2 interface with energy states in the silicon forbidden band gap and they can exchange charges with silicon in a short time. For the present MOS devices having thermally grown SiO_2 on Si, low temperature (450°C) hydrogen annealing can neutralize most of the interface-trapped charge [Nicollian82]. Excess silicon or the loss of an electron from excess oxygen centers near the Si-SiO_2 interface is the origin of *fixed oxide charges (Q_f)*. These charges are located at or near the interface and they are immobile under the influence of an applied electric field. The density of fixed oxide charge depends on the oxidation temperature, on cooling

conditions and the crystallographic orientation of the silicon grains. It is not influenced by the electrical operating conditions of the MOS transistor and by the oxide thickness [Sze81]. *Oxide trapped charges (Q_{ot})* are commonly produced by the injection of hot electrons or holes from an avalanche plasma in a high field region in the silicon, injection of carriers by photoemission or by exposure to ionizing radiation [Sze81]. These oxide traps are associated with defects in SiO_2. The oxide traps are usually electrically neutral, and are charged by electrons and holes introduced into the oxide. The area of injection depends on the device under test and the field distribution. Like for fixed oxide charge Q_{ot} is fixed. Oxide trapped charge is located either at the metal-SiO_2 interface or at the Si-SiO_2 interface. Only when the oxide traps are introduced by ion implantation Q_{ot} can be distributed within the oxide layer [Nicollian82]. In thermally grown SiO_2 films, *mobile ionic charges (Q_m),* such as sodium and potassium, are mainly responsible for the instability of the oxide-passivated devices. At high temperatures and voltages, Q_m can move back and forth through the oxide layer, depending on biasing conditions giving rise to voltage shifts. Thus, many reliability problems in semiconductor devices may be related to trace contamination by alkali metal ions. This type of charge is located at the metal-SiO_2 interface, where it originally entered the oxide layer and at the Si-SiO_2 interface under an applied field. A film impervious to mobile ions can prevent mobile ionic charge contamination of the oxide during device life [Nicollian82]. Temperature, illumination, ionisation radiation and *hot carrier (HC)* injection are some of the most common external influences that can increase the concentration of these defects inside the oxide and a certain point affect the normal device behaviour. In the next paragraph we will give a detailed overview of hot carrier injection and SILC mechanisms, which are the main topics of this work.

2.2. Hot-carrier Injection

It is recognized that hot carrier degradation is one of the foremost reliability problems in submicron transistors. The decrease of device dimensions, such as the channel length, the junction dept and the gate oxide thickness, without proportional scaling of the power supply voltage to sub-micron ranges, accompanied by increasing substrate-doping densities, results in a significant increase of the horizontal and vertical electric fields in the channel region. Electrons and holes, gaining high kinetic energies in the electric field, may be injected into the gate oxide and cause trapping of carriers on defect sites in the oxide or the creation of interface states at the silicon-oxide interface, or both as a

consequence of the different stress condition applied to the device. The physical nature of degradation is mainly based on the shifts in device current characteristics. However, shifts in threshold voltage and changes in transconductance or substrate current only indirectly reflect the physical damage at the interface. Moreover, hot-carrier degradation is very localized and the area of degradation depends on the technology under study. Therefore, the interpretation and the analysis of the data are complex and should be made with care [Groeseneken99]. On the other hand, carrier injection should not always be considered as an undesirable process. The programming mechanism of all non-volatile memory devices indeed is based on the possibility for carriers to be injected into the gate insulator, and be trapped there (EEPROM nMOS cells) or collected on a floating gate (EPROM, EEPROM, flash EEPROM). A wide variety of injection mechanisms can be adopted, and hot-carrier injection is one of them [Dreesen99].

2.2.1. Hot-carrier Injection into SiO_2: physical mechanisms

There are many different mechanisms of carrier injection into the SiO_2. For nMOS transistors, the main degradation effect at high drain voltage is still the channel hot-carrier injection. In the channel injection mechanism, several types of scattering events have to be considered to quantify the probability that electrons could be injected into the gate oxide. The first event to be considered is the acceleration of a channel electron by the lateral electric field along the channel. When the hot-electron reaches the drain end of the channel its momentum has to be redirected toward the interface by a collision, which should not be an energy-robbing collision. The "lucky" electron will retain the kinetic energy required to surmount the Si-SiO_2 potential barrier through *quasi-elastic-scattering* [Hu79].

Following the redirecting collision, the electron must travel from the point of collision to the oxide interface without suffering further collisions, which would redirect its momentum or diminish its kinetic energy. If the electron reaching the oxide interface has sufficient kinetic energy to overcome the oxide potential barrier, it is injected into the gate oxide. The channel hot-electron current and the subsequent damage in the gate oxide are localized where the lateral electric field is high (*injection zone*) [Dreesen99]. It is also possible that electrons (E_e=1.6eV), moving from source to drain by the high electric field, first create *avalanche plasma* by impact ionization, consisting of generated electrons and holes pairs. While most of the created electrons are attracted toward the drain, some electrons and holes in the avalanche plasma with sufficient kinetic energy

(E_e=3.1eV, E_h=4.8eV) are injected into the gate oxide. Most of the holes created by this process are collected by the substrate, creating the drift component of the substrate current [Hu79]. The fraction of the drain current that contributes to the impact ionization substrate current is a function of the lateral electric field (E_L) in the drain depletion region, the gate bias V_{gs} and the channel length (L) [Dreesen99]. However, the differences between quasi-elastic-scattering mechanism and avalanche plasma mechanism are disputable.

2.2.2. Oxide defects due to hot carrier injection

The oxide trapped charge and interface trapped charge play an important role in the degradation of the oxide characteristics. The charge distribution and the charge density inside the oxide are altered when the existing traps in the oxide capture excess of electrons and holes. The probability that injected carriers can be capture by an empty trap depends on the available trap density and the trapping cross section. However, charge trapping can explain only some of the observed degradation effects in nMOS transistors. Nowadays, it is established that not only charge trapping but also interface trap generation contributes to the degradation of the electrical characteristics. Hot electrons and hot holes can generate new interface traps, which are in electrical communication with the conduction and valence bands of the silicon and can be charged and discharged depending on the surface potential [DiMaria93]. The gate voltage applied determines the contribution of the two mechanisms.

Usually, in standard MOSFETs, the shift of the device parameters follows a time power law At^n, where t is the stress time and A is a parameter, which depends on the applied drain voltage and on the technology. The induced damage increases when the hot carrier injection is performed at gate voltage corresponding to the maximum substrate current. The slope n≈0.5-0.7 of the power law is due to the creation of fast interface traps. At low V_g, hot electrons and hot holes are injected together in the oxide leading to a combination of interface state creation, hole trapping and electron trapping. At high V_g, only electrons are injected into the oxide inducing electron trapping. A power law with n≈0.2-0.3 characterizes the degradation under these gate voltages [Hu85]. This physical behavior should not be generalized to all MOS devices. For example, the shift of LDD MOSFETs parameters saturates at high stress condition and cannot be described by a simple power law. In power DMOS transistors the contribution of charge trapping and interface trap generation is a complex function of the applied stress voltage, due to the complexity of

the device structure. However, the knowledge of standard MOSFET degradation mechanisms will be used as a starting point in the analysis of power devices.

2.2.3. Different structures used in VLSI nMOS transistors

In modern technologies, conventional devices cannot longer guarantee the hot carrier degradation-related criteria demanded to guarantee reliable circuit performance. Since hot-carrier degradation was recognized as an obstacle for device scaling, many attempts have been made for limiting its impact and making devices more resistant to it. The key to hot-carrier optimisation is the reduction of the electric field peak. In the LDD structure, narrow self-aligned n^- regions are introduced between the channel and the n^+ regions. This structure reduces impact ionisation (and thus hot-carrier emission) by spreading the high electric field at the drain pinch-off region into the n^- region. As a consequence of the lower field intensity, an LDD nMOSFET shows a significant reduced degradation. This allows either an increase in power supply voltage or a reduction in channel length at a given voltage to achieve a performance enhancement. Thus, a shorter channel length can be used for a given supply voltage. However, these devices suffer from additional degradation associated with the spacer oxide region [Dreesen99]. LDD MOSFETs are not the only devices developed to achieve better reliable performances. In the last few years, the market and in particular automotive industries drove the research in the direction of novel structures capable of handling high drain voltages and high current levels combined with standard low voltage CMOS logic cells. Lateral DMOS transistors (LDMOS) are one of the devices of choice. In the last two chapters of this work, based on the knowledge achieved on standard nMOSFET devices and LDD-nMOSFET, we will perform a complete analysis and modeling of this emerging technology.

2.3. Stress-Induced Leakage Current (SILC)

In ultra-thin oxides (t_{ox}<3.5nm), when an external gate voltage (V_G) is applied across the oxide, due to the resulting oxide field ($E_{OX}=V_{OX}/t_{OX}$), electrons can tunnel directly (DT) (fig. 2.2) through the trapezoidal oxide barrier, from the cathode to the anode without entering the SiO_2-conduction band leading to a gradually increasing gate current over time [Stathis98]. During this high field stress, several phenomena such as interface trap creation, charge trapping, hole fluence and neutral electron trap creation occur. The prediction of oxide reliability under operating conditions still involves extrapolation

beyond the range of gate voltages used in stress experiments, and this requires a trustful knowledge of the dependencies of defect generation and critical breakdown defect density on stress voltage and temperature. The interpretation of the term defect at the microscopic level has not been fully clarified. Moreover, we do not have techniques for the direct measurement of the defect density.

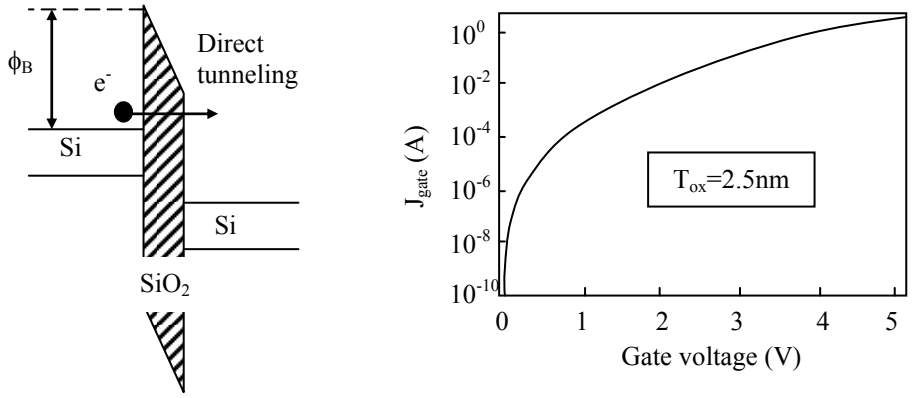

Figure 2.2: Energy band diagram for direct tunneling oxide injection and an example of current-voltage characteristic [Degraeve99].

2.3.1. SILC: standard method to monitor oxide degradation in thin oxide

The methods used for monitoring the oxide degradation do not yield a direct measure of the amount of generated defects but only an associated electrical effect [Stathis00]. In thick oxides, the decrease of current or the C-V shift are related to electron trapping in the generated trapping sites. In thinner oxides, SILC has already become an indirect standard method used for monitoring the oxide degradation [Nigam98]. However, a high-resolution state-of-the-art measurement technique is necessary because the background direct tunneling current can mask the time evolution of SILC at low voltages. In the early eighties Maserjian et al. [Maserjian82] reported on the degraded insulating quality of thin SiO_2 layers which had been subjected to electrical stress. For the first time they observed that the leakage current through such a dielectric layer at low and medium oxide fields increased with increasing electrical stress. In the last few years with the development of new technologies, SILC itself became in some cases a more important reliability problem than oxide breakdown [Maserjian82]. Under a given stress condition, SILC, continuously monitored as a function of time rises with injected fluence and shows two main

components. An initial decaying transient component leads to a steady state SILC after some time. Directly after stress, the interface traps are charged giving rise to the transient component [Nigam99]. Later on, trap-assisted tunneling from cathode to anode causes Steady-state SILC. In thick oxides the probability that an electron has sufficient traps that can be used as stepping-stones for tunneling is very small, resulting in a small steady-state component. In thinner oxides, fewer traps are necessary for the electrons to move from cathode to anode and therefore the steady-state component will dominate.

2.3.2. SILC related reliability problems

Leakage current through the gate means a permanent power waste problem in MOSFETs but especially in non-volatile memories SILC can be a dangerous problem erasing the information memorized. Some observations indicate that power consumption increase, due to SILC, is most likely not to become a critical issue. The importance of DT-current rapidly increases and becomes the main contributor to I_G current under operating conditions since the gate insulator thickness is reduced. Therefore, compared to SILC generated after high electrical stress, DT-current contribution remains the main cause of off-state power consumption. Moreover, in a well designed/fabricated integrated circuit only part of the power consumption is due to the gate leakage current and electrical stress is an exceptional event that occurs only in a very small fraction of the transistors. Therefore, even if SILC is generated, it's unlikely to have a substantial impact on the total power IC consumption or in case it will create a problem only in non-mainstream applications, as e.g. low-power applications. [Nigam98]. On the other hands, in floating-gate *non-volatile memories (NVM)* the situation is different. The memory content of a floating-gate device depends on the amount of charge stored on the floating-gate and consequently, any charge transfer affects its state. On this principle is based the electrical programming and erase operations and any unwanted leakage current, e.g. SILC, can change the memory content and also the non-volatility of the device. In order to facilitate the programming/erase (P/E) operations thin dielectrics are recommended as floating-gate insulation, but they suffer more from SILC. Due to the stress induced by repeated P/E-cycling, the generation of SILC is very likely to occur in NVM devices. These considerations need to be balanced to obtain devices both performant and reliable.

2.4. Models for oxide degradation

Even if there is a disagreement about the physical mechanisms involved in the generation of the oxide defects, two main types of model can be find in the most recent literature [Sune01]. There is the thermo-chemical model of McPherson and co-workers, who consider that the generation of defects is driven by the electric field and the stress time [McPherson98]. On the other side, there is the electron energy dissipation model, in which it is considered that the injection of carriers through the oxide is required to create the damage. In both cases there is a general agreement to relate the defect generation to breakdown.

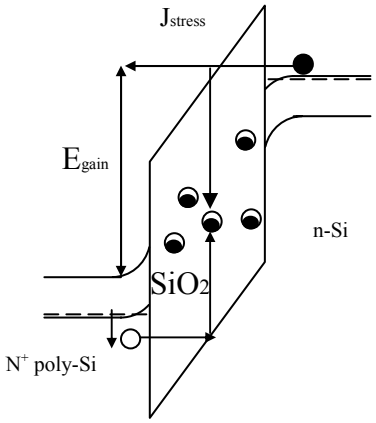

Figure 2.3: Energy band diagram showing the oxide defects mechanism based on the Anode Hole Injection (AHI) model.

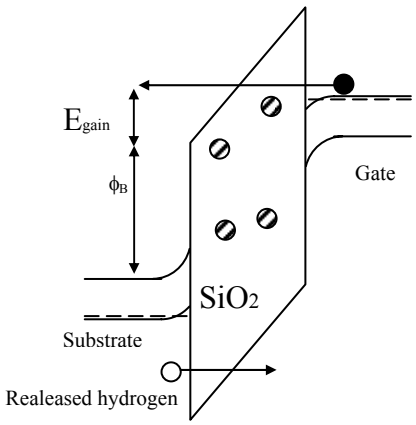

Figure 2.4: Energy band diagram showing the oxide defects mechanism based on the Hydrogen Release (HR) model.

Even if the electric field mechanism has a certain success based on physical basis, there is much experimental evidence in the literature to demonstrate the essential role of the energy delivered by the electrons and the fluency and energy driven phenomenon of the breakdown. For thin oxides in the ballistic regime, the energy dissipation model is compatible with an exponential dependence on the applied voltage in reasonable agreement with experimental results. The electron energy dissipation model has two main versions: The *Hydrogen Release (HR)* model and the *Anode Hole Injection (AHI)* model. In both cases, electrons are injected through the oxide and release their energy at the anode interface where they free up some positively charged species, which are

subsequently re-injected into the oxide and generate the damage [DiMaria93]. The AHI model (fig. 2.3) was initially proposed in the mid eighties by Hu and co-workers, and in the last few years has received more consideration based on detailed physics-based simulations. The basic idea of this model is that the positively charged species generated in the anode and re-injected into the oxide are holes [Sune01]. After getting trapped in some precursor site, the holes cooperate with electrons in the generation of permanent defects. However, the actual mechanism by which holes create the oxide defects has not been clarified yet, and recent experimental results suggest that the rate of defect creation by holes in SiO_2 is by far too low. The general process assumed in the HR model (fig. 2.4) is similar to that of the AHI model. In this case, the role of the positively charged species is assumed by some hydrogen species. For long time Hydrogen has been considered as an intrinsic impurity in the Si/SiO_2 system, but recent experimental evidences suggest its direct relation with the degradation of SiO_2. In this model, hot electrons are assumed to dissipate their energy and release hydrogen form the Si/SiO_2 anode interface. In a second stage of the process, hydrogen travels through the oxide and reacts with some precursors to form the neutral electron traps and as a consequence trigger the breakdown. The energy associated to this defect is comparable with recent carrier separation measurements demonstrating inelastic trap assisted tunneling as the mechanism involved in the stress induced leakage current that precedes the dielectric breakdown in thin oxides. Moreover, the hydrogen bridge also fulfils the requirement of being a neutral electron trap [DiMaria93].

2.5. Conclusion

Oxide defects like interface traps and oxide charges are intrinsic in a practical MOS transistors and, in one way or another, affect the ideal characteristics. External factors such as temperature, illumination, ionization radiation and hot carrier or avalanche injection can influence the concentration of these defects and the normal behaviour of the device. Therefore, a trustful knowledge of the physical mechanisms involved is required.

In the never-ending technology evolution, HC injection still reveals to be the most important degradation mechanism. On the other hand, real world insulators like SiO_2 show carrier conduction when the electric field or temperature is sufficiently high. The case of thin oxides, operating at very low gate voltages, requires special attention. The prediction of oxide reliability under operating conditions still involves extrapolation beyond the range of gate voltages used in stress experiments, and this requires a trustful knowledge of the dependencies of defect generation and critical breakdown defect density on stress voltage and temperature. Stress Induced Leakage Current (SILC) has already become an indirect standard method used for monitoring the oxide degradation of small devices.

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3. High-resolution SILC measurement technique

3.1. Introduction

The oxide thickness in recent CMOS technologies has decreased to only a few nanometers and simultaneously the device operating voltage has been lowered. This evolution has created new challenges for accurate determination of the gate oxide reliability, since the time to oxide breakdown, as measured at the stress voltage, now has to be extrapolated to a voltage range comparable to the Si-bandgap. A phenomenon that occurs during oxide degradation is the generation of a low-field leakage current through the gate well known as Stress-Induced Leakage Current (SILC). SILC generated after constant voltage stress has in the past proven to be a very sensitive tool to study low voltage oxide degradation. Accurate SILC-measurements, however, require a well-controlled experimental environment, and especially the temperature control during the stress is critical.

The Institute of Material Research (IMO) and IMEC vzw developed the in-situ accelerated ageing technique with electrical testing [In-situ90]. The goal of this technique was to study the electrical behaviour of a given material during thermal annealing as a function of temperature and time. A device can be submitted to a desired temperature profile and the electrical property of interest can be continuously measured, i.e. in-situ. In the beginning, the method has only been used to study accelerated ageing of material systems of which the ageing can be characterized by the DC electrical resistance. A high measurement resolution is obtained in the order of 1 to 5 parts per million (ppm) for a device with a temperature coefficient of around 100 ppm/°C, whereas the comparable resolution with the conventional method (off-line) is in the order of 500 ppm [De Schepper90a]. Therefore, the ageing kinetics of the system can be studied in more detail, and on the shorter time scale.

The studies performed with the in-situ accelerated ageing technique were done on passive components as well as on active components with the temperature and/or the current/voltage as a stress condition. Some typical applications of the in-situ technique are hybrid thick film ageing [De Schepper90b], ageing behaviour of ball bonds [Tielemans89], diffusion in thin film resistors [De Ceuninck92], defect relaxation [De Ceuninck90], ageing behaviour of glass ceramic dielectrics in thick film multilayer [Manca94], electromigration [D'Haeger93] and hot-carrier degradation [Dreesen99]. In

this work the technique will be used to study SILC on thin oxide at ultra low voltages. The experience obtained using the in-situ measurement in numerous different applications gave us the possibility to build a dedicated high-resolution measurement system to monitor small current changes at high speed.

This is important in order to determine the individual contributions of SILC among different degradation mechanisms in the complete time frame of stress and therefore a full validation of the proposed model is obtained. With this set-up, the stress voltage can be lowered to $|V_g|$=0.9 V on 2.4 nm oxides, corresponding to actual device operating conditions. It has been shown by Stathis et al. [Stathis00] that, for an oxide with this thickness and area of 5 10^{-4} cm^2, it takes approximately 300 years to reach breakdown at $|V_g|$=1.9 V. In this case, therefore, it is impossible to reach breakdown at lower voltages within a reasonable measurement time. However, we shall demonstrate that oxide degradation occurs under these stress conditions and no significant change in the degradation mechanism could be observed. This proves that extrapolations of high voltage measurements to operating conditions are indeed possible, provided that the correct extrapolation model is used.

In this chapter, the high-resolution SILC measurement system (HR-S-MT) is proposed in order to perform high-resolution SILC measurement on thin oxide at ultra-low voltages. The advantages of using such measurement are:

- Degradation at low stress voltage can be distinguished.
- The contribution of different degradation mechanisms can be distinguished.
- Modelling as well prediction can be improved by making use of high-resolution data.

Performing high-resolution SILC measurements on thin SiO_2 is not straightforward. During this work, the test equipment has to be protected from environmental influences as described further in this chapter.

In section 3.2, the devices under study and the reasons why we choose them to study SILC degradation will be described. Then (section 3.3), the degradation parameters are defined and the measurement set-up is discussed. The reason for using constant voltage stress and the measurement procedure will be explained in detail (section 3.4). Power supply stability and the high temperature stability (section 3.5) will all contribute to the high-measurement resolution of the test system (section 3.6).

3.2. Devices under study

The MOS capacitor is generally used to study the electrical properties in the SiO_2, at the Si-SiO_2 interface and in the silicon, due to its simplicity of fabrication. The fabrication of the MOS capacitor uses the same processing as used for the fabrication of integrated circuits. Therefore the MOS capacitor provides a direct measurement of the SiO_2 oxide behaviour [Sze81].

Planar MOS capacitors with 2.4 nm conventional oxides grown on p-type substrate were used for the purpose of this study. The capacitor area equals 1.26 10^{-3} cm^2.

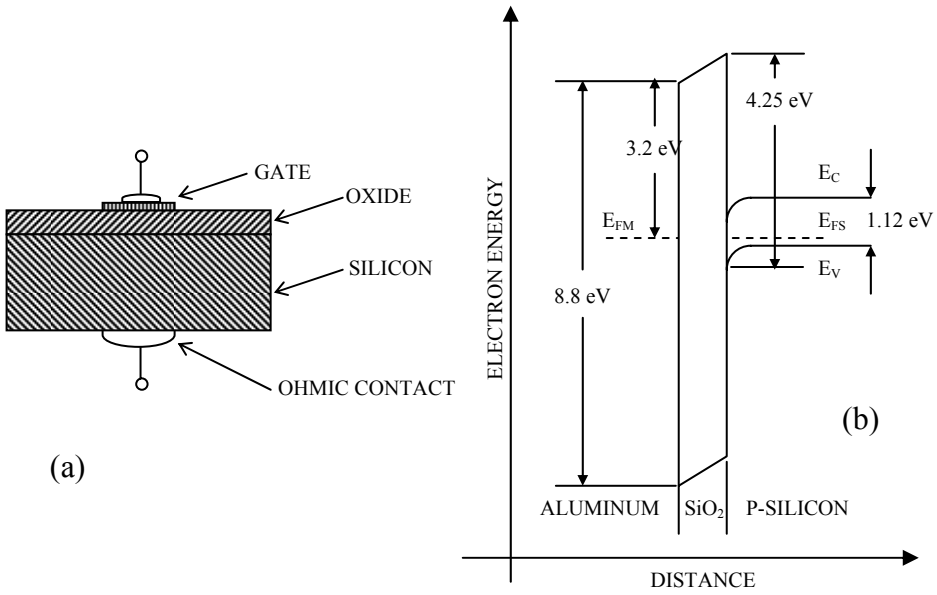

Figure 3.1: (a) Cross section of a MOS capacitor. (b) Energy band diagram of a MOS capacitor [Sze81].

The MOS capacitor consists of parallel plates with one electrode a metallic plate called the gate, while the other electrode consist of the silicon. A thin insulating layer of SiO_2, as shown in figure 3.1a, separates the two electrodes. Figure 3.1b shows the forbidden energy gaps in SiO_2 and silicon for the MOS capacitor and the Fermi level in the gate and in the silicon.

The forbidden gap in SiO_2 is very large (8.8 eV), whereas that of the silicon is much smaller (1.12 eV). Also shown is the Fermi level for the aluminium gate. Aluminium is a common gate metal because it's easy to evaporate and it adheres strongly to the oxide. A large energy barrier exists between the metal and the oxide, with an equally large barrier between the silicon and the oxide. These energy barriers are generally determined by internal photoemission measurements. The importance of these energy barriers is that they prevent free flow of carriers from the metal to the silicon or vice versa. Thus the application of a bias across the MOS capacitor in normal condition does not result in current flow (apart from transients related to charging the capacitor). Rather, an electric field is established in the oxide by surface charge layers that form in the metal and in the silicon [Sze81].

By placing a negative bias on the gate, the negative charges on the gate attract holes to the silicon surface to form an accumulation layer. With the increase of bias gate voltage negative charges are removed form the gate and holes leave the *accumulation layer*. At a gate bias called the *flatband* voltage, the silicon will be neutral everywhere. As the gate bias is made positive with respect to the flatband, holes are repelled from the silicon surface by negative acceptor ions in the *depletion layer*, so called because holes have been depleted from this region. When the bias gate voltage is increased, electrons appear at the silicon surface in great numbers due to thermal equilibrium. As holes are repelled from the silicon surface, electron density must increase to keep the *pn* product constant. These electrons form a thin *inversion layer* located very near to the $Si\text{-}SiO_2$ interface. The depletion layer and the neutral silicon are placed below the inversion layer. Any further increase in positive gate charge is balanced almost entirely by the addition of electrons to the inversion layer [Sze81].

3.3. The measurement-setup

Figure 3.2 shows a schematic overview of the main parts of the measurement set-up. The measurement equipment is connected to the routing box. From the routing box, a direct connection with the DUT is established. A platinum resistor is used to measure the temperature as close as possible to the DUT. All the measurements are performed on packaged devices, which are placed in a special designed furnace.

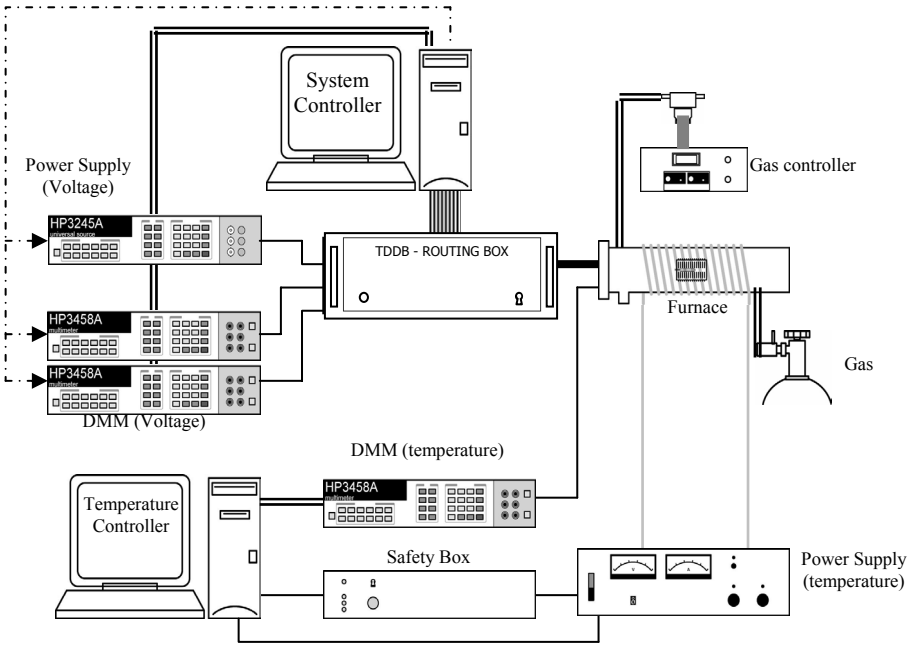

Figure 3.2: schematic overview of the main parts of the measurement set-up.

Figure 3.3 shows the routing box with 17 relays to select the DUT, two Butterworth filters and two amplification circuits.

- From R1 to R8, one of the DUTs can be routed to the voltage source.
- From R9 to R16, the capacitors not connected to the voltage source are connected in parallel to a resistor of 1 MΩ to avoid electrostatic discharge in case the samples are floating.
- R17 connects all the capacitors to ground through a resistor of 1 MΩ to avoid electrostatic discharge when the package is placed on the sample holder inside the chamber.
- A current to voltage module converts the leakage current in voltage.
- Two Butterworth Filters are included to limit the bandwidth of the signal to avoid aliasing frequencies.
- A non-inverting amplifier magnifies the incoming signal.

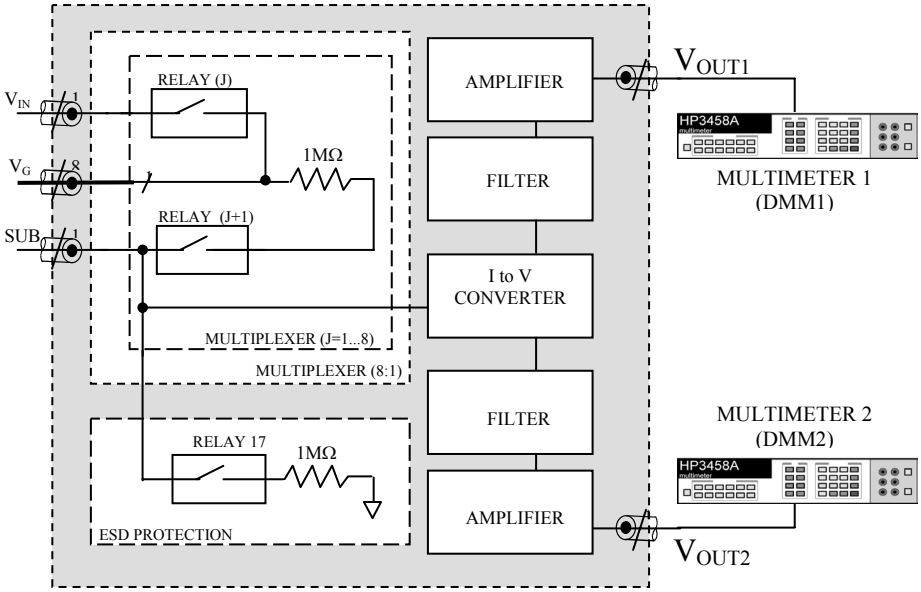

Figure 3.3: Block diagram of the routing box.

Figure 3.4 gives a detail overview of the measurement equipment.

- The voltage source is used to apply negative gate voltage V_g, while keeping the substrate grounded.
- Multimeter 1 (DMM1) monitors the output voltage of the circuit at high speed in the order of 100 microseconds and afterwards at 1 reading per second.
- Multimeter 2 (DMM2) measures the output voltage of the circuit for longer period at half the speed of multimeter1 in buffer mode.
- Multimeter 3 (DMM3) is needed for the measurement of the temperature inside the chamber.

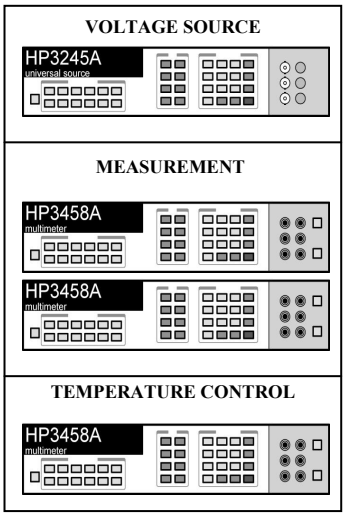

Figure 3.4: Measurement equipment overview.

Apart from the high resolution of the meters, several factors can disturb the measurement signal and many precautions have been undertaken to minimize their effects. Vibration, insulator deformation, contamination, humidity, electrostatic coupling and groundloops can all generate stray currents in the test circuit and reduce measurement accuracy. The cabling of the electrical circuit, the handling of the test structures and the control of the measurement environment have a great importance to achieve high-resolution. Therefore, all the connections from the DUT to the routing box and from the routing box to the measurement equipment are made with special coaxial cables to reduce disturbances on the low level signal due to triboelectrical effects. Additionally, the cables, being as short as possible, have been tied or taped down as much as possible [Keithley92].

3.4. Measurement procedure

In this section, it will be explained in detail how this equipment has been used for measuring the degradation parameter of interest.

3.4.1. Handling of the samples

Special precautions have been taken to avoid unwanted *Electrostatic discharge (ESD)* on the sample during the handling. ESD is an important problem in VLSI technology and can be confused with many other oxide degradation mechanisms. The use of special input protection circuits virtually eliminates the concern about instabilities due to ESD stress at the gate. However non-catastrophic ESD stress can be still possible and samples should be handled with care. Moreover, contamination from materials such as body sweat, containing numerous cations and anions, and solder flux combined with humidity causes electrochemical reactions, which can result in picoamps or more of error current.

In order to avoid contamination of the test structures, DUTs are stored in a special box and during mounting into the sample holder they are handled with antistatic gloves. Since the construction of the sample holder requires soldering, careful cleaning is needed afterwards. Firstly, the sample holder is immersed in an acetone bath and submitted to ultrasonic vibrations during 15 minutes. After 24 hours drying the sample holder undergoes a similar treatment in a methanol bath and is allowed to dry before use. The effect of these operations reduces the magnitude of the residual currents in the sample holder in the order of 10^{-13} A [Manca94].

3.4.2. Stress condition

In the two most accepted models (Anode hole injection model and Hydrogen release model) it is assumed that a positive species generated at the anode is responsible for oxide degradation, which leads to breakdown [Nigam99]. The generation rate of the positive species is determined by the energy of the electron at the anode. For thicker oxide (>7 nm) FN-injected electrons enter the conduction band of the silicon dioxide and interact with the SiO_2-lattice. This is the *Non-ballistic FN-Tunneling* as schematically illustrated in figure 3.5c.

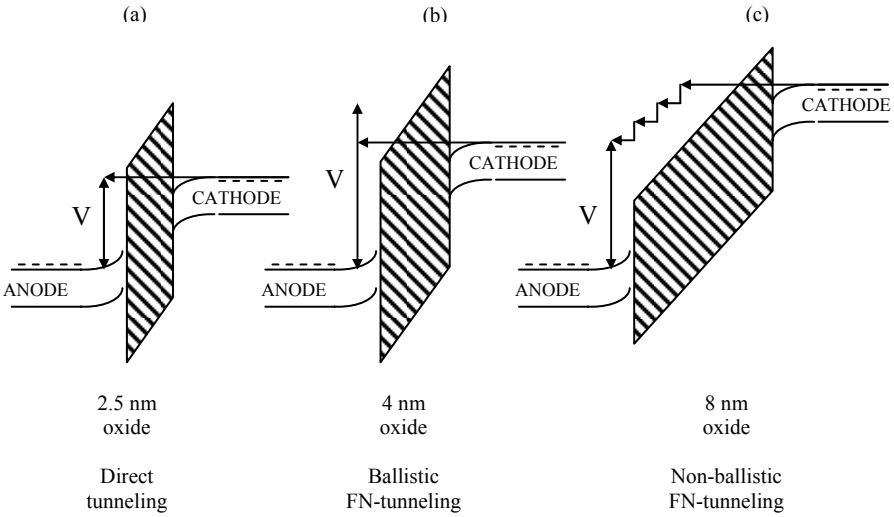

Figure 3.5: Energy band diagram for three different tunneling oxide injections: Direct Tunneling, Ballistic FN-tunneling and Non-ballistic FN-tunneling

The oxide field determines the electron energy at the anode and consequently the oxide degradation. Since there exists a unique relationship between the FN current density and oxide field, the charge to breakdown should be measured using *Constant Current Stress (CCS)*. For ultra thin oxides (<5 nm) the injected electrons travel ballistically through the oxides without interacting with the SiO_2. This can be *Ballistic FN-tunneling* (5 nm to 3.5 nm) or *Direct-tunneling (DT)* (<3.5 nm) as illustrated in figure 3.5b and figure 3.5a, respectively. Therefore, the electron energy at the anode is determined by the voltage difference between the cathode and the anode, which correspond to the applied gate voltage. As a consequence the charge to breakdown should be measured using Constant Voltage Stress (CVS) and not CCS [Nigam98].

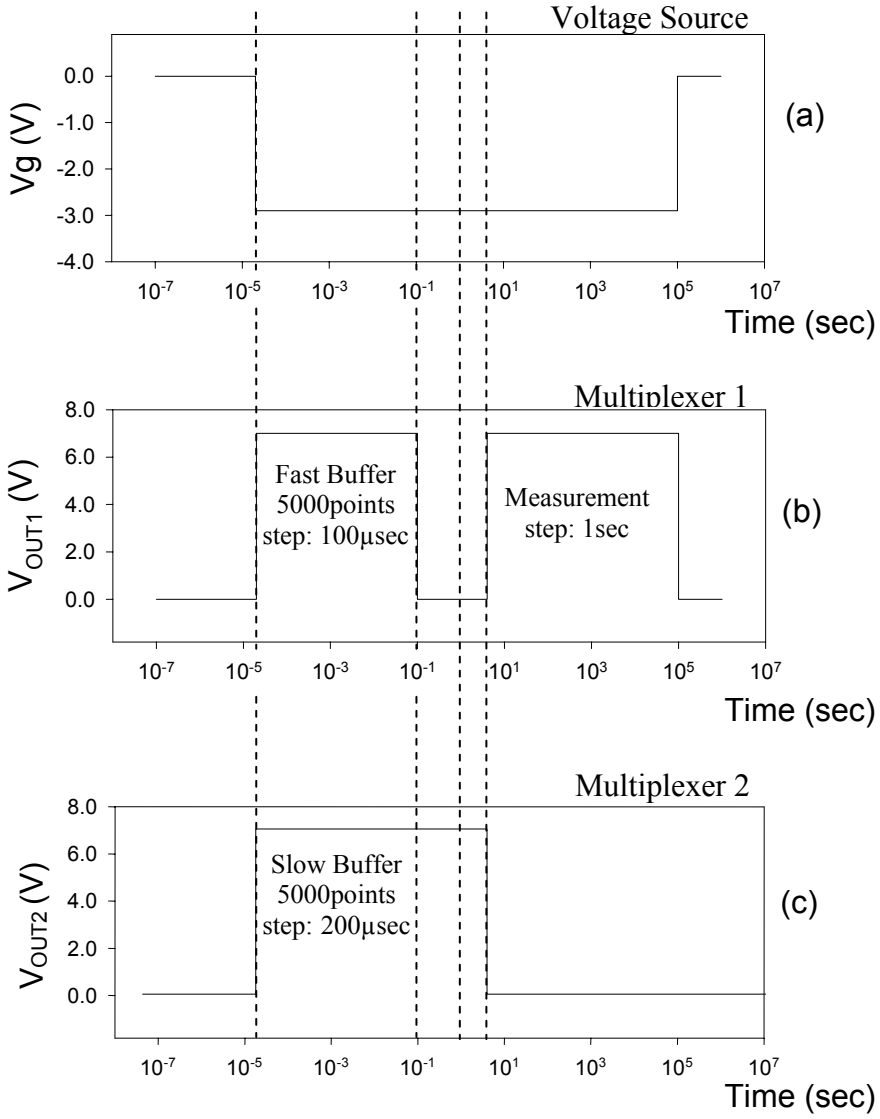

Figure 3.6: Schematic representation of the measurement cycle for measuring leakage current through thin oxide at constant stress voltage.

3.4.3. High-speed measurement

Commercial electrometers such as K2400 or K487 are too slow to measure leakage current in thin oxide capacitors. Therefore it was necessary to make our own I/V converter to perform high-speed measurement. The high-resolution SILC measurement system is able to detect small current changes after short stress time. The high-resolution combined with high-speed measurement is used to distinguish the contribution of the different degradation mechanisms. Figure 3.6 gives a schematic representation of the measurement cycle for measuring leakage current through a thin oxide at constant stress voltage. All the measurements are performed at 100 °C. During the degradation, the leakage current is converted to voltage, allowing measurements at high speed. The stress voltage is applied as soon as a temperature stability of 0.002 °C is reached.

Figure 3.6 (a) shows the constant stress voltage as a function of time. In contrast with previous works the stress and the measurement voltages are equal and it's not necessary to interrupt the stress periodically for measuring the SILC effect. Comparisons between SILC measured at different voltages are possible when normalizing the measurements to the same reference voltage (V_{ref}) as explained in the next chapter [Nigam99]. Two HP 3458A multimeters are set to buffer mode measurement and waiting for the signal trigger from the computer. The source voltage and the meters are synchronized and triggered at the same time. The fast buffer stores 5000 points at a frequency of 10 kHz. The transfer of the data to the PC takes less than one second. The second buffer, called slow buffer stores 5000 points at a frequency of 5 kHz. As soon as the data of the second buffer are transferred, multimeter 1 switches to a normal continuous measurement mode at a rate of one reading per second (fig. 3.6 (b)). The slow buffer has been introduced to avoid a data gap between the fast buffer measurement and the continuous measurement (fig. 3.6 (c)).

3.5. Performance of the measurement system

The measurement resolution is determined by three contributions: the stability of the voltage supply, the accuracy of the multimeters and the temperature stability.

3.5.1. Constant Voltage Stress (CVS)

A negative gate voltage Vg was used to stress the gate oxide, while keeping the substrate grounded. Other stress mechanisms such as Substrate Hot Hole Injection (SHHI) and plasma-process, which result in SILC as well, won't be taken in consideration. [Nigam99]. The measurement resolution of a given electrical parameter is also

determined by the stability of the voltage supply. Therefore, the voltages are supplied by a HP3245A with a high stability of ±10 ppm (fig. 3.7). The measurement set-up is able to monitor current changes in the order of 100 microseconds. Thus, it's important that the power supply reaches the constant stress level and stabilizes before the first value of current is measured (fig. 3.8).

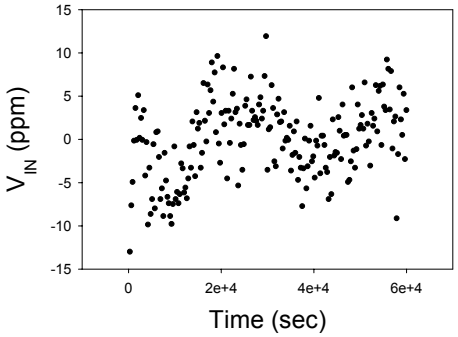

Figure 3.7: Power supply stability.

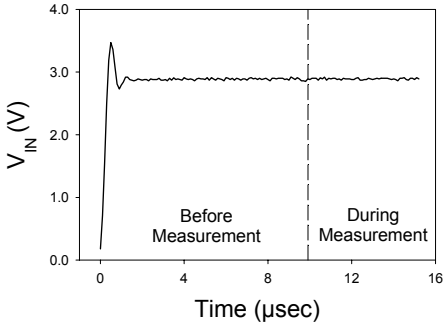

Figure 3.8: Rise time characteristic of the power supply.

3.5.2. Frequency analysis

The two multimeters HP3458A are set in high-speed mode. In this mode, there is no rejection of power line related disturbances. Since the multimeters have a variable sample rate no anti-alias filter is provided. The Nyquist or sampling theorem states:

If a continuous bandwidth limited signal contains no frequency components higher than F, then the original signal can be recovered without distortion (aliasing) if it is sampled at a rate that is greater than 2F samples per second.

In practice, the multimeter's sampling rate must be at least twice the highest frequency component of the signal being measured. Therefore, an external anti-aliasing low-pass filter with a sharp cut-off at a frequency equal to half the digitizer's sample rate is used to bandlimit the input signal. The maximum sample frequency of the multimeter HP3458A is equal to 100 kHz. Figure 3.9 shows the frequency spectrum of a fast buffer mode measurement after the I/V converter (R_{conv}=2.2kΩ), calculated using Fourier technique. Unwanted frequencies can be detected in the spectrum, which are probably due to

parasitic. The I/V converter with a capacitor as a device under test (fig. 3.10), acts like a differentiator and therefore amplifies high frequency (parasitic) signals. The value of the conversion resistance determines the amount of amplification at high frequency as can be seen in figure 3.11.

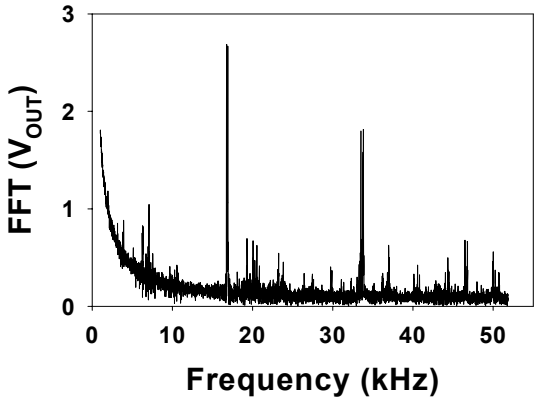

Figure 3.9: Frequency Spectrum of a buffer test measurement after the I/V converter (R_{conv}=2.2kΩ) calculated with Fourier technique.

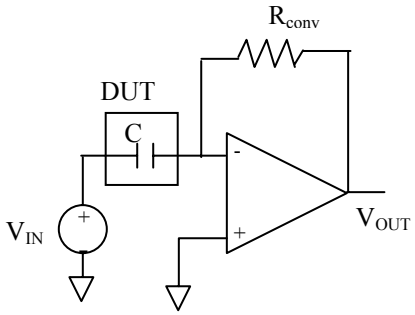

Figure 3.10: Overview of the capacitor under study and the conversion circuit.

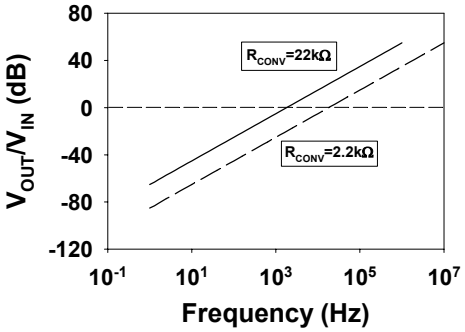

Figure 3.11: Frequency response of the capacitor under study and the conversion circuit.

The amplitude of the parasitic peaks needs to be substantially lower compared to the signal itself to avoid clipping of the signal. A lower value of conversion resistance

reduces the amplification of the unwanted signal inside the circuit. However, the resistance must be high enough to convert the small input current to a measurable output voltage.

A good compromise is a conversion resistance equals to 2 kΩ and a sample rate of 10 kHz with a band limitation of the signal at 5 kHz for the fast buffer and a sample rate of 5 kHz with a band limitation of the signal at 2.5 kHz for the slow buffer. Two dedicated 4th order Butterworth filters, specific for each buffer, are introduced in the circuit in agreement with the Nyquist theorem.

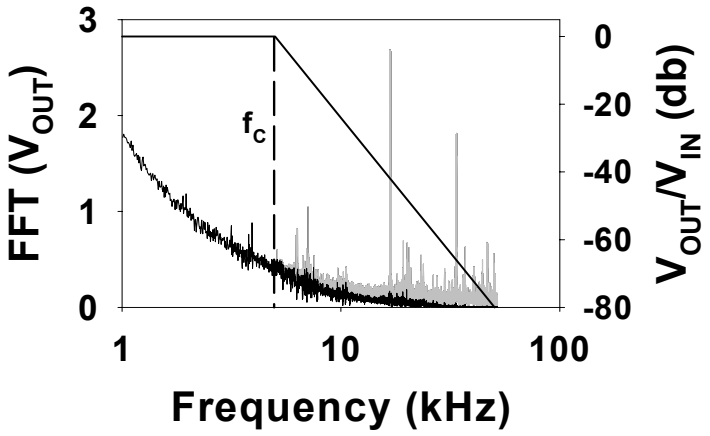

Figure 3.12: Frequency Spectrum of a buffer test measurement after the I/V converter (R_{conv}=2.2kΩ) calculated with Fourier technique.

Figure 3.12 shows the FFT signal with the filter response on top. The peaks of the unwanted frequencies are out of the bandwidth of the Nyquist filter and are not enough high to get clipping at the output of the I/V converter.

3.5.3. High resolution temperature stability

Temperature fluctuation is an important factor that can influence the measurement resolution. The *temperature coefficient (TC)* will be determined from a measurement performed at low stress Vg=0.9 V. In this case all the fluctuations of the leakage current are due to the temperature fluctuations. Figure 3.13 shows the plot of ΔP versus ΔT. A straight line is obtained and the TC is defined as the slope of this line. A TC of 5000

ppm/°C is obtained. Measurements were performed at 100 °C in agreement with the industrial reliability specifications for oxide lifetime (90 to 120 °C). Figure 3.14 shows the long-term temperature stability of the furnace used in this work. A temperature stability of 0.002 °C was obtained by making use of this special designed furnace. With this temperature stability the maximum parameter change due to a temperature fluctuation is around 10 ppm. Thus, the temperature fluctuation is no longer the crucial factor that determines the measurement resolution.

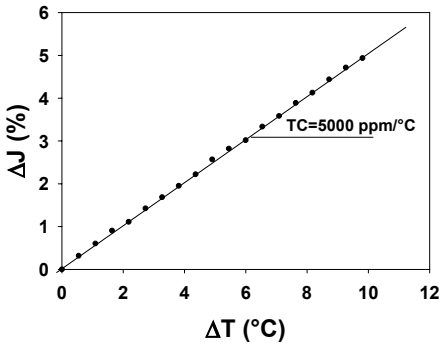

Figure 3.13: ΔP versus ΔT to determine the temperature coefficient (TC).

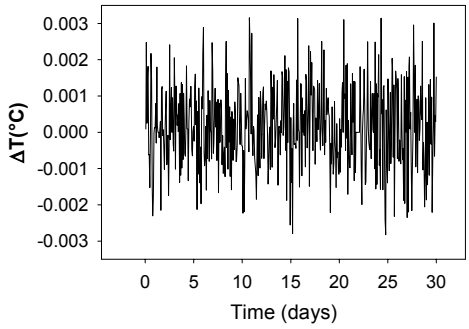

Figure 3.14: Long-term temperature stability of the furnace used in this work with a set point of 100°C.

3.6. Measurement resolution

The measurement of very low current is a delicate matter. Two high-resolution multimeters HP3458A has been used. The resolution of the meters is different depending on the sample-rate chosen during the measurement.

Figure 3.15 shows the measurement resolution at room temperature of the fast buffer (±60 ppm) during a test on a resistor of 500 kΩ to have the same current level with the same stress voltage used during a SILC measurement. A comparable plot is shown in figure 3.16 for the second buffer (±6 ppm). Afterwards, in a normal mode measurement at one reading per second the accuracy of the meter can reach few ppm.

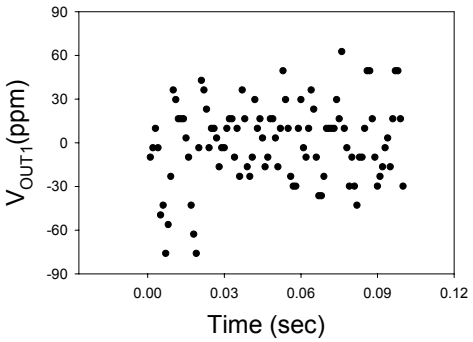

Figure 3.15: Measurement resolution of the fast buffer (±60 ppm) during a test on a resistor of 500 kΩ.

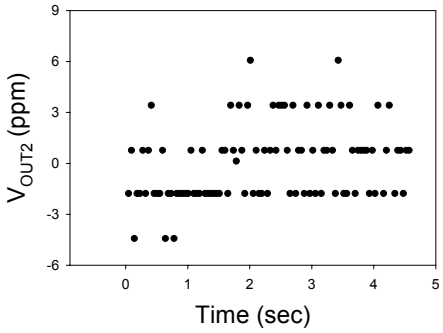

Figure 3.16: Measurement resolution of the slow buffer (±6 ppm) during a test on a resistor of 500 kΩ.

3.7. Conclusion

In this chapter, the HR-S-MT is proposed in order to perform high-resolution SILC measurements on thin oxide at ultra-low voltages.

The advantages of using such measurement are:

- A new generation high-speed, high-resolution system setup has been developed to monitor small current changes at speed in the order of 100 microseconds.
- The initial degradation mechanisms can be studied to extend the knowledge of the degradation process.
- A temperature stability of 0.002 °C was obtained by making use of this special designed furnace.

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4. SILC measurements of thin SiO_2 at ultra low voltages

4.1. Introduction

As already discussed in the previous chapters, leakage current through the gate becomes very important issue in thin oxide, depending on the different applications. It has been evidenced by several people [De Blauwe98] that high gate current cannot affect the MOSFET operation and the general power consumption of the integrated circuit. On the other hand, the continuous downscaling of the devices and the different applications make SILC more and more a serious issue. For example, in non-volatile memories any charge transfer to/from the floating-gate affects the memory state. SILC can affect the most essential feature of a NVM device. Moreover, SILC can lead to oxide breakdown in novel devices making use of ultra-thin oxides. A high-resolution state-of-the-art technique is necessary to measure low magnitude of leakage current at voltage levels as low as |Vg|=0.9 V, corresponding to actual device operating conditions [Insitu90]. In this chapter an initial overview of the SILC degradation mechanisms and models will be given (section 4.2 and 4.3). The contribution due to SILC and the contribution due to charge trapping will be distinguished. Through the use of an appropriate model, SILC-related parameters and trapping-related parameters will be quantified. The extrapolation of high voltage measurements to operating conditions is still possible taking into account these new results, but should be performed with care. The refined model of Nigam and co-workers [Nigam99] with some adaptations can describe the gate current behaviour (section 4.3.2). An alternative method for the determination of part of the fitting constants is used (section 4.4), fitting the current's derivative instead of the actual current density (section 4.4.1). The derivative *dJ/dt* shows significant scattering particularly during the initial period of the measurement. In section 4.4.2, a smoothing method, based on a least structure method of Cook, is applied to the original measured data before taking the derivative. In section 4.5, the voltage dependency will be discussed and conclusions will be drawn in the last section.

4.2. Trap-Assisted-Tunneling mechanism (TAT)

In the last few years several models have been proposed in order to explain the physical origin of the characteristic field-dependence of SILC. The *Poole-Frenkel mechanism*

(PF) was the first one that introduced the conduction of carriers from trap to trap in a thermally assisted way. However, the leakage current is independent on the temperature. Therefore, this model revealed to be not consistent [De Blauwe98].

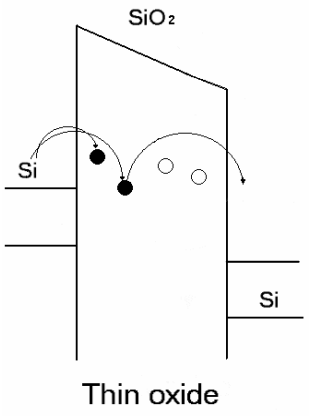

Figure 4.1: Schematic representation of the Trap-Assisted Tunneling mechanism.

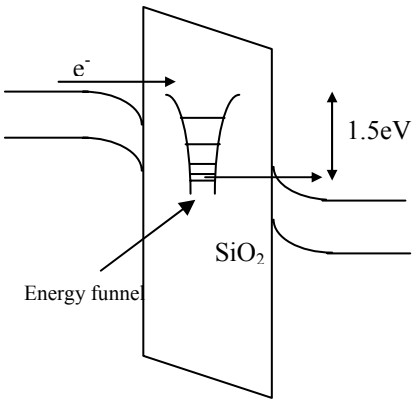

Figure 4.2: Schematic representation of the Energy funnel.

Accordingly to the *charge-assisted tunneling mechanism (CAT),* SILC is the result of a local lowering of the oxide barrier for the conduction band electrons due to the presence of the trapped positive charge. Even in this case, SILC has been found almost independent of the measurement polarity and of the stress polarity. Therefore if trapped charge is at its origin, the charge configuration in the oxide after the stress should be symmetrical in contradiction with the C-V characteristics [DiMaria93], [Sze81]. The most common accepted model is the *trap-assisted tunneling mechanism (TAT)* (fig. 4.1). Electrons directly tunnel from trap to trap in a field assisted way with a two-step process or a multi-step process. This can be respectively from the cathode into a trap and from the trap to the anode or with multiple traps involved. The trap-assisted conduction mechanism implies that the traps are both spatially and energetically located not further than 3 to 4 nm to communicate with each other and with the interfaces. When the distance is larger the direct-tunneling probabilities become too small to be consistent with the large SILC current levels. Recently, it has been shown that the carriers lose 1.5 eV in the SiO_2 layer [De Blauwe98]. Two mechanisms based on trap-assisted tunneling have been proposed to explain the physical origin of this energy loss: *Inelastic conduction band tunneling (ICBT)* and *elastic valence band tunneling (EVBT)*. Inelastic tunneling is supported by the oxide thickness dependence of SILC and carrier separation

experiments. However, the exact mechanism for the energy loss is still not yet clear. Another explanation is the multi-phonon emission on the so-called *energy funnels*. According to this mechanism, resonant tunneling occurs from trap to trap and energy relaxation happens by emitting multiple phonons within the trap, i.e. in the energy funnel (fig. 4.2). The inelastic trap-assisted tunneling mechanism is consistent with many experimental observations. For a given trap density the probability to tunnel from the cathode to the trap is independent on the oxide thickness and only the probability to tunnel from the trap to the anode increases in a thin oxide. As a consequence, the leakage current in thin oxide increases even if fewer charges are trapped. In a thick oxide the leakage current is negligible and the trapping component is predominant [DiMaria93]. According to the inelastic trap-assisted tunneling mechanism, SILC increases at higher electrical stress conditions, due to the larger number of bulk-oxide traps. This mechanism is supported by experimental evidence given by the one-to-one correlation between SILC and the neutral electron traps [De Blauwe98]. Moreover, the insensitivity of SILC with respect to the stress polarity is explained by assuming that trap creation is spatially uniformly distributed. The percolation model for the dielectric breakdown and tunneling-front model for trapping have already described the uniformity trap creation [Degraeve99]. These experimental evidences made the trap-assisted tunneling the most accepted and supported mechanism to describe SILC degradation of thin oxides.

4.3. Modelling of the degradation behaviour

Within a thin dielectric layer significant direct tunneling (DT) through the trapezoidal oxide barrier occurs, and with it, a new defect creation mode, characterized by an increasing current over the time at constant voltage [Nigam98]. In the beginning of the 1997s, Xie and co-authors presented an interesting investigation about the instability of defects created in ultra-thin insulator, metal-oxide-silicon biased in the direct tunnel regime [Xie97]. In this study, the gradually increasing current over time has shown to correspond both to an increase in positive charge trapped in the thin oxide, which increases the tunnel probability for DT electrons and to the growth of a defect-assisted conduction path through the oxide. Each defect is assumed to contribute to the fractional increase in the leakage current. The model used to fit the experiment results is a modified first order kinetic equation with the reasonable assumption that the defect creation probability is exponentially dependent on the depth of the defect precursor in the oxide. The precursors closer to the oxide surface will be converted to defects at higher speed

than those located deep inside the oxide. Thus, the depth dependence is taken in account by explicit adding exponential time dependence to the first order kinetic relationship. The defect creation rate is given by:

$$\frac{dn}{dt} = n_h \nu_{th} \sigma_0 e^{-t/\tau_{tr}} \left(n_{\max} - n\right) = K e^{-t/\tau_{tr}} \left(n_{\max} - n\right) \tag{4.1}$$

where n_h is the density of carrier that may be holes, which control the degradation, ν_{th} is the charge carrier thermal velocity and $\sigma_0 e^{-t/\tau_{tr}}$ is the capture cross section for these charges, including the explicit dependence on the oxide depth by way of exponential time dependence with time constant τ_{tr}. n_{max} is the total number of defect precursors and n is the number of precursors transformed to active defects. The solution to this equation can be written as:

$$n(t) = n_{\max} - \left(n_{\max} - n_{\min}\right) \exp\left[K \tau_{tr} \left(e^{-t/\tau_{tr}} - 1 \right) \right] \tag{4.2}$$

n_{min} is the number of defects, which are already present at the start of a degradation period, assumed to be zero at the initial stressing of a device, but not necessary zero for subsequent stressing periods. Using the approximation $e^{-x} \approx 1-x$ we have:

$$\frac{J - J_0}{J_0} = n(t) = n_{\max} - n_{\max} \left[1 - 1 - K \tau_{tr} \left(e^{-t/\tau_{tr}} - 1 \right) \right] \tag{4.3}$$

and then:

$$\Delta J = J_0\left(V_g\right) + J_0\left(V_g\right) n_{\max} K \tau_{tr} \left[1 - e^{-t/\tau_{tr}} \right] \tag{4.4}$$

and if we impose:

$$N^+\left(V_g\right) = J_0\left(V_g\right) n_{\max} K \tau_{tr} \tag{4.5}$$

we have:

$$\Delta J = J_0\left(V_g\right) + N^+\left(V_g\right) \left[1 - e^{-t/\tau_{tr}} \right] \tag{4.6}$$

However, this first order kinetic model of Xie predicts saturation behaviour of the gate current as opposed to the measured current behaviour (fig. 4.3) [Xie97].

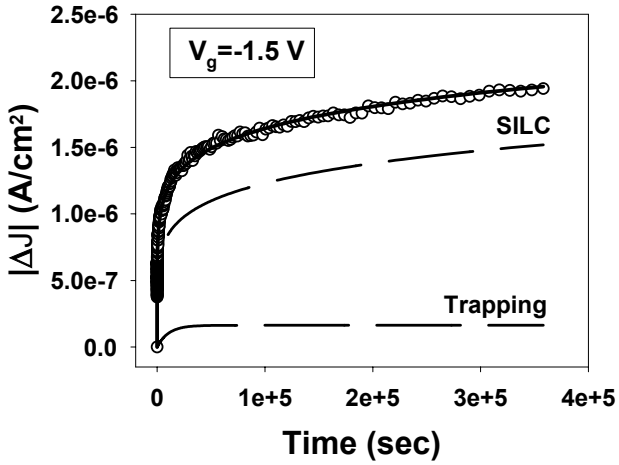

Figure 4.3: Dots: Change in current density as a function of time at V_g = -1.5 V. Line: Fit with the model of Nigam. Long dash lines: Positive charge trapping component and SILC component.

The positive charge trapping alone cannot fully explain the increase in current. One year later De Blauwe at al. [De Blauwe98] proposed that this increase in tunnel current is due to SILC, which is superimposed on the positive charge trapping effect. SILC is described by a power law equation as a function of stress time and injected charge:

$$J_{SILC} = \alpha \cdot t^{\nu} \tag{4.7}$$

Therefore, the tunnel current increase can be described using a combination of trapping and SILC generation. The model of Nigam [Nigam99] describes the change in the current density as a function of time:

$$\Delta J = N^{+}\left(V_g\right)\left[1 - e^{-t/\tau_{tr}}\right] + \alpha.t^{\nu} \tag{4.8}$$

with ΔJ the change in current density, t the time, $N^{+}(V_g)$ the saturation value of positive charge trapping, τ_{tr} the trapping time constant and α and ν the SILC-related parameters, as discussed further on. The first term in the equation represents an exponentially saturating trapping of positive charge, while the second term represents the increase due to SILC-generation.

4.3.1. Direct tunneling (J_0) determination

The change in current density ΔJ as a function of time at a fixed voltage V_g is a sum of three different components defined as:

$$\Delta J = J_{meas} - J_{tun} - J_{Leak}(0) = J_{SILC}(t) \tag{4.9}$$

where J_{meas} is the total measured current density, J_{tun} is the direct tunnelling current density in an ideal oxide without traps and $J_{Leak}(0)$ is the leakage current density due to neutral electron traps already present in the device. The first value of measured current density (J_0) can be defined as:

$$J_0 = J_{tun} + J_{Leak}(0) \tag{4.10}$$

The small contribution of the initial leakage current $J_{Leak}(0)$ can be neglected and the total current density in thin oxide at time zero is, therefore, equal to the direct tunnelling current.

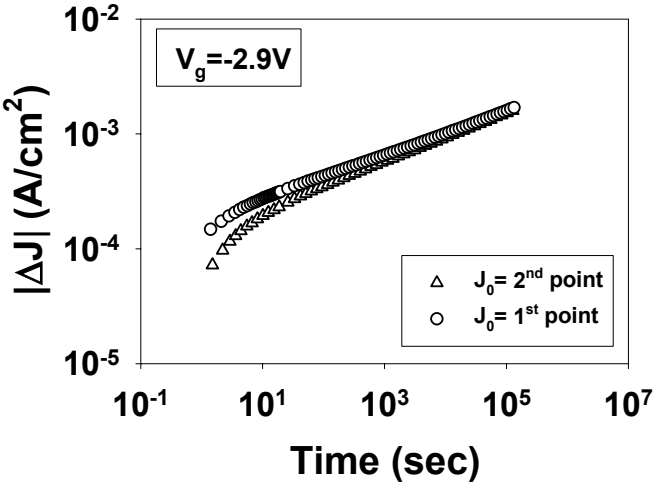

Figure 4.4: Change in current density as a function of time at V_g = -2.9 V using the first measured point as J_0 (upper plot) and the second measured point as J_0 (lower plot).

The state-of-the-art measurement technique used in this work drastically improves the resolution of the SILC measurement as never obtained for such low magnitude of leakage current at working voltages conditions. However, this measurement result creates

an initial difficulty for fitting the model of Nigam to the measured data and in particular the determination of J_0 becomes an important issue. Figure 4.4 shows the change in current density as a function of time at V_g=-2.9 V using the first measured point as J_0 in the upper curve and the second measured point as J_0 in the lower curve. The change in current density is largely dependent on the value of J_0 chosen. Small changes of the first value (J_0) lead to a complete different slope of the curve and, therefore, an uncertainty in the fitting results, proving the necessity to determine J_0 more accurately.

4.3.2. Refined model of Nigam

A first attempt for the determination of J_0 has been made fitting the actual current instead of current change and treating J_0 as a fit parameter. In other word the model of Nigam is rewritten as:

$$J = J_0 + N^+(V_g).\left[1 - e^{-t/\tau_{tr}}\right] + \alpha.t^{\nu} \tag{4.11}$$

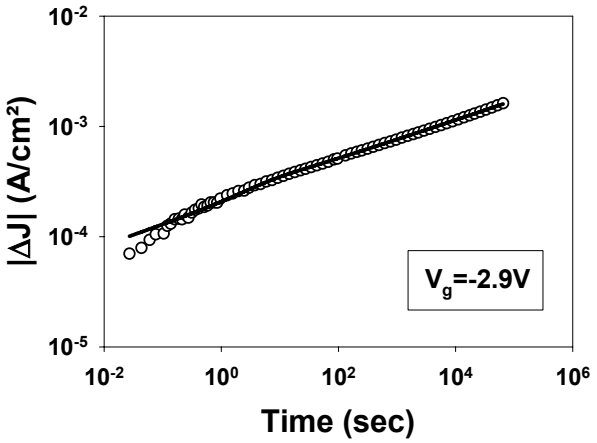

Figure 4.5: Dots: Current density as a function of time at Vg = -2.9 V. Lines: fit with the refined model of Nigam

As shown in figure 4.5 the fitting can describe the change in current density after 30sec of stress where the SILC component is predominant but it has still some problems during the first few seconds of stress where the charge trapping effect is predominant. The difficulties are related with the number of parameters included in the model and the

dependence between them. In the equation 4.5 the dependence between J_0 and N^+ is shown. In particular the determination of J_0 and τ_{tr} influence the fitting of the measured data during the first seconds of stress.

Many numerical elaboration methods, like statistical weight or graphical estimation, have been used to extrapolate the value of J_0 from the measurement data. However, none of those methods were accurate enough. For this reason, a new fitting procedure, based on the independent determination of τ_{tr}, will be proposed in the next section.

4.4. New fitting procedure

The new procedure allows a very precise fitting of the data and the determination of the parameters in two steps independent from each other. The fitting procedure can be list-up in the following way:

- An adapted smoothing method of Cook is applied to the measured current density data.
- The discrete derivative is calculated using the method of Lagrange.
- The derivative data is fitted and the parameter τ is determined in that way, independent on the rest of the parameters and in particular from J_0.
- The refined model of Nigam is now used to fit the measured data using a fixed value of τ_{tr}.

The smoothing method is used to overcome the initial scattering of the derivative. Using simulation data, it proved to be the case that the derivative is very sensitive to the exact value of the model parameter τ_{tr}. As shown before, the fitting can already describe the change in current density after 30 sec of stress where the SILC component is predominant and α and ν can be evaluated. Therefore, using a fixed value for τ_{tr}, J_0 and N^+ can be determined accurately.

4.4.1. Current density derivative

Fitting the current's derivative instead of the actual current density reduces the number of the free variables eliminating J_0 from the model:

$$\frac{dJ}{dt} = \frac{N^+}{\tau}.\left[e^{-t/\tau_{tr}} \right] + \alpha.\nu t^{\nu-1} \tag{4.12}$$

Moreover, the derivative is strongly dependent from the exact value of τ_{tr} but relative independent on the exact value of the rest of the parameters.

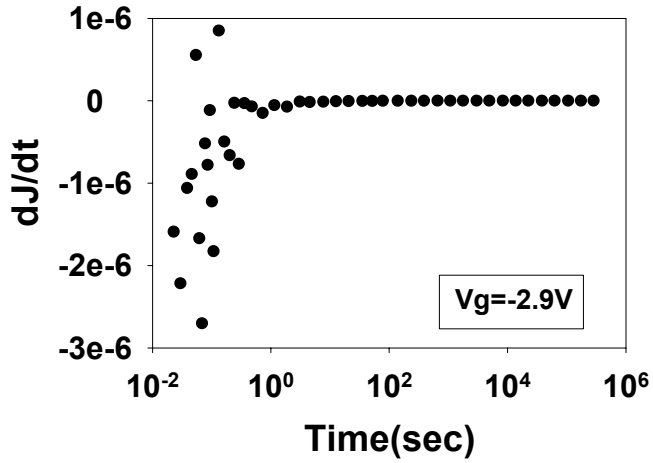

Figure 4.6: Derivative of current density as a function of time at V_g = -2.9 V.

Figure 4.6 shows the derivative of the measured current J at V_g = -2.9 V versus time on a logarithmic scale. The derivative has been calculated using the equation of Lagrange:

$$f'(x) = \sum_{k=0}^{n} l'_k(x) f_k + R'_n(x) \tag{4.13}$$

where:

$$l'_k(x) = \sum_{\substack{j=0 \\ j \neq k}}^{n} \frac{\Pi_n(x)}{(x - x_k)(x - x_j)\Pi'_n(x_k)} \tag{4.14}$$

and:

$$R'_n(x) = \frac{f^{(n+1)}}{(n+1)!}(\xi)\Pi'_n(x) + \frac{\Pi_n(x)}{(n+1)!}\frac{d}{dx} f^{(n+1)}(\xi) \tag{4.15}$$

where:

$$\xi = \xi(x) \qquad (x_0 < \xi < x_n) \tag{4.16}$$

and:

$$\Pi_n(x) = (x - x_0)(x - x_1)\ldots(x - x_n) \tag{4.17}$$

$$\Pi_n(x_k) = (x_k - x_0)\ldots(x_k - x_{k-1})(x_k - x_{K+1})\ldots(x_k - x_n) \tag{4.18}$$

However, unless the current density *J(t)* has been measured with extreme precision, the derivative *dJ/dt* shows significant scattering particularly during the initial period of the measurement. To solve this issue a smoothing method will be applied to the original measured data before calculate the derivative.

4.4.2. Adapted smoothing method of Cook

Among the smoothing methods present in the literature an adaptation of the least structure method of Cook proved to be the most successful method [Cook63]. The method tries to find the smoothest curve that fits the data within the measurement error. Two conditions have to be satisfied to find the smoothest curve and to determine the most acceptable fit of the data within the error:

$$S_I = \sum_{i=1}^{N-1} (J_{i+1} - J_i)^2 \qquad \chi^2 = \sum_{i=1}^{N} \left(\frac{J_i - J_i^{\exp}}{\varepsilon_i} \right)^2 = N \tag{4.19}$$

where S_I is an arbitrary auxiliary function called “the structure function”, χ^2 a statistical variable, N the number of measured points and ε_i the error for a generic measurement J_i. An alternative auxiliary function can be:

$$S_{II} = \sum_{i=1}^{N-1} (J_{i+1} - 2J_i + J_{i-1})^2 \tag{4.20}$$

The mathematical procedure to find the solution J_i which minimizes the $S(J_i)$ with the additional restriction that $\chi^2 = N = \text{const}$ is a well-known problem in the calculus of variations (fig. 4.7).

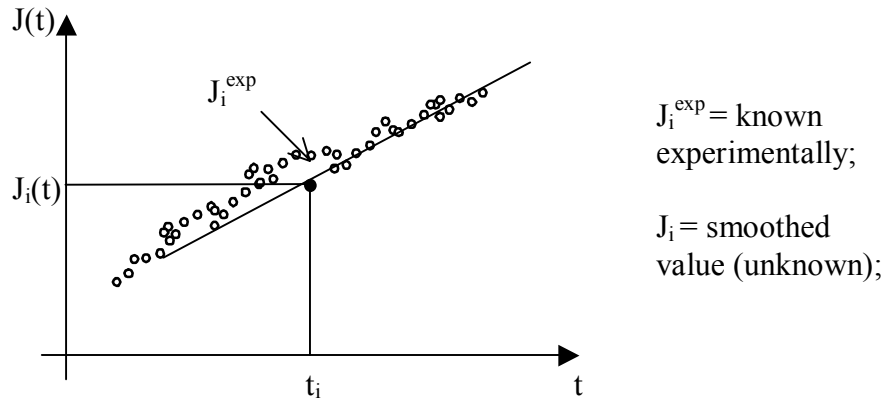

Figure 4.7: Simulation of the current versus time (red dotes) and calculation of the smoothest curve

$S(J_i)$ can be considered as a Lagrange function with dynamic variables J_i. The variables are constrained to lie on a surface χ^2 = const. Using standard methods of variation calculus, the problem can be written as:

$$\lambda \delta S_I + \delta \sum_{i=1}^{N} \left(\frac{J_i - J_i^{\exp}}{\varepsilon_i} \right)^2 = 0 \tag{4.21}$$

where λ is the Lagrange multiplier introduced in the conventional way. The equation can be solved in the follow way:

$$\lambda \delta S_I = 2\lambda \sum_{i=1}^{N} \left(-J_{i-1} + 2J_i - J_{i+1} \right) \delta J_i \tag{4.22}$$

$$\delta \sum_{i=1}^{N} \left(\frac{J_i - J_i^{\exp}}{\varepsilon_i} \right)^2 = 2 \sum_{i=1}^{N} \left(\frac{J_i - J_i^{\exp}}{\varepsilon_i^{\,2}} \right) \delta J_i \tag{4.23}$$

and substituting in the Lagrange equation:

$$\lambda \left(-J_{i-1} + 2J_i - J_{i+1} \right) \delta J_i + \left(\frac{J_i - J_i^{\exp}}{\varepsilon_i^{\,2}} \right) \delta J_i = 0 \tag{4.24}$$

where i=1,2…. N. The δJ_i are independent quantities in the Lagrange method, therefore:

$$\lambda\left(-J_{i-1}+2J_i-J_{i+1}\right)+\left(\frac{J_i-J_i^{\exp}}{\varepsilon_i^{\,2}}\right)=0 \tag{4.25}$$

where i=1,2…. N and with the simplification $\varepsilon_I=\varepsilon$=equal we have:

$$\lambda\varepsilon^2\left(-J_{i-1}+2J_i-J_{i+1}\right)+J_i=J_i^{\exp} \tag{4.26}$$

where i=1,2…. N, that is equal to the matrix form:

$$MJ=J^{\exp} \tag{4.28}$$

where M is defined as:

$$M=\lambda\varepsilon^2 S_I^{matrix}+I \tag{4.29}$$

with:

$$S_I^{Matrix}=\begin{pmatrix} 1 & -1 & 0 & . & . & . & . & 0 \\ -1 & 2 & -1 & 0 & . & . & . & 0 \\ 0 & -1 & 2 & -1 & 0 & . & . & 0 \\ 0 & 0 & -1 & 2 & -1 & 0 & . & 0 \\ . & . & . & . & . & . & . & . \\ 0 & . & . & 0 & -1 & 2 & -1 & 0 \\ 0 & . & . & . & 0 & -1 & 2 & -1 \\ 0 & . & . & . & . & 0 & -1 & 1 \end{pmatrix} \tag{4.30}$$

Therefore, the solution of the equation is:

$$J=M^{-1}J^{\exp} \tag{4.31}$$

or:

$$J_i=\sum_{j=1}^{N}\left(M^{-1}\right)_{ij}J_j^{\exp} \tag{4.32}$$

where M^{-1} is the inverse matrix of M. The alternative auxiliary function S_{II} instead of the S_I gives the alternative matrix S_{II}^{matrix}:

$$S_{II}^{Matrix} = \begin{pmatrix} 1 & -2 & -1 & 0 & . & . & . & 0 \\ -2 & 5 & -4 & 1 & 0 & . & . & 0 \\ 1 & -4 & 6 & -4 & 1 & 0 & . & 0 \\ 0 & 1 & -4 & 6 & -4 & 1 & 0 & 0 \\ . & . & . & . & . & . & . & . \\ 0 & . & 0 & 1 & -4 & 6 & -4 & 1 \\ 0 & . & . & 0 & 1 & -4 & 5 & -2 \\ 0 & . & . & . & 0 & 1 & -2 & 1 \end{pmatrix} \tag{4.33}$$

The solution with $\chi^2 = N$ is called the solution with optimal smoothing or more briefly the solution. Solutions with $\chi^2 < N$ are said to be under-smoothed and solutions with $\chi^2 > N$ are said to be over-smoothed [Cook63].

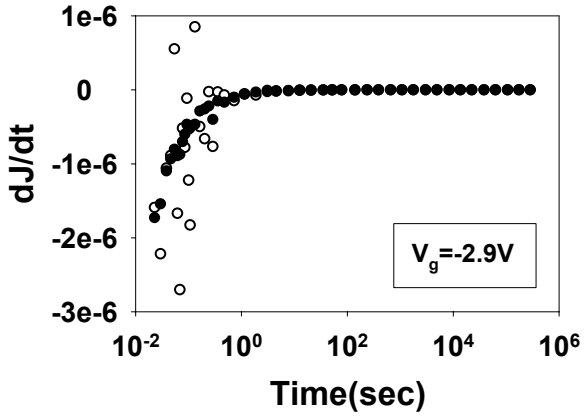

Figure 4.8: Open dots: Derivative of current density as a function of time at V_g = -2.9 V. Full dots: Derivative of smoothed current density at V_g = -2.9 V.

Figure 4.8 shows the derivative of the measured current J at V_g = -2.9 V versus time on a logarithmic scale before and after the smoothing method is applied to the measured data. The smoothing procedure completely solves the scattering issue (full dots).

4.4.3. τ determination

As already shown in the previous section, fitting the current's derivative instead of the actual current density eliminates J_0 from the model and can be used to determine the

exact value of τ_{tr}. The iterative procedure is based on the independence of the derivative from the first measured value. We define an index i as the i-derivative, eliminating i values (i=0…10) in the derivative of the current density. Figure 4.8 shows the values τ_i calculated fitting each i-derivative after applying the smoothing method to the measured current density.

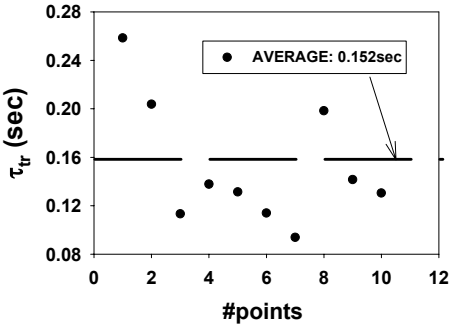

Figure 4.9: Values of τ_i calculated fitting each i-derivative after applying the smoothing method. Measurement at V_g = -2.9 V.

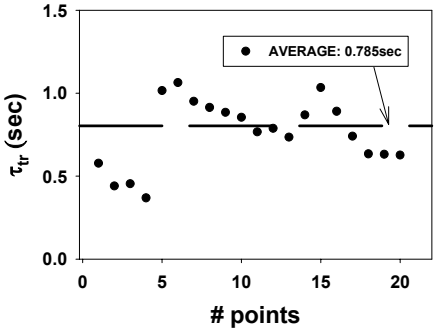

Figure 4.10: Values of τ_i calculated fitting each i-derivative after applying the smoothing method. Simulated measurement.

The average of τ_i gives the value of the τ_{tr}. Simulation has been used to validate the procedure used to determinate τ_{tr}. The model of Nigam is used to simulate the measured current imposing a generic τ_{tr} = 0.787 sec. Noise in the order of 2000 ppm is added to the simulated current density. The smoothing method is applied to the simulated measurement before calculating the derivative. Figure 4.10 shows the values of τ_i calculated using the iterative procedure described above. The average value is $(\tau_i)_{average}$ = 0.785 sec, which is within an error of 0.25 % compared to the proposed value.

4.4.4. Other constant parameters determination

The fit parameters are determined using the refined model of Nigam with a fixed value of τ_{tr}. As shown in figure 4.11 the new procedure improves the fitting of the data during the first few seconds of stress, where the charge trapping effect dominates. This result is due to the reduction of the number of parameters in the model and the independent determination of the charge trapping related parameter τ_{tr}.

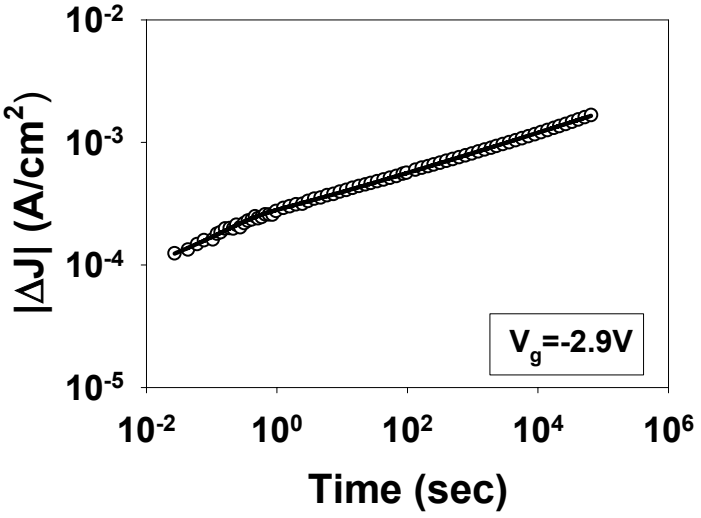

Figure 4.11. Dots: Current density as a function of time at V_g = -2.9 V. Lines: fit with the new procedure.

4.5. Voltage dependency

The SILC-generation is usually measured by interrupting the stress at regular time intervals to measure the JV-characteristics from which the J_{SILC} is extracted at a specific oxide field or voltage. In the measurement technique used in this work the stress voltage equals the measurement voltage.

For the different stress conditions SILC is obtained at different measured voltages and therefore it is necessary to normalize the data to a reference gate voltage (V_{ref}). After this normalization the obtained SILC is identical to the values that would have been obtained if the stress had been periodically interrupted to measure the leakage current at V_{ref} [Nigam99]. The normalization method of Nigam requires the voltage dependence of ΔJ:

- A J-V sweep on a fresh device is performed.
- A stress measurement is performed for an arbitrary time and voltage.
- A second J-V sweep is performed.

- The degradation mechanism is fitted with the model and the charge-trapping component is determined.
- The first J-V sweep and the charge-trapping component are subtracted from the second sweep and the calibration curve ΔJ versus V_g is determined (fig. 4.12).

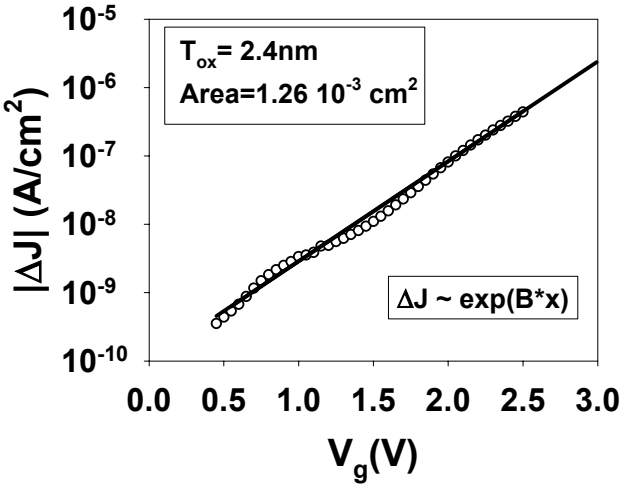

Figure 4.12: Voltage dependency of ΔJ for 2.4nm technology.

The voltage dependency of ΔJ can be described by an exponential. For a chosen V_{ref}, all the measurements are multiplied by the ratio $\Delta J(V_{ref})/ \Delta J(V_g)$. In this way the change in the current density will be the same obtained if the current is measured at reference voltage.

Figure 4.13 shows the performed measurements at gate voltage range –2.9 V down to –0.9 V. The solid lines are fits using the proposed refined model of Nigam. At high voltages, the curves clearly show three different slopes as a consequence of a two-stage degradation process. The measurements show the typical bumpy behaviour during the initial phase of the applied stress, which is attributed to trapping effects superimposed on the straight-line SILC behaviour. In a later stage, the curve becomes parallel to the other as a consequence of the more important contribution of the SILC component. It can be observed that even at V_g as low as –0.9 V, the change in the current density can be described well. At the lower voltages (-2.1 V<Vg<1.9 V), the low contribution of positive charge trapping compared with the SILC contribution allowed fitting the

measured data only with the second term of the equation, resulting in a straight-line behaviour. The measurements do not show the bumpy behaviour during the initial phase of the applied stress but only the parallel straight-line SILC behaviour.

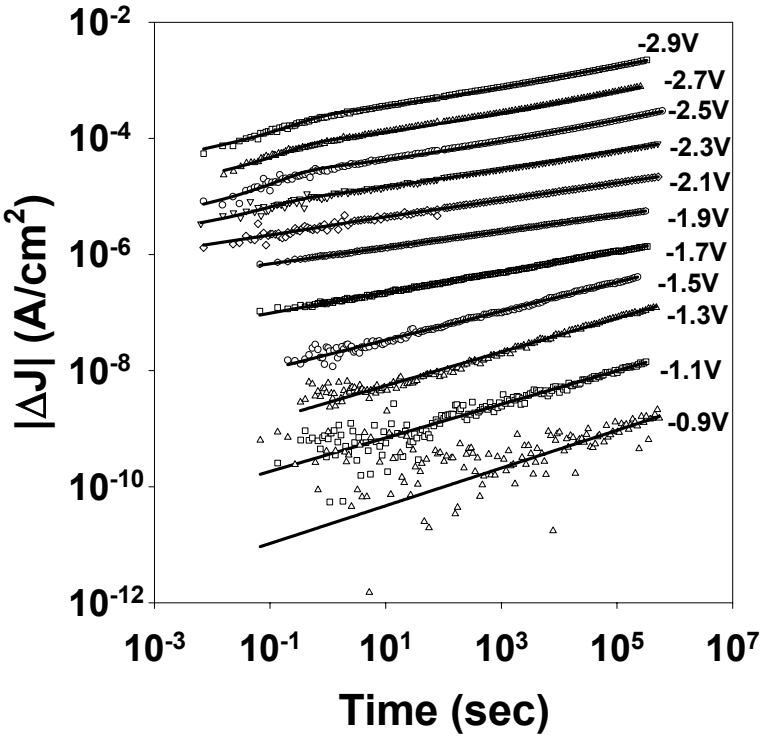

Figure 4.13: Dots: Change in current density as a function of time at 11 different voltages. Lines: Fit with the refined model of Nigam.

At the lowest voltages (-1.7 V<Vg<-0.9 V), a clear change in the slope of the curves can be detected. At these extreme low conditions, we believe that the SILC effect is neglected and the slightly increase of current is due to charge trapping, now visible and not yet saturated. The effect most probably is due to the capture of electrons in already present process-induced bulks traps. These measurements and the initial phase of the measurements at high stress voltages show the same slope (~ 0.3).

4.5.1. Charge trapping-related parameters

The constants in figure 4.14 and figure 4.15 are related to the positive trapping behaviour of the oxide. The trapping time (τ_{tr}) is nearly a constant value (fig. 4.15), which is in agreement with the observation of Nigam e al. [Nigam99] and Xie at al. [Xie97]. Small values of trapping time (τ_{tr}) and the small contribution of positive charge trapping compared with the SILC contribution confirm the importance to detect small current changes after few milliseconds of stress. The saturation value of the positive charge trapping N^+ decreases at low voltages (fig. 4.14). The reduction can be explained by the smaller contribution of the charge trapping, as a consequence of the existence of fewer traps generated at these low stress voltages [Degraeve99].

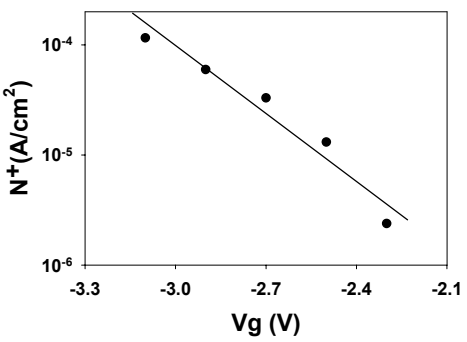

Figure 4.14: The fit constant N^+ related to charge trapping as a function of V_g, in the refined model of Nigam.

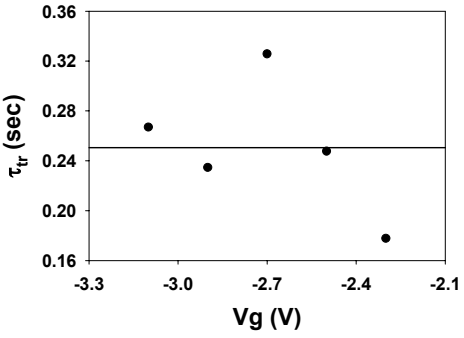

Figure 4.15: The fit constant τ_{tr} related to charge trapping as a function of V_g, in the refined model of Nigam.

4.5.2. SILC-related parameters

In figure 4.16 and figure 4.17, the SILC-related parameters are plotted. Since the SILC is one-to-one related to the trap generation in the oxide, especially at low injected fluence, both α and ν provide information on the stress-induced trap generation. α is the leakage current caused by the traps generated after 1 sec and ν is the trap generation rate. This fit parameter shows an exponential decrease as the applied gate voltage V_g decreases, as a consequence of the trap generation density dependence on the field stress applied during oxide degradation. The trap generation rate ν, as a function of V_g, is nearly a constant value as observed in literature [Nigam99].

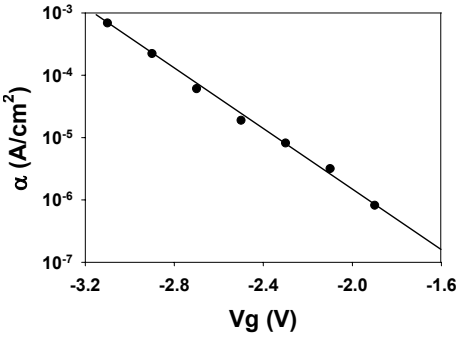

Figure 4.16: The fit constant α related to SILC as a function of V_g, refined model of Nigam.

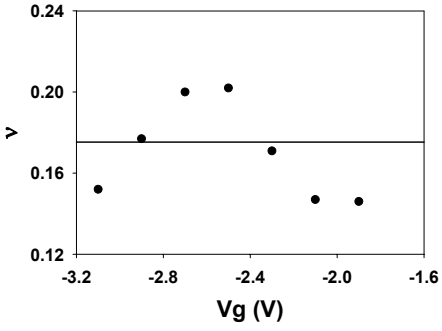

Figure 4.17: The fit constant ν related to SILC as a function of V_g, refined model of Nigam.

4.6. Validation of the model in the complete time frame of stress

As shown in the previous chapter a complete new experimental system setup has been developed to monitor small current changes at high speed of the order of 10 microseconds.

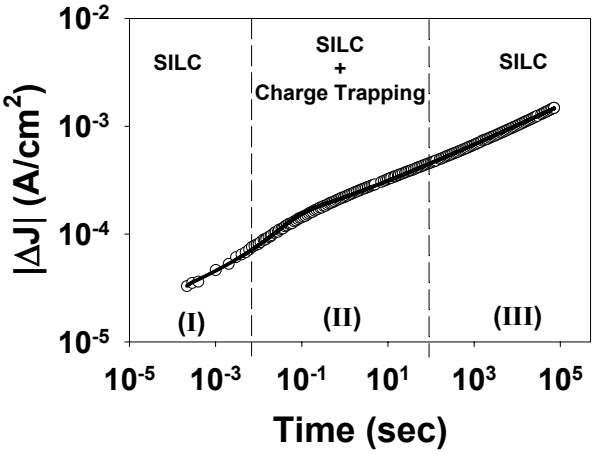

Figure 4.18. Dots: Current density as a function of time at V_g = -2.9 V. Lines: fit with the new procedure.

This is important in order to determine the on-set of trapping so that the individual contributions of SILC and trapping can be distinguished in the complete time-frame of stress and therefore a full validation of the proposed model is obtained. Figure 4.18 shows the current density as a function of time at V_g =-2.9 V together with the model fitting. In the first interval (I), the charge-trapping component is almost negligible and the increasing current corresponds to SILC, proving that the model is also valid in this region. In the second interval (II), the trapping effect is superimposed on the straight-line SILC behaviour and in the last interval (III), the current increases due to SILC.

4.7. Conclusion

The refined model of Nigam is able to describe the gate current behaviour over a broad stress voltage range.

An alternative method for the determination of the fitting constants has been developed, fitting the current's derivative instead of the actual current density. The derivative *dJ/dt* shows significant scattering particularly during the initial period of the measurement. A smoothing method, based on least structure method of Cook is applied to the original measured data before taking the derivative. Through the use of an appropriate model, it has been proved that SILC-related parameters and trapping-related parameters can be quantified.

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5. High resolution HC measurement technique

5.1. Introduction

Performing high-resolution hot-carrier measurements on high power devices is not straightforward. During this work, the test bench has to be protected from environmental influences. In section 5.2, the devices under study will be described and the degradation parameters are defined. Then the measurement set-up is presented (section 5.3). In section 5.4 the measurement procedure will be explained in detail. The stability of the power supply and the temperature (section 5.5) contribute to the high-measurement resolution of the in-situ technique [In-situ90]. In the last section, conclusions will be drawn.

5.2. Devices under study

The general structure of enhancement MOSFETs cannot be used in high power applications. The drain current of an n-channel MOSFET in the saturation region is defined as:

$$I_{d,sat} = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)\left(V_{gs} - V_t\right)^2 \tag{5.1}$$

where V_{gs} is the gate voltage, V_t the threshold voltage, μ_n is the electron mobility, C_{ox} the oxide capacitance, L the channel length and W the channel width. A high value of W and a short channel length (L) is necessary to increase the maximum drain current in saturation regime. Unfortunately, the use of short channels reduces the breakdown voltage of standard MOSFETs. The inverted drain-body region extends to the short channel leading to breakdown at low voltages. For this reasons new structures have been developed to achieve high voltage and high current levels.

The DMOS structure can have a very short channel and does not depend on a lithographic mask to determine the channel length. The structure has good punch-through control because of the heavily doped p-shield. The lightly doped drift region minimizes the voltage drop across the region by maintaining a uniform field to achieve velocity saturation. The field near the drain is the same as in the drift region, so avalanche breakdown, multiplication, and oxides charging are lessened, compared to conventional

MOSFETs. However, the threshold voltage V_t is more difficult to control in a DMOS technology. V_t is determined by the maximum doping concentration $N_{A,max}$ along the semiconductor surface. Varying $N_{A,max}$ leads to variation in V_t. The localization of punch-through control to a thin p^+ shield region requires a higher doping level, which leads to slower turn-off behaviour for DMOS transistors. Despite the different layout, DMOS shows characteristics similar to the standard MOSFET transistors. In saturation region, the drain current follows the same quadratic dependence with the gate voltage (equation 5.1).

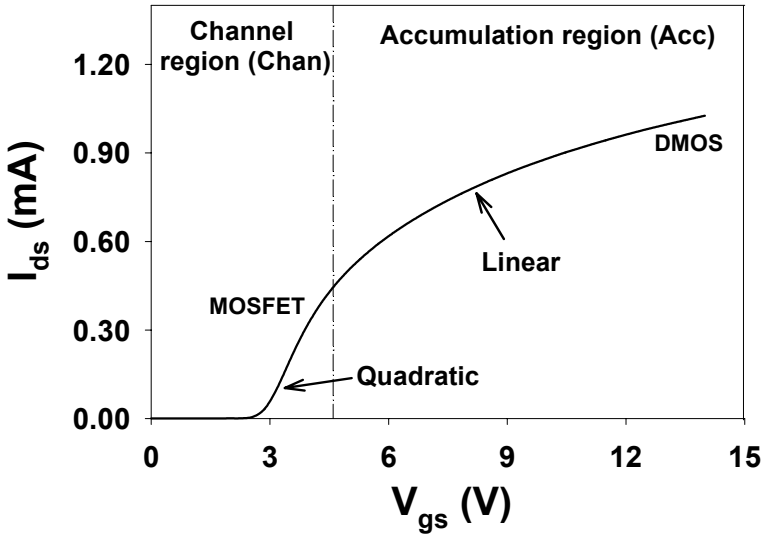

Figure 5.1: Typical I_{ds}-V_{gs} characteristic for a power MOSFETs.

However, as shown in figure 5.1, the I-V characteristic becomes linear at high gate voltage due to the presence of the accumulation or drift region. The carrier velocity saturates and the drain current becomes:

$$I_{d,sat} = \frac{1}{2} W C_{OX} U_{sat} \left(V_{gs} - V_t \right) \tag{5.2}$$

where U_{sat} is the saturated carrier velocity (5 10^6 cm/s for electrons inside the silicon). The linear region implies a constant transconductance (g_m) due to the saturated carrier velocity. g_m depends on the width (W) and it's generally elevated for power devices.

The devices used in the present study are lateral DMOS transistors processed in a 0.7 µm CMOS based smart power technology (fig. 5.2) [Ballan99]. The devices have a field oxide in the drift region. The channel implant is self-aligned to the poly gate. The gate oxide thickness is T_{ox}= 42 nm, V_t= 2.4 V, V_{bd}= 54 V and the specific on-resistance R_{on}= 90 mΩ*mm^2.

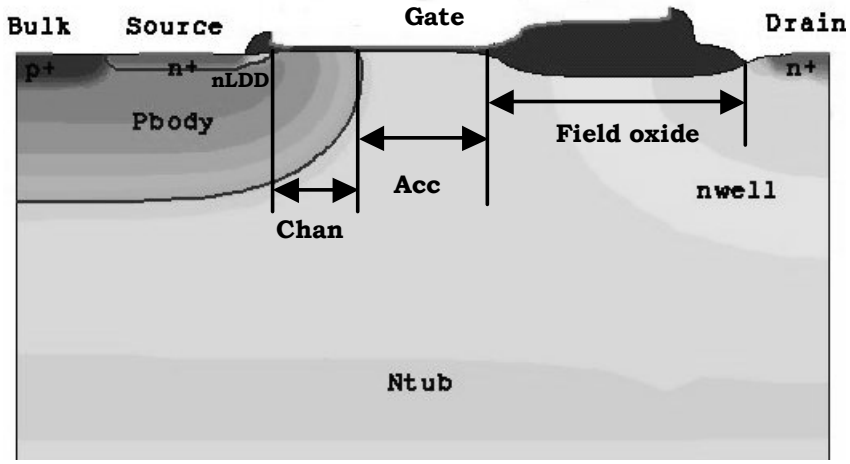

Figure 5.2: Schematic overview of the lateral DMOS transistor processed in a 0.7µm CMOS based smart power technology.

5.2.1. The characterisation parameters

As it's the case with devices based on field effect, the oxide degradation of the DMOS transistor, due to the injection of hot-carriers, leads to a deformation of the electrical characteristics that has a negative influence on its function in the IC. When a certain level of oxide degradation is reached, the device is unable to execute its function and as a consequence, the total IC will fail. When the reliability of the device under stress (DUT) is tested at operating conditions, the oxide degradation occurs very slowly and it can take many years to determine its lifetime, therefore, it is necessary to use accelerated ageing. During an accelerated in-situ ageing test, there will be continuously switched between measurement and stress. During measurement, certain parameters of interest of the DMOS are determined from the I-V characteristic and used to monitor the physical behaviour of the device under test. During stress, a high drain/gate voltage is applied in order to accelerate the oxide degradation. As a result of the test, the degradation

behaviour of the parameters as a function of stress time is obtained. The lifetime of the DUT is defined as the time where the parameter drift exceeds a predefined failure criterion. With the aid of an appropriate lifetime model, the lifetime at operating conditions can be extrapolated.

5.2.1.1 Linear region

In the linear region the linear drain current ($I_{d,lin}$) is measured and the transconductance ($g_{m,max}$) and the threshold voltage (V_t) extrapolated from the transfer characteristic. Figure 5.3 shows the I_{ds} - V_{gs} characteristic at V_{ds}= 0.5 V, as measured on a packaged DMOS transistor. The dotted line shows the derivative of the I_{ds} - V_{gs} characteristic.

- The maximum transconductance $g_{m,max}$ (unit: mA/V) is defined as the maximum value of the dotted line (fig. 5.3).
- The linear drain current $I_{d,lin}$ (unit: mA) defines the drain current I_d at drain voltage V_{ds}= 0.5 V and gate voltage V_{gs}= 12 V.
- V_t can be defined as the gate voltage V_{gs} at a predefined current level (I_d= 0.4 µA). V_t can also be extrapolated as the intersection of the tangent line at $g_{m,max}$ with the V_{gs}-axis. V_{ds}/2 has to be subtracted from the obtained value.

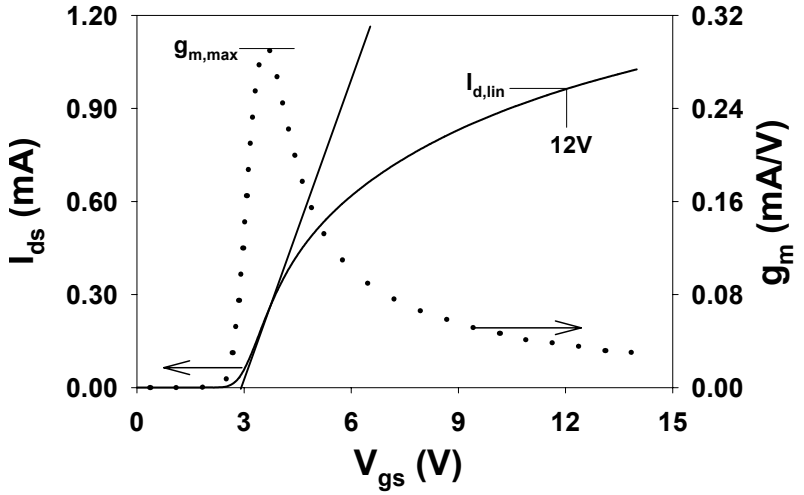

Figure 5.3: I_{ds}-V_{gs} characteristic at V_{ds}= 0.5 V in the linear region measured on a packaged DMOS.

5.2.1.2 Saturation region

In the saturation region, the saturation drain current is measured. Figure 5.4 shows the I_{ds} - V_{gs} characteristic at V_{ds}= 30 V, as measured on a packaged DMOS transistor.

- The saturation drain $I_{d,sat}$ (unit: mA) is defined as the drain current I_d at drain voltage V_{ds}= 30 V and gate voltage V_{gs}= 5 V. The substrate current I_{sub} (unit: mA) can be measured instead of $I_{d,sat}$ if the device has separated bulk and source terminals.

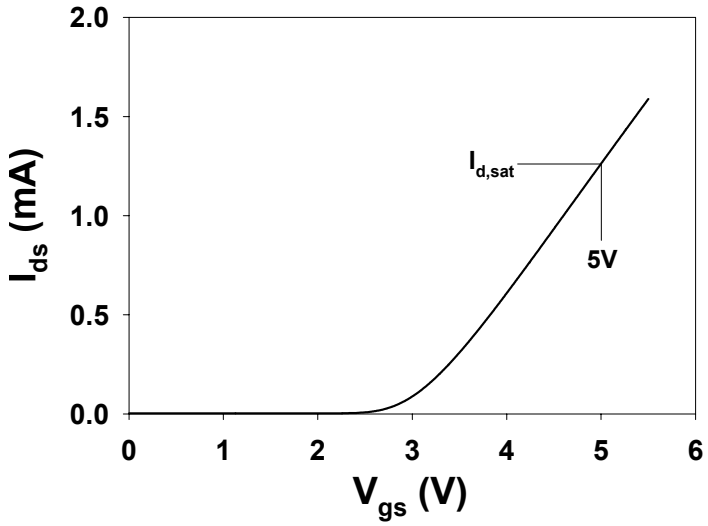

Figure 5.4: I_{ds}-V_{gs} characteristic at V_{ds}= 30 V in the saturation region measured on a packaged DMOS.

5.2.2. Interface characterisation by Charge Pumping (CP)

Besides the substrate current characteristic, the *Charge Pumping (CP)* technique is frequently used to study the degradation due to hot-carrier injection. CP consists of applying a pulse train with a certain amplitude (ΔV_A) and base level (V_{base}) at the gate of the transistor, while a small reverse bias (V_r) is applied at source and drain. If the gate pulses drive the channel continuosly in inversion and in accumulation, a recombination process occurs at the interface traps between carriers from the source and the drain and carriers from the substrate. As a result, a substrate current is generated, which is directly

proportional to the interface trap density, the transistor gate area and the frequency of the gate pulses [Wang92] [Here89]. Van den bosch and co-workers [Gvdb04] have performed complementary charge pumping measurements to confirm and provide more information on the location of the hot carrier damage on the device under test. The CP characteristic can be calculated by determining the local conditions for inversion and accumulation over the thin oxide region of the lateral DMOS transistor. This is done with the standard equations for the MOS system, the surface potential versus gate voltage relation. The input parameters, oxide thickness and surface dopant concentration, are extracted from calibrated TCAD process simulation. The result is two variables V_{g_e} and V_{g_h}, defined as the gate voltages needed to induce respectively an electron and hole concentration of $10^{14}/cm^3$ at the Si-SiO_2 interface, necessary to enable the CP phenomenon (fig. 5.5) [Here89].

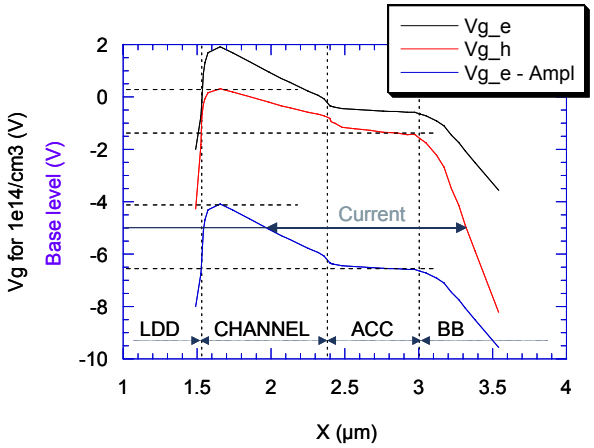

Figure 5.5: Variation of essential CP quantities over thin oxide region [Gvdb04].

Mainly because of the lateral variation in doping profile, V_{g_e} and V_{g_h} are smoothly varying over the different transistor regions as indicated in figure 5.5. The strong drop at the left is due to the high doping level in the LDD, the drop at the right is due to the thick oxide in the source-side bird's beak region (BB). A given location X contributes to the CP signal as long as accumulation and inversion is locally reached, i.e. the low (base) level of the gate pulse is below V_{g_h}, and the high level is above V_{g_e}. In terms of gate pulse base level and amplitude (taken as 6V), the second requirement becomes $V_{bl} > V_{g\_e}$ – Ampl. With this last parameter introduced, the y-axis of figure 5.5 can be interpreted as

the base level axis of the CP characteristic. The different regions in the lateral DMOS transistor are now linked to a range in V_{bl} of its CP characteristic.

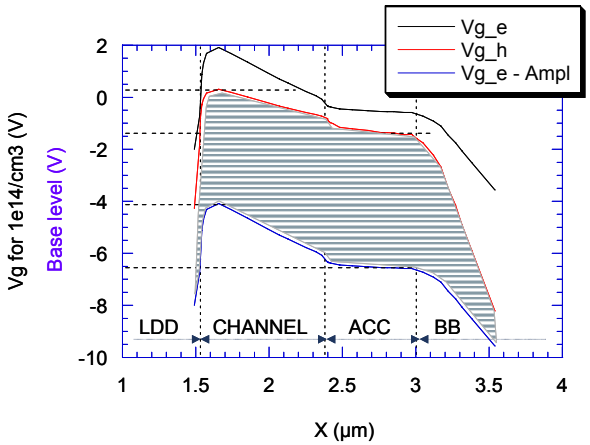

Figure 5.6: Graphical representation of the I_{cp}—V_{bl} characteristic [Gvdb04].

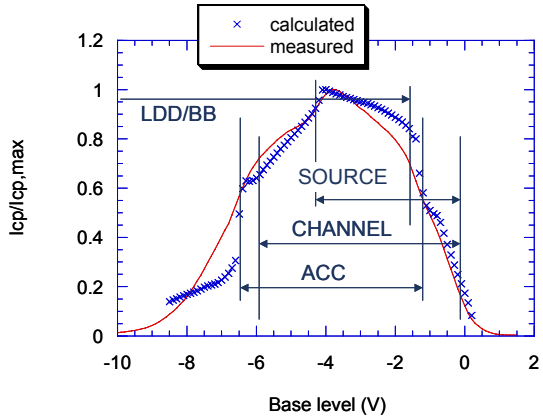

Figure 5.7: Comparison of measured and calculated CP characteristic (normalized to maximum). Identification of different regions responsible for the various CP signal features. SOURCE is the region of the device where V_{g_e} and V_{g_h} reach their maximum, and as such is part of the CHANNEL region [Gvdb04].

For example, the gate controlled accumulation region (ACC) reaches from approximately V_{bl}= -6.5V till approximately V_{bl}= -1.5V. In addition, the part of the device that

contributes to the Icp current at given V_{bl} is given by the length of the X-interval enclosed by V_{g_e} – Ampl and V_{g_h}, as indicated by the arrowed line in figure 5.6. The calculation of the I_{cp}-V_{bl} curve is then in essence nothing else than determining the length of this line (or these lines) at each V_{bl}, as schematically illustrated in figure 5.7. The underlying assumption is that interface trap density Dit is constant throughout the thin oxide region, a condition that is not necessarily fulfilled but is good enough as first approximation.

5.3. The measurement-setup

Figure 5.8 gives an overview of the different hardware components of the hot-carrier reliability test system. 4 dedicated *burn-in boards (BIB)* are mounted in the furnace, each one connected to one of the 4 *Programmable Power Supplies (PPS)*. A BIB can contain up to 6 DIL-28 ZIF sockets, in which the DUTs are placed. Each DUT can contain 2 transistors and one p-n junction to monitor the temperature. With this basic set-up, 48 devices can be measured at four different stress conditions. The gate, source and substrate contacts are common for each BIB, while only the 2 drains have different individual contacts.

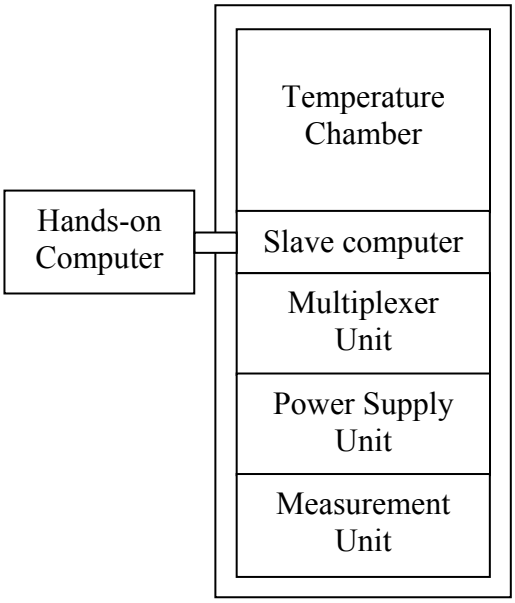

Figure 5.8: schematic overview of the main parts of the measurement set-up.

5.4. Measurement procedure

5.4.1. Handling of the samples

Special precautions have been taken to avoid unwanted Electrostatic discharge (ESD) on the sample during handling. ESD is an important problem in VLSI technology and can be confused with many other oxide damages. The use of special input protection circuits virtually eliminates the concern about instabilities due to low-level ESD stress at the gate.

However non-catastrophic ESD stress can be still possible and samples should be handled with extreme care. A general shift of the linear drain current due to ESD can be observed during hot carrier degradation leading to an error in the lifetime extrapolation of the devices under study. Figure 5.9 shows an example of two measurements on two identical samples with and without the effect of electrostatic discharge [Wang92].

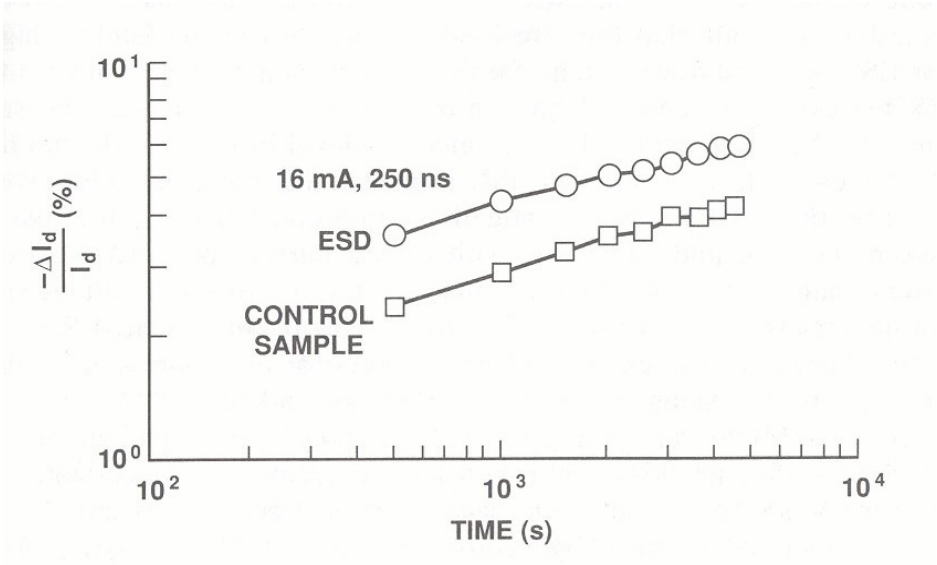

Figure 5.9: Linear drain current shift due to the electrostatic discharge [Wang92].

Moreover, many external contaminations can cause electrochemical reactions, which can reduce the measurement resolution due to increase of noise level. Therefore, the test structures are stored in a special box and during the mounting into the sample holder they are handled with antistatic gloves [Manca94].

The 4 dedicated burn-in boards (BIB) are designed to avoid electrostatic discharge. The device is grounded when it's inserted inside the socket of the BIB and when the burn-in board is mounted inside the oven.

5.4.2. The measurement cycle

Initially, all devices are in the off state, i.e. drain and source are short-circuited and no voltage is applied to the drain and the gate ($V_d = V_g = 0$ V). Next, the hot-carrier experiment starts by stressing ($V_d \neq 0$ V; $V_g \neq 0$ V) the different MOSFETs during a certain time interval Δt, followed by a measurement of all the different degradation parameters (P1, P2, …Pi). This stress/measurement sequence is repeated several times, while the duration of the stress time interval is increased on a logarithmic time scale. In practice, the way of stressing the devices depends on the duration of the stress time interval Δt, which varies from milliseconds (shortest stress time is ± 30 ms) to several hours. For short stress times, the different transistors are sequentially stressed, i.e. each sample is individually stressed during a short time one after the other. For long stress times on the other hand, parallel stressing will be used, i.e. the stress is switched on for all the samples more or less simultaneously during a long time interval and afterwards also switched off simultaneously. After stressing, all the devices are measured sequentially. The introduction of the parallel stress mode reduces the test time, which could be too long using sequential stress mode, considering the large number of samples under study. However, in case of oxide damage of one transistor under parallel stress, a short circuit on the gate can lead to overflow of the gate power supply. The voltage drop on the gate of the damaged transistor leads to a voltage drop on all the transistors in the parallel circuit. For this reason, all the transistors are characterized before stress and excluded from the test measurement in case of damage.

5.5. Performance of the measurement system

5.5.1. Power supply stability

The power supply unit consist of 4 Programmable Power Supplies (PPS). Each of them contains two voltage sources. The drain voltage can be regulated between –100 V and +100 V with a maximal current of 100 mA. The gate voltage can be regulated between –20 and +20 V with a maximum current of 100 mA. The PPS, which is controlled by a digital I/O card and a timer I/O card in the slave computer, provides the voltage stress to the drain (V_d) and the gate (V_g) of each DMOS. The drain and gate voltages are

continuously monitored using a high precision $6^{1/2}$ digits multimeter and used in a software feedback loop (fig. 5.10) to keep both voltages V_d and V_g stable at a constant value (fig. 5.11). A memory card contains all the necessary control and timer hardware of the dual power supplies.

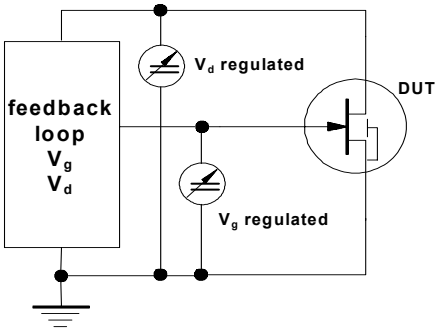

Figure 5.10: Constant voltage mode configuration.

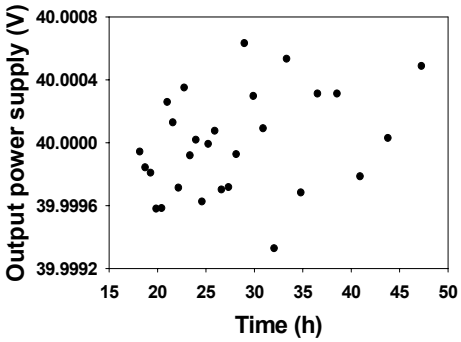

Figure 5.11: Resolution of the power supply during a test measurement.

5.5.2. High temperature stability

Temperature fluctuation is an important factor that can influence the measurement resolution. When the DUT degrades, the change in property is given by:

$$\Delta P(t) = \Delta F(t) + TC\Delta T \tag{5.3}$$

where F is an unknown degradation model which is a function of the stress time t and ΔF is the change for a given time interval and ΔT is the correspondent change in temperature. The temperature coefficient (TC) can be determined from a characterization measurement (ΔF=0) so that the observed parameter change is due to the temperature fluctuations [D'Haeger93]. Figure 5.12 shows the plot of $\Delta I_{d,lin}$ versus ΔT. A straight line is obtained and the TC is defined as the slope of this line. A TC of 1758 ppm/°C is obtained. The DUT is placed in a protective chamber and the temperature inside is stabilized. Figure 5.13 shows the temperature behaviour of the system with a set point of –30 °C, resulting in a temperature stability of 0.03 °C. In this case, the maximum parameter change due to temperature fluctuations is around 50 ppm.

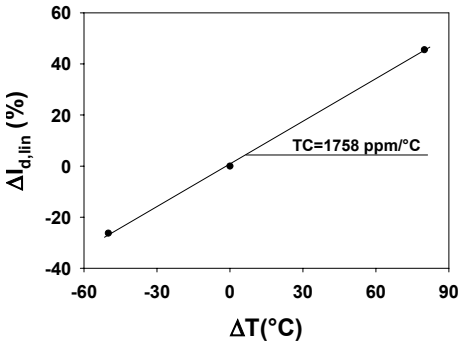

Figure 5.12: $\Delta I_{d,lin}$ versus ΔT to determine temperature coefficient (TC).

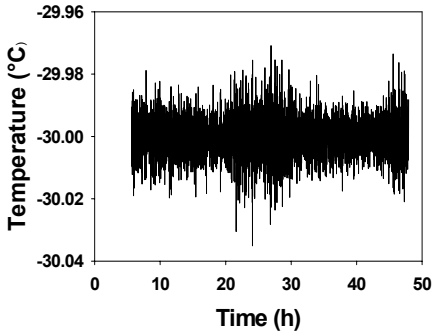

Figure 5.13: Temperature stability of the oven with a set point of –30 °C.

5.5.3. Self-heating issues

New characterisation and measurement techniques have to be developed to analyse the hot carrier degradation behaviour of power devices. The standard CMOS characterisation technique is not applicable to the integrated power transistors, due to the self-heating effect as a consequence of the higher power.

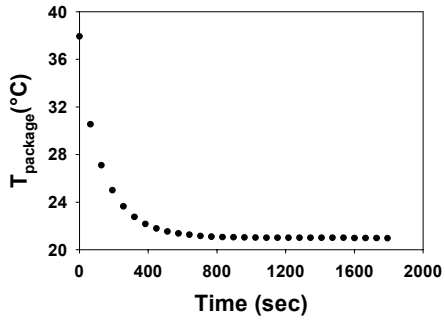

Figure 5.14: Temperature of the package after one stress cycle.

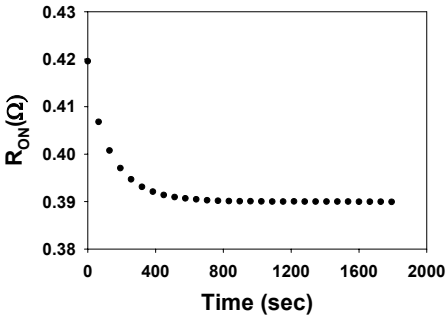

Figure 5.15: R_{ON} of the device after one stress cycle.

Under high voltage stress the temperature of the package has clearly increased (fig. 5.14) leading to an error in the determination of the degradation parameter (i.e. R_{on}, fig. 5.15). For this reason, after each stress cycle the device parameters are measured with a delay,

defined as the time necessary for the package to cool down to the temperature set point of the ambient. For lateral DMOS transistors the delay is usually set to 30min.

5.6. Measurement resolution

Until now, the measurement resolution of 0.5 % in traditional high power test benches allows a failure criterion of 10 % for this technology. A degradation of 0.5 % implies that a lot of damage has already occurred in the oxide or in the silicon-oxide interface. The new high-resolution HC multi-sample test bench is able to measure small changes as low as 0.01 % and it allows us to lower the failure criterion value to 1% if necessary. This high resolution allows precise prediction to operating conditions and improved modelling. Different factors are needed to obtain the desired high measurement resolution. Dense measurements around a small region instead of complete I_{ds}–V_{gs} characteristic are performed during the extraction of the desired degradation parameters. The stability of the power supply, the stability of the temperature (external and junction temperature) and the highly accurate measurement unit finally leads to a stability of around 0.02% as shown in figure 5.16.

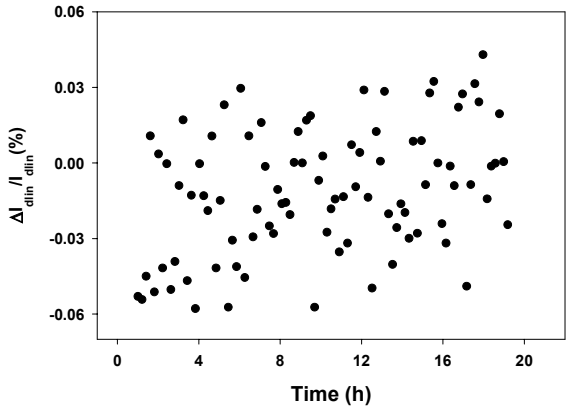

Figure 5.16: Linear drain current stability during a test measurement at $V_g=V_d=0V$.

5.7. Conclusion

In this chapter, the HRMT is proposed in order to perform high-resolution hot-carrier measurement on power DMOS technology.

The in-situ accelerated ageing technique with electrical testing was developed to study hot-carrier degradation on LDD MOSFETs devices [Dreesen99], [In-situ90]. In this work the technique will be used to extend hot-carrier degradation analysis on power devices. The experience obtained using the in-situ measurement in numerous different applications gave us the possibility to keep the same high-resolution measurement obtained on hot-carrier degradation of MOSFETs at room temperature but to handle higher voltages and high power.

The advantages of using such measurement are:

- Test time can be reduced.
- Measurement at high-resolution and stress condition can be lowered in comparison to the measurement performed with other techniques.
- Measurement at operating conditions can be performed allowing more confident prediction.
- Better modelling is obtained.

5.8. Reference of the chapter

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6. Hot-carrier degradation of power DMOS devices

6.1. Introduction

In this chapter the analysis of the hot carrier injection behaviour of a high voltage lateral nDMOS technology is presented. Recent work [Wang92], [Moens01] tries to describe the effects of hot electron/hole injection in the channel region and/or the gate controlled drift region of DMOS transistors. The first mechanism is attributed to decreased electron mobility due to increased carrier scattering upon D_{it} formation at the drain end of the channel or beyond, whereas the second mechanism occurs in the gate overlapped drift region of the device and is due to *hot-hole injection (HHI)* and trapping. The competition of both mechanisms depends strongly on the stress conditions. In this work, we will analyse in detail these mechanisms and we will prove that *Source Side Injection (SSI)* takes place under high stress conditions, which leads to rather moderate changes of the linear drain current ($I_{d,lin}$) but significant changes of the saturation drain current ($I_{d,sat}$) and the threshold voltage (V_t). In the first section the devices and experiments are described. It will be shown that upon hot carrier stress, three different and competing hot carrier related degradation mechanisms occur. The mechanisms could be identified by analysis of the electrical data and by performing Charge Pumping (CP) experiments on the DMOS device with separated bulk and source connections. Detailed TCAD simulations were also performed, supporting the proposed degradation mechanisms. The experimental results will be discussed giving a clear evidence for the existence of a source-side injection degradation component (section 6.2). An overview of the most used models will be proposed and among them the best suitable models will be adapted and used to describe the behaviour of the lateral DMOS transistor (section 6.3). Finally in the last section we draw some conclusions.

6.2. Hot carrier degradation mechanism on power DMOS device

High drain voltages up to V_d= 40 V and high gate voltages up to V_g= 15 V are applied in order to accelerate the hot carrier degradation. The linear drain current ($I_{d,lin}$), the saturation drain current ($I_{d,sat}$), the transconductance ($g_{m,max}$), the extrapolated threshold voltage ($V_{t,e}$) and the threshold voltage measured at constant current ($V_{t,cc}$) (I_d=400mA) have been monitored continuously to analyze the physical degradation mechanisms of the DMOS transistors (see chapter 5). Each parameter degrades in a different way depending

on the applied stress voltage, allowing us to distinguish the contribution of the different degradation mechanisms. Figure 6.1, 6.2 and 6.3 show the degradation parameters of two identical Lateral DMOS transistors stressed at V_d= 40 V and V_g= 15 V.

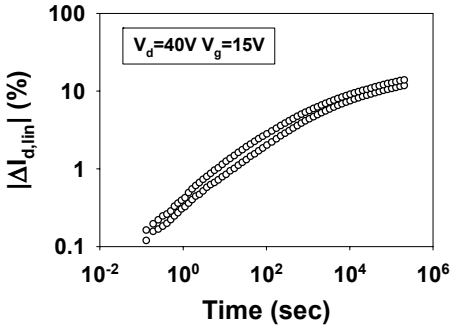

Figure 6.1: Linear drain current degradation during stress of two LDMOS transistors at V_d=40 V and V_g=15 V.

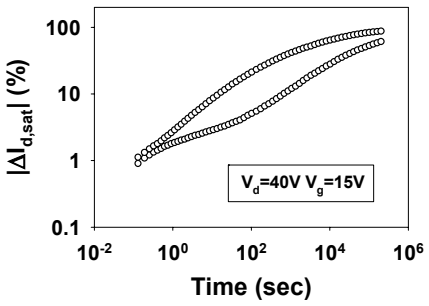

Figure 6.2: Saturation drain current degradation during stress of two LDMOS transistors at V_d=40 V and V_g=15 V.

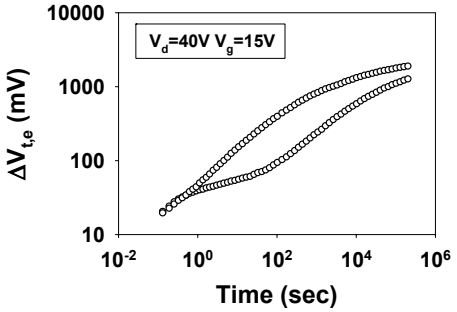

Figure 6.3: Extrapolated threshold voltage shift during stress of two LDMOS transistors at V_d=40 V and V_g=15 V.

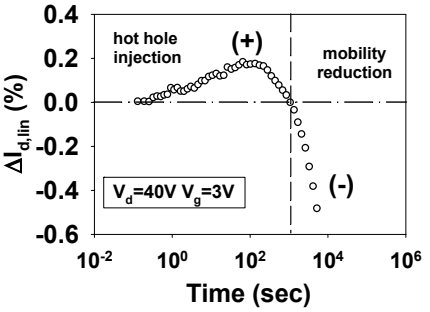

Figure 6.4: Linear drain current degradation during stress at V_g=3 V and V_d=40 V.

The linear and the saturation current are plotted in absolute value. $I_{d,lin}$ decreases with time and saturates. $I_{d,sat}$ also decreases with a much larger drift, which is also reflected in a positive shift of the threshold voltage in the order of 1-2 V. Also a statistical spread for the $I_{d,sat}$ and V_t parameters is observed. Out of these experimental observations, it is evident that at least two different degradation mechanisms occur in the LDMOS transistor at high drain voltage and high gate voltage. At low gate voltage (V_g < 3 V), an

initial increase of the linear drain current can be observed after short stress time (fig. 6.4), giving rise to another degradation mechanism as shown in more detail in the next sections. The activation of the three degradation mechanisms is manly due to the applied gate voltage level. The mobility reduction and the hot hole-injection increase at higher drain voltage. However, source side injection is relatively insensitive to the drain voltage.

6.2.1. Substrate (I_{sub}) and gate current (I_g)

If the lateral electric field is sufficiently high, strong carrier heating occurs and the average electron energy rises above the thermal energy of the lattice. Some electrons can create an electron-hole pair by impact ionisation. During device operation, the holes generated can be monitored as a substrate current. Compared to a standard MOSFET, the substrate current of a power DMOS transistor does not have the typical bell-shape due to a second impact ionisation spot (fig 6.5).

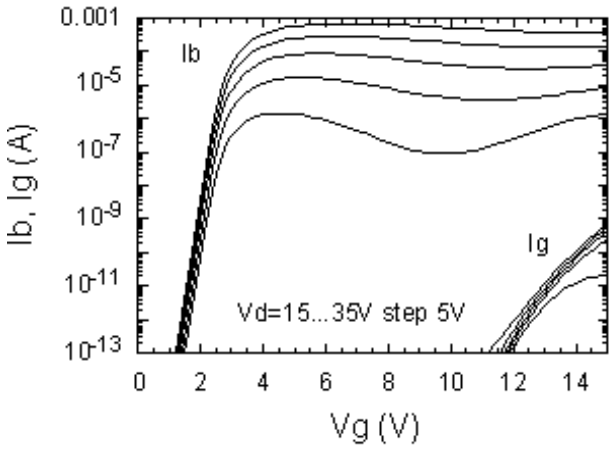

Figure 6.5: Substrate and gate currents as a function of gate voltage for various drain voltages (15, 20, 30 and 35 V).

The substrate current increases with the gate voltage, due to a first impact ionisation spot at the p-body/Ntub interface, located at the beginning of the accumulation region. The maximum I_{sub} is at around V_g= 4 V. At high gate voltage I_{sub} remains relatively high as a result of a second impact ionisation spot at the transition Ntub/n-well/n^+-drain, due to the presence of the Kirk effect, which alters the space charge distribution and pushes the potential lines towards the drain region [Sze81]. Once the space charge region reaches the

highly doped drain region a second electric field peak develops at the drain side, giving rise to an additional source of impact ionisation. The magnitude of the Kirk effect and hence the presence of the second impact ionisation spot at the drain side is related to the total current density and is thus dependent on the drain/gate voltage applied. However, the only impact ionisation spot important for the degradation is the first one in the beginning of the accumulation region, where the current is close to the interface. The second spot is near the drain side bird beak, where the current avoids the Si-SiO_2 interface. Hence any carrier injection at this side does not affect the current flow and cannot be detected from the shift in the electrical parameters [Moens01]. At high gate voltages a third impact ionisation spot occurs at the source side of the channel in the nLDD region. The substrate current (fig. 6.5) shows a clear drain voltage dependency. However, this third mechanism is relatively independent from the drain voltage. Therefore, the contribution of this effect to the total substrate current is secondary compared to the impact ionisation at the drain side and cannot be seen in the I_{sub} plotted in figure 6.5.

The gate current (I_g) is another important parameter that represents a direct measure of the injection of carriers into the oxide. It consists of those carriers that have enough energy to overcome the Si-SiO_2 barrier. At low gate voltage, when the vertical electric field favours hole injection towards the gate, the gate current nearly matches the injected hole current. Only a small number of injected holes is scattered back to the interface. For larger gate voltage, electron injection dominates [Wang92]. As long as the surface potential at the injection point is larger than the gate voltage, injected electrons are scattered back to the interface by the repelling oxide electric field, unless the oxide is very thin. However, an electron gate current is expected for very high gate voltage. During operation at normal bias conditions, the gate current is extremely small and direct measurement becomes difficult. Different methods have been developed in the last few years mostly based on floating gate transistors that allows sensitivities of 1 aA (10^{-18} A). At high gate voltages the gate current is high enough to be measured by means of an electrometer. The measurement of gate current is essential to study the hot carrier degradation behaviour of the transistor. Moreover, further evidence of source side injection is found as shown on figure 6.5. A clear electron current is measured at high gate voltages at the same conditions where the large V_t-shift is observed. The I_g is relatively insensitive to the drain voltage, which supports the idea that the electron injection is at the source side, due to the high vertical electric field in this region.

6.2.2. Mobility reduction (MR)

Mobility reduction is due to interface state generation in the gate oxide of the transistor. The most important mechanism for the creation of interface traps involves hot carriers breaking the hydrogen bonds at the interface, releasing the hydrogen atom and leaving behind dangling Si- or O- bonds.

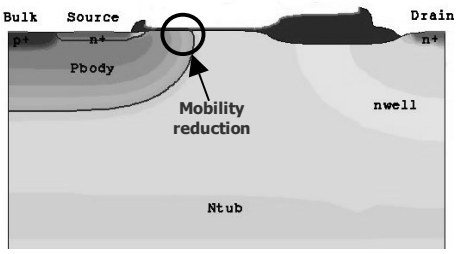

Figure 6.6: Schematic overview of the Lateral DMOS transistor channel, accumulation region and field oxide.

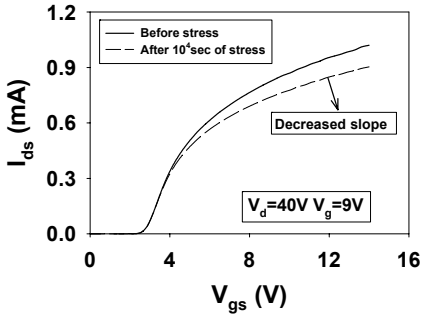

Figure 6.7: I_{ds}-V_{gs} characteristic before and after stress at V_g=9 V V_d=40 V.

These may easily acquire an electron when the device is in strong inversion and become negatively charged [Sah87]. Interface traps are in electrical communication with the conduction and valence bands of the silicon and thus can be charged and discharged, depending on the surface potential. The traps are localized at the drain end of channel in the accumulation region, because the lateral electric field accelerating the electrons and holes (created by impact ionisation) in the channel attains its maximum in the accumulation region, leading to localized injection into the Si-SiO_2 interface (fig. 6.6).

I_{ds}-V_{gs} characteristics are plotted in figure 6.7 before and after stress at V_d= 40 V and V_g= 9 V. At high measured V_{gs}, where the current is dominated by the drift region of the DMOS transistor, a drop in current can be observed leading to a change in the slope of the I_{ds}-V_{gs} characteristic. Hence the linear drain current (fig. 6.8) and the maximum transconductance (fig 6.12) decrease. At low measured V_{gs}, where the current is dominated by the channel part of the DMOS transistor, no horizontal shift of the transfer characteristic can be observed and the threshold voltage, measured in subthreshold region at constant current (I_d=400nA), is not affected (fig. 6.9). Due to the increased scattering of the carriers at the interface states, the mobility is reduced and the current will decrease.

As the current is decreased, the impact generation will decrease and so will also the bulk current.

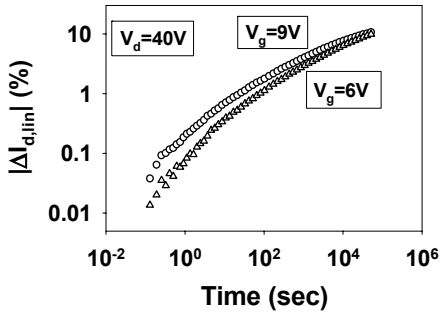

Figure 6.8: Linear drain current degradation during stress at V_g=9 V, V_g=6 V and V_d=40 V.

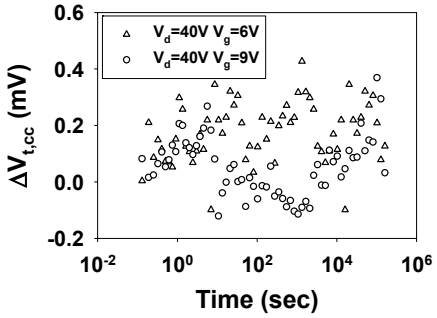

Figure 6.9: Threshold voltage shift measured at constant current (I_d=400nA) during stress at V_g=9 V, V_g=6 V and V_d=40 V.

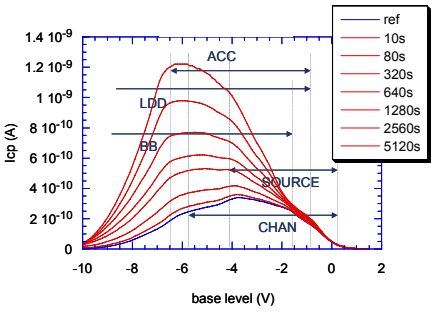

Figure 6.10: Icp signal during stress at V_g=6 V and V_d=40 V [Gvdb04].

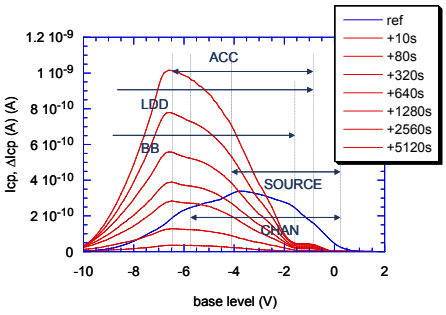

Figure 6.11: Differential Icp signal during stress at V_g=6 V and V_d=40 V [Gvdb04].

The carriers try to avoid the surface and follow a current path slightly deeper in the silicon. Thus, the creation of new interface traps is reduced and the effect of the traps on the current distribution is diminished. As such, a certain equilibrium condition is reached. This explains the saturation behaviour of the linear drain current [Moens01]. Charge pumping measurement was performed on the DMOS device after stress at V_g= 6 V and V_d= 40 V (fig. 6.10). The CP spectrum shows moderate left skew with almost no I_{cp} at

base level voltage $V_{bl} > -2V$. This is clearly seen in figure 6.11, where the differential signal is plotted. The creation of interface state (D_{it}) can be observed. The increased D_{it} is distributed suggesting spatially nonuniform interface trap formation. Neither the maximum of ΔD_{it} nor the rising edge does move appreciably, suggesting only limited charge trapping. The exact location of the damage is not easily deduced. What is known for sure is that it is away from the source, at the drain end of the channel or beyond [Gvdb04].

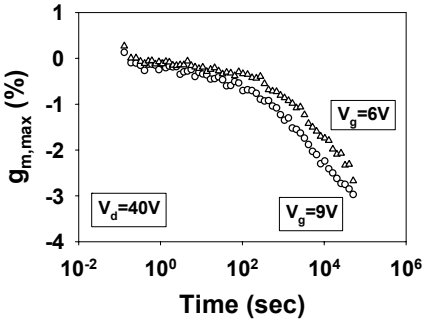

Figure 6.12: Maximum transconductance degradation during stress at V_g=9 V, V_g=6 V and V_d=40 V.

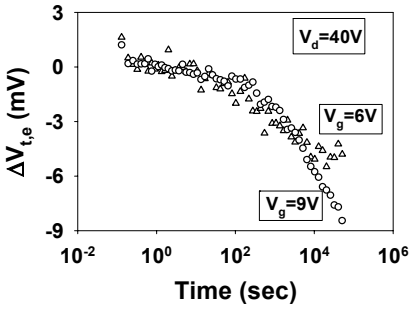

Figure 6.13: Extrapolated threshold voltage shift during stress at V_g=9 V, V_g=6 V and V_d=40 V.

Figure 6.13 shows the extrapolated threshold voltage at two different stress conditions V_g=9V, V_g=6V and V_d=40V. Compared to the V_t-shift at constant current (I_d=400nA) (fig. 6.9), the extrapolated V_t is not constant and slightly decreases with the stress time, as observed in the maximum transconductance (fig 6.12). This is due to the change in the slope of the I_{ds}-V_{gs} characteristic, which influences the extrapolated threshold voltage.

6.2.3. Hot-hole injection (HHI)

At low gate voltage ($V_g \leq 3$ V) and high drain voltage (V_d= 40 V), hot-hole trapping in the gate oxide of the accumulation region (fig. 6.14) is superimposed on the mobility reduction. This mechanism induces a recovering effect on the linear drain current with a consistent positive shift (fig. 6.15) and no effect on the threshold voltage measured in subthreshold region at constant current (I_d=400nA) (fig. 6.16).

From TCAD simulations performed by Moens at al. [Moens01] it follows that the electric field across the thin gate oxide changes sign in the accumulation region, becoming favourable for hole-injection (fig. 6.17). The maximum electric field is reached at the end

of the accumulation region i.e. at the beginning of the birds-beak. With the increase of the stress time, the injected holes create an opposing electric field forcing other holes to be injected in the gate oxide more towards the p-body. Also this second mechanism will vanish because the vertical electric field and the hole-energy are becoming too small when approaching the p-body.

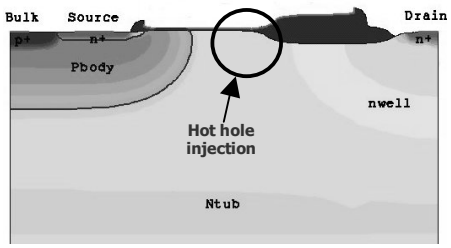

Figure 6.14: Schematic overview of the Lateral DMOS transistor channel, accumulation region and field oxide.

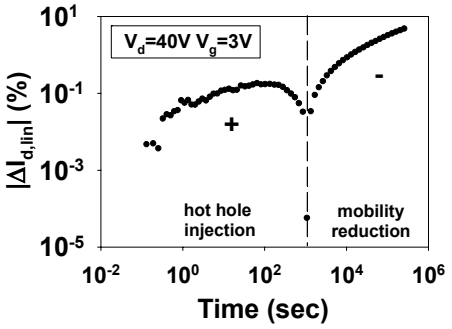

Figure 6.15: Linear drain current degradation during stress at V_g=3 V and V_d=40 V.

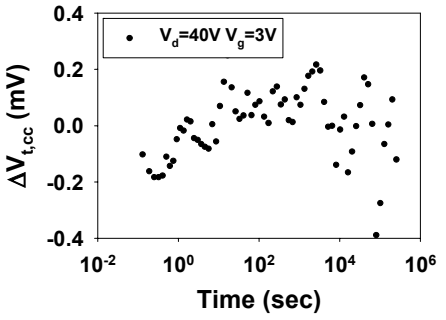

Figure 6.16: Threshold voltage shift measured at constant current (I_d=400nA) during stress at V_g=3 V and V_d=40 V.

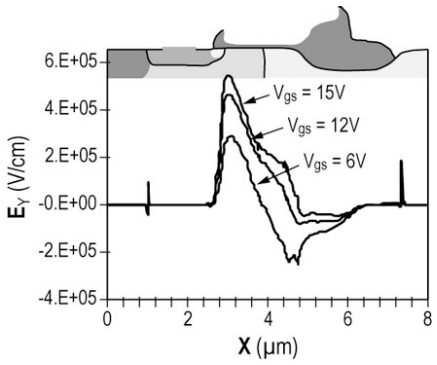

Figure 6.17: Hydrodynamic TCAD simulations showing the vertical electric field at the silicon surface for different Vgs (Vds=40V, Vgs=6V, 12V, 15V).

The recovering effect can be detected on the maximum transconductance, which slightly increases (fig. 6.18) due to the positive change in the slope of the I_{ds}-V_{gs} characteristic. This affects the extrapolated V_t, which is not constant and slightly increases with the stress time (fig.6.19). Charge pumping measurement was performed on the DMOS device

after stress at V_g= 3 V and V_d= 40 V (fig. 6.20). There is essentially no charge pumping current above V_{bl} = –3V. In addition the rising edge of the CP signal clearly shifts to lower base voltage levels with stress time, which is evidence for positive charge trapping. In the differential signal, the same trapping is also observed as the shift to lower V_{bl} of the negative part of the ΔI_{cp} (fig. 6.21).

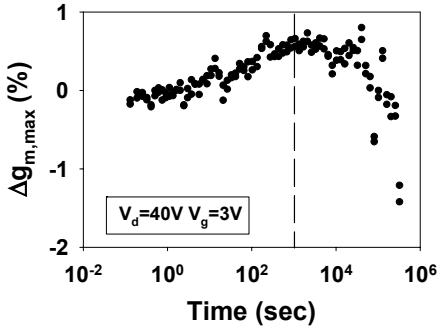

Figure 6.18: Maximum transconductance degradation during stress at V_g=3 V and V_d=40 V.

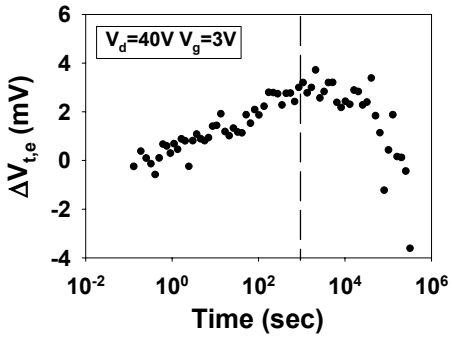

Figure 6.19: Extrapolated threshold voltage shift during stress at V_g=3 V and V_d=40 V.

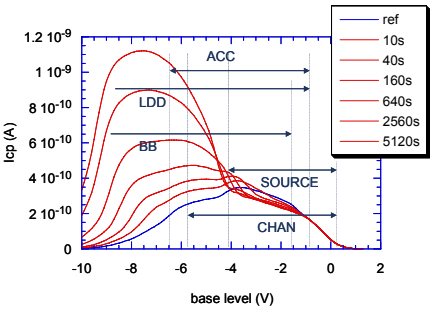

Figure 6.20: Icp signal during stress at V_g=3 V and V_d=40 V [Gvdb04].

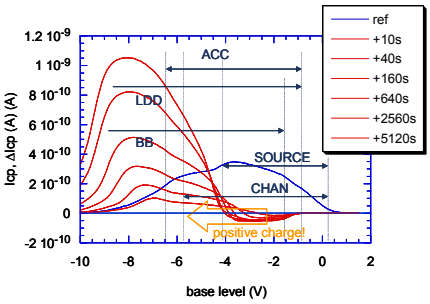

Figure 6.21: Differential Icp signal during stress at V_g=3 V and V_d=40 V [Gvdb04].

The negative increase in itself means that existing interface traps are located at another lower V_{bl} as a result of local positive charge trapping. At longer stress times the left-shift saturates, since the "normal" hot-carrier degradation mechanism must be acting as well. The ΔI_{cp} suggests that the location of the damage is outside the channel, i.e. in the accumulation region or under the bird's beak [Gvdb04].

6.2.4. Source Side Injection (SSI) effect

As already mentioned in chapter 2, the injection of carriers heated in the lateral electric field is one of the main reasons of performance degradation in MOS transistors. In order to minimize carrier heating, drain engineering has become a valuable tool. A successful example is the Lightly Doped Drain (LDD) structure. The basic idea of the nLDD implantation is to reduce the peak of the lateral electric field for a given power supply and technological node. This is achieved by avoiding the steep pbody-n^+ junction at the Si-surface by using a double implantation scheme. The peak lateral electric field decreases with smaller n^- implant dose and as a consequence much larger drain voltages have to be applied in order to obtain equal gate current levels. However, some unwanted effects needs to be taken in consideration. In recent works, too low nLDD doping level already revealed the presence of new harmful degradation mechanisms [Goo94]. Firstly, even a moderate amount of localized interface charge can significantly increase the series resistance and degrade the current characteristics. Moreover, during degradation at high gate voltage a large voltage drop and corresponding lateral field peak occurs at the source junction as a result of the large series resistance of the low n^- implantation region. Hot carriers are then generated at the source leading to additional degradation [Katto84]. Optimised nLDD structures have been reported to safely allow scaling of MOSFETs down to 0.7µm [Kakumu86]. By self-aligned processing, a spacer oxide is deposited above the lightly doped region for technological reasons, which is usually of minor quality as compared to the thermally grown gate oxide. It is well known that electron trapping can occur in this spacer oxide after stresses at large V_g. This negative charge influences the channel current, because the gate has a limited control over the underlying channel region. In some of today's most advanced drain engineered structures, the gate is given an inverse T-shape, in order to avoid contact between the spacer oxide and the nLDD region. Not only electron trapping can be eliminated, but also the enhanced gate control over the nLDD region results in an additional reduction of the lateral field. The nLDD structure is used also in lateral DMOS transistor at the source side of the channel to avoid the steep pbody-n^+ junction and to make contact with the channel. Above this second implantation a spacer oxide is deposited. At high gate voltage ($V_g \geq$ 12 V) source side injection (fig. 6.22) is superimposed on the mobility reduction. I_{ds}-V_{gs} characteristics are plotted in figure 6.23, before and after stress at V_d= 40 V and V_g= 15 V. At low measured V_{gs}, where the current is dominated by the channel part of the DMOS transistor, we observe a clear horizontal shift of the curves. As a result, a large drift of $I_{d,sat}$ and a large V_t shift can be detected. This effect is indicative for negative charge

generation at the source side of the channel [Wang92]. At high measured V_{gs} a drop in current can be observed as well, due to mobility reduction.

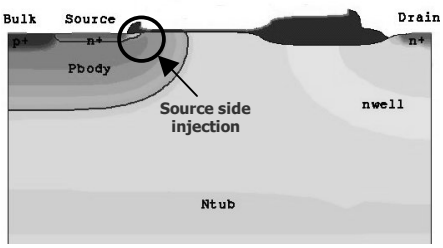

Figure 6.22: Schematic overview of the Lateral DMOS transistor channel, accumulation region and field oxide.

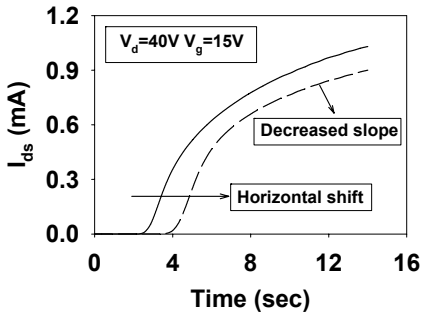

Figure 6.23: I_{ds}-V_{gs} characteristic before and after stress at V_g=15 V V_d=40 V.

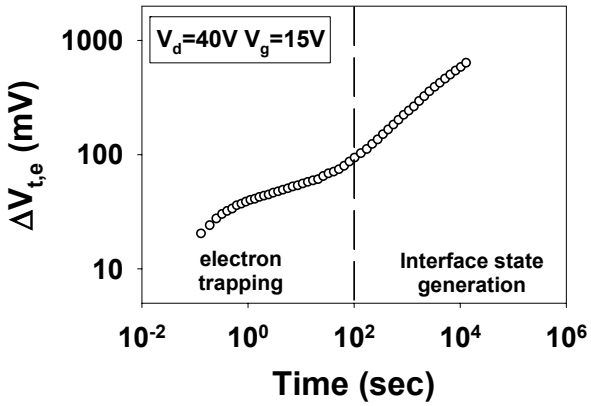

Figure 6.24: Extrapolated threshold voltage shift during stress at V_d=40 V and V_g=15 V.

Figure 6.24 shows the extrapolated V_t shift. As a result of electron injection at the source side, two degradation mechanisms can be distinguished in the complete time frame of stress. At first, $V_{t,e}$ increases with stress time and saturates. Under the applied drain voltage, electrons flow from the source into the channel through the nLDD implantation. It is possible that electrons (E_e=1.6eV), moving from source to drain by the high electric field, first create *avalanche plasma* by impact ionisation, consisting of generated

electrons and holes pairs. While most of the created electrons are attracted toward the drain, some electrons and holes in the avalanche plasma with sufficient kinetic energy (E_e=3.1eV, E_h=4.8eV) are injected into the gate oxide at the source side of the channel. The probability that some electrons can surmount the Si-SiO_2 potential barrier is also dependent on the vertical electric field and therefore determined by the gate bias [DiMaria93]. The higher vertical electric field leads to a lower potential barrier at the Si-SiO_2 interface and higher probability of electron injection into the oxide. Electrons injected into the oxide, can give rise to electron trapping and/or interface state generation. At this stage, the two degradation mechanisms at the source have a secondary importance and do not influence the device parameters. However, even a small amount of these defects can significantly increase the series resistance as a result of too low LDD dose [Katto84]. A voltage drop and corresponding lateral field peak at the source near the nLDD/pbody junction increases with the stresstime, due to the gradual increase of the series resistance of the low n^- implantation region. The local lateral electric field peak leads to higher injection probability due to the higher electron energy.

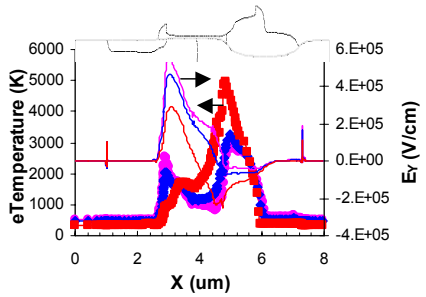

Figure 6.25: Hydrodynamic TCAD simulations showing the vertical electric field and the electron temperature at the silicon surface, for different Vgs (V_d=40 V: V_g=6 V (red), 12V (blue) and 15V (pink).

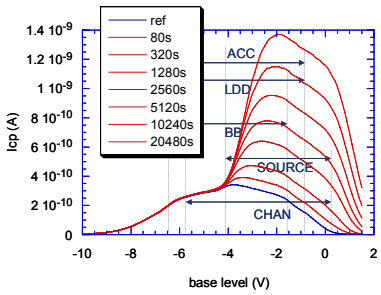

Figure 6.26: Icp signal during stress at V_g=15 V and V_d=15 V [Gvdb04].

Afterwards, the injected electrons create an opposing electric field, forcing other electrons to be injected in the gate oxide more towards the p-body. The resistivity of the n^- region increases with the oxide degradation and saturates with the increased stress time. As a consequence, the V_t-shift also saturates and the maximum transconductance slowly decreases. Electrons are then injected into the oxide at source side of the channel, where the vertical electric field reaches its maximum. Interface state generation occurs in

this region, giving rise to the large V_t-shift. TCAD simulations further support the analysis. Figure 6.25 shows the electric field and the electron temperature at the silicon surface for different V_g values (V_d=40 V). A vertical electric field peak at the source of the transistor is clearly present at high V_g. The electron temperature has two maxima, one at the source side of the channel, the other at the birds beak tip.

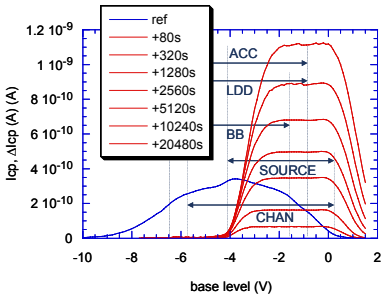

Figure 6.27: Differential Icp signal during stress at V_g=15 V and V_d=15 V [Gvdb04].

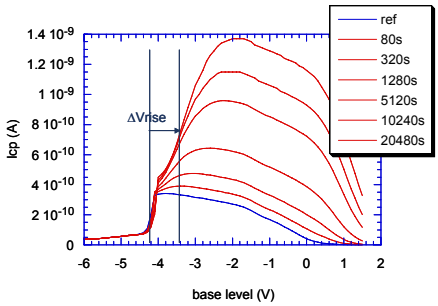

Figure 6.28: Variation in rising edge of the CP signal, during stress at V_g=15 V and V_d=15 V, measured with drain open [Gvdb04].

Charge pumping measurement was performed on DMOS device with separated bulk and source connections, after stress at V_g= 15 V and V_d= 15 V, i.e. well into the assumed SSI regime (fig. 6.26). The strong right skew of the stressed characteristics is apparent, with essentially zero added signal below –4V. There is clear evidence for D_{it} formation at the source. Despite the strong right skew of the added D_{it}, the contribution of charging must be limited since the rising edge of the "bump" does not shift much with stress time. This is even more clearly evidenced in figure 6.27, where the differential CP signal is plotted.

The almost ideal box-shape of the added D_{it} throughout the entire stress sequence indicates homogeneous D_{it} formation in a well-defined region of the device, i.e. the source. The large V_t-shift is assumed due to the formation of a potential barrier at the source as a result of SSI and electron trapping. This potential barrier should be visible in the CP characteristics as well, when the drain connection of the transistor is left open (fig. 6.28). The shift in rising edge of the CP characteristics reflects the formation of the potential barrier. The extracted V_{rise} closely tracks the threshold voltage shift measured at constant current (I_d=400nA) for low stress time (fig. 6.29). Afterwards, the generated D_{it} interferes [Gvdb04].

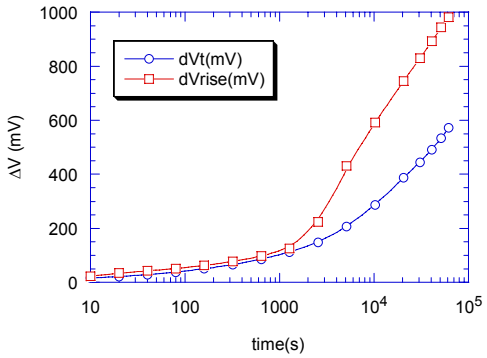

Figure 6.29: Comparison of ΔV_{rise} from CP and the threshold voltage shift measured at constant current (I_d=400nA) during stress at V_g=15 V and V_d=15 V [Gvdb04].

6.2.5. Drain and gate voltage dependency

In order to verify the contribution of each degradation mechanism, measurements have been performed at drain voltages down to V_d=5 V and at gate voltages down to V_g=3 V.

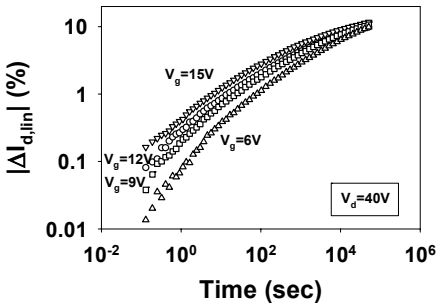

Figure 6.30: Linear drain current degradation at gate voltage stress between V_g=15 V and V_g=6 V and at constant drain voltage V_d=40 V.

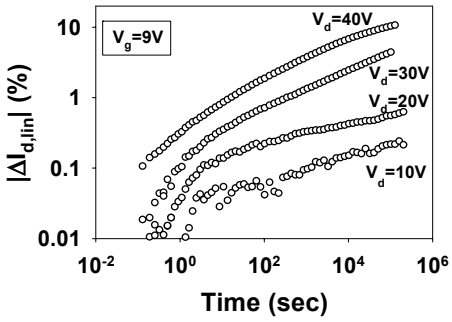

Figure 6.31: Linear drain current degradation at drain voltage stress between V_d=40 V and V_d=10 V and at constant gate voltage V_g=9 V.

Mobility reduction increases with increasing drain and gate voltage, although the gate voltage dependency appears to be rather weak (fig. 6.30). The linear drain current degradation shows the exponential dependence on drain voltage expected for normal hot

carrier degradation mechanism. High drain voltage will increase the impact ionisation creating more carriers to be injected. Moreover, a higher electric field leads to an increase of the injection probability (fig. 6.31). In contrast to the first mechanism, hot hole injection increases with drain voltage but decreases at higher gate voltage. High drain voltage will raise the impact ionisation located in the accumulation region creating more carriers to be injected. Moreover, the electric field in the silicon close to the gate oxide increases at high drain voltage, leading to the injection probability increase. Figure 6.32 shows the linear drain current as a function of the stress time at different drain voltages. Hot-hole injection can be neglected at V_d=30V. The gate voltage dependency can be understood by analysing the variation of the maximum hole temperature in the accumulation region and the electric field vertical to the Si/SiO_2 interface as a function of V_g. Increasing the gate voltage will decrease both the electric field as well as the hole-temperature. Hence the carrier generation and injection mechanism will be reduced and as such this second mechanism will be less present at higher gate voltages [Moens01] (fig. 6.33).

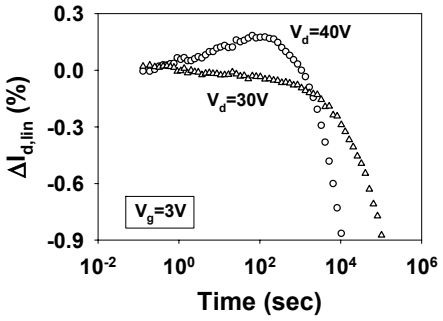

Figure 6.32: Linear drain current degradation during stress at V_d=40 V, V_d= 30 V and V_g= 3 V.

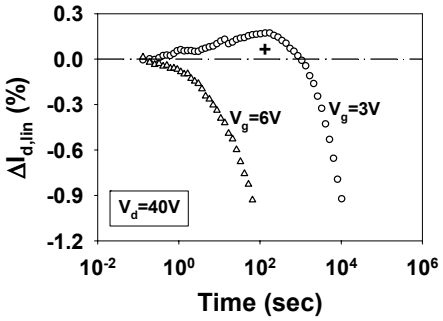

Figure 6.33: Linear drain current degradation during stress at V_g=3 V, V_g= 6 V and V_d=40 V.

$I_{d,sat}$ and V_t, which are more susceptible to SSI, show a very high drift, which is relatively insensitive to the drain voltage, as can be seen in figure 6.34 and figure 6.35. The shift in V_t is clearly determined by the gate voltage, as shown on figure 6.36. The higher vertical electric field leads to lower potential barrier at the $Si\text{-}SiO_2$ interface and higher probability of electron injection into the oxide. As a result of these local damages the series resistance of the n^- implantation region increases due to the low LDD dose. A larger voltage drop and a corresponding higher lateral field peak occur at the source near

the nLDD/pbody junction. As a consequence, a larger V_t-shift will be measured due to the increased hot carrier effect in this region. If the gate voltage is too low (V_g<12V) the electron will not have enough energy to overcome the energy barrier at the <Si-SiO_2 interface.

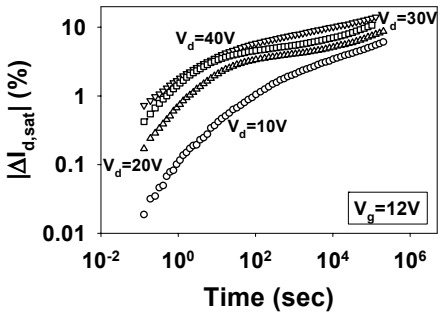

Figure 6.34: Saturation drain current degradation at drain voltage stress between V_d=40 V and V_d=10 V and at constant gate voltage V_g=12 V.

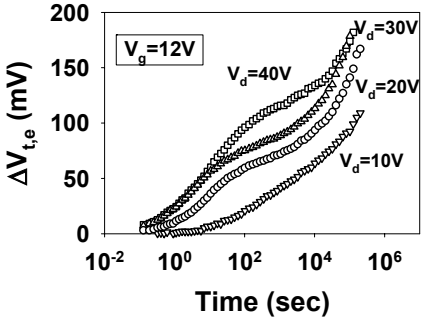

Figure 6.35: Extrapolated threshold voltage shift at drain voltage stress between V_d=40 V and V_d=10 V and at constant gate voltage V_g=12V.

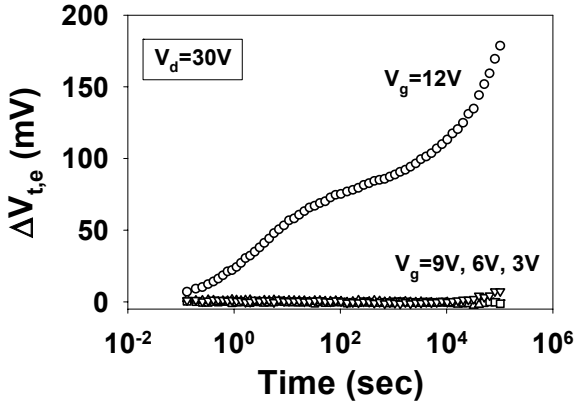

Figure 6.36: Extrapolated threshold voltage shift at gate voltage stress between V_g=3 V and V_g=12 V and at constant drain voltage V_d=30 V.

When the drain voltage is reduced, but the gate voltage is still high, the total lateral electric field decreases but the local lateral field in the nLDD region is still high enough to create hole-electron pairs. However, at very low drain voltage (V_d<5V) source side

injection is no longer detected proving that the lateral electric field, due to the drain voltage, has a role in the activation of the degradation mechanism. Probably the electrons gain enough energy to create electron-hole pairs also due to a small contribution of the lateral electric field related to the drain voltage.

6.2.6. Splits processing and solution to SSI

A variation (type 2) of the standard lateral DMOS transistor used in this work (type 1) with bigger active region below the poly-gate and more extended field oxide of the drift region has been stressed at V_d=40 V and V_g=15 V. In this device the charge trapping effect is small and only interface trap generation give rise to the high V_t-shift (fig. 6.37). The larger dimensions of this split lead to a reduction of the total lateral electric field. The drain voltage, at which source side injection is no longer detected, increases to V_d=10 V. The probability that some electrons can surmount the Si-SiO_2 potential barrier will be reduced [DiMaria93] leading to less initial electron trapping and/or interface state generation.

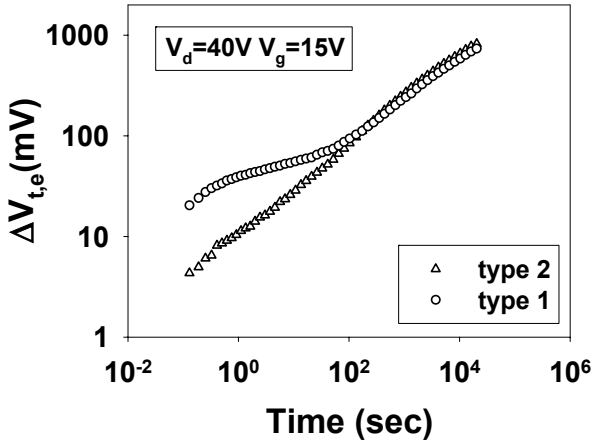

Figure 6.37: Extrapolated threshold voltage shift during stress at V_d=40 V and V_g=12 V for two lateral DMOS transistor type 1 and type 2.

As we previously discussed, a small amount of these defects can increase the series resistance as a result of too low LDD dose [Katto84]. A voltage drop and corresponding lateral field peak at the source near the nLDD/pbody junction increases with the stresstime, due to the gradually increase of the series resistance of the low n^- implantation

region. In the type 2, the lower initial electron trapping and/or interface state generation will lead to the lower series resistance and local lateral electric field peak. The injection probability is clearly reduced and, as a result, the electron trapping in the nLDD region can be neglected. The carriers flow inside the channel, where the vertical electric field is still high enough to redirect some of them towards the oxide channel and lower the potential barrier. Hot-electrons with enough energy will overcome the Si-SiO_2 barrier, giving rise to interface state generation.

Another variation (type 3) of the standard lateral DMOS transistor used in this work (type 1) with double nLDD dose has been stressed at V_d=40 V and V_g=12 V. Figure 6.38 shows the extrapolated threshold voltage of the three different types of lateral DMOS transistor (type 1, type 2 and type 3). Higher nLDD dose clearly reduces the V_t-shift.

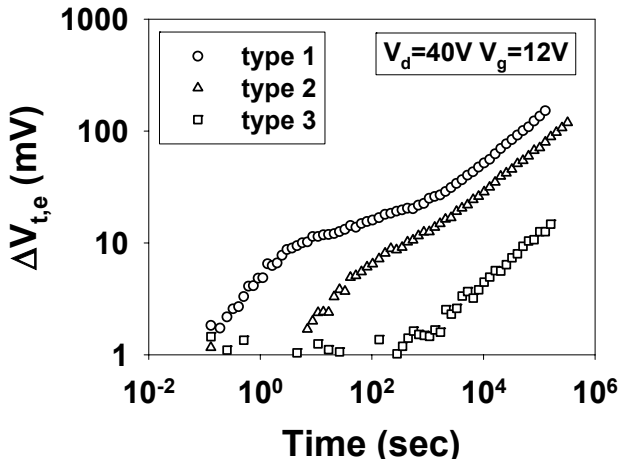

Figure 6.38: Extrapolated threshold voltage shift during stress at V_d=40 V and V_g=12 V for lateral DMOS transistor type 1, type 2 and type 3.

A higher LDD dose leads to a lower series resistance [Katto84]. It can be concluded that the voltage drop and corresponding lateral field peak in this region will be reduced. Less carriers flowing into the channel will have enough energy to overcome the Si-SiO_2 interface, even where the vertical electric field peak lowers the potential barrier.

6.2.7. Statistical spread on the measurements

As already shown, a large statistical spread for the $I_{d,sat}$ and V_t parameters is observed. The result of this spread is associated with the source side injection and the oxide damage

in this region, which influences mostly these two parameters. Figure 6.39 shows the linear drain current degradation of 8 identical lateral DMOS transistors after stress at V_d=40V and V_g=15V. No significant spread can be observed.

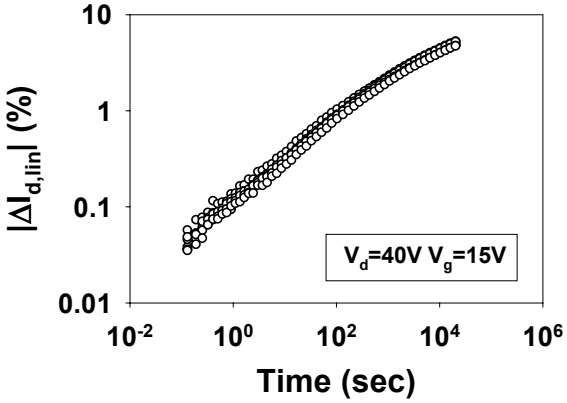

Figure 6.39: Linear drain current degradation of lateral DMOS transistor (type 2) during stress at V_d=40 V and V_g=15 V.

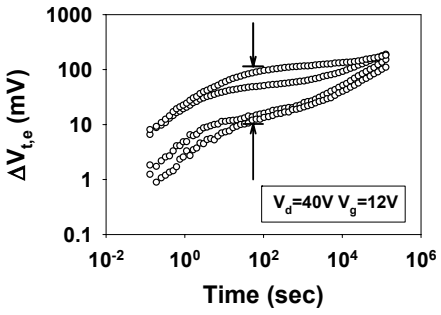

Figure 6.40: Extrapolated threshold voltage shift of lateral DMOS transistor (type 1) during stress at V_d=40 V and V_g=12 V.

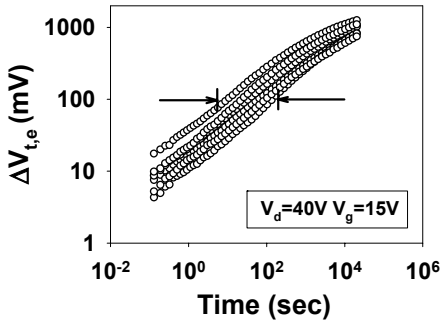

Figure 6.41: Extrapolated threshold voltage shift of lateral DMOS transistor (type 2) during stress at V_d=40 V and V_g=15 V.

There are two different statistical effects. Each of them is associated with one of the degradation mechanisms at the source. Figure 6.40 shows the extrapolated threshold voltage of 4 identical lateral DMOS transistors after stress at V_d=40 V and V_g=12 V. A

large spread is measured after 100sec of stress, as a consequence of the different saturation levels associated with the electron trapping. The reason of this effect can be due to a possible low quality of the oxide and/or not well-controlled LDD dose at the source side of the channel leading to electric field variations inside the DMOS transistor.

Figure 6.41 shows the extrapolated threshold voltage of 8 identical lateral DMOS transistors (type 2) after stress at V_d=40 V and V_g=15 V, where only interface state generation is present. The large statistical spread measured in this second type can be related to not well-controlled LDD dose at the source and/or can be associated to the location of the electron injection. If the injection point moves further away from the source side the oxide degradation will less affect the threshold voltage. The injection point location is a function of the lateral and vertical electric field and will change in case of not well-controlled device dimensions.

6.3. Modelling of the lateral DMOS transistor degradation

Two different models are presented in this work. The Goo model [Goo95], used to describe the degradation behaviour of LDD MOSFETs, is used in this work to describe the "normal" hot carrier degradation of lateral DMOS transistor. The linear drain current, which is the worst parameter at gate voltages below V_g< 9V, will be fitted with the Goo equation. The drain voltage dependency and the extrapolation at working condition will be presented (section 6.3.2.). Afterwards, an adaptation of this model is used to describe the slight increase of the linear drain current at gate voltages below V_g< 3V due to the hot-hole injection. A second model will be presented able to describe the large V_t-shift due to source side injection (section 6.3.3.).

6.3.1. Degradation models: overview

In the last few years, different models have been developed to describe hot-carrier degradation on standard field effect transistors (i.e.: MOSFETs, LDD MOSFETs…). Hu [Hu85], Goo [Goo95] and Dreesen-Croes [Dreesen00] describe the shift of the degradation parameters due to hot carrier effects for different technologies. The physical effects behind these models are well known. Recent articles try to extend them to describe the hot-carrier degradation on high power devices [Moens01]. However, as shown in the next sections, this is not straightforward and needs to be done with care. High voltage MOS transistors exhibit an electric field and carrier temperature distribution which is a complex function of V_{ds} and V_{gs}, the device process and layout parameters.

Modelling of device degradation due to hot-carrier effects is a translation of the understanding of the physical mechanisms. The model of Hu is mostly used to describe the degradation behaviour of standard MOSFETs:

$$\frac{\Delta I_{d,lin}}{I_{d,lin}} = C.\left[t.\frac{I_d}{W}.\left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right]^n \qquad (6.1)$$

with t the stress time, W the channel width, I_d the drain current at time t=0 during stress, I_{sub} the substrate current at time t=0 during stress, φ_{it} the energy to create interface states, φ_i the impact ionisation energy, C and n the fit constants [Hu85].

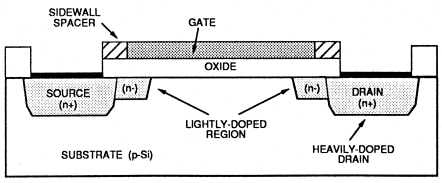

Figure 6.42: Schematic overview of LDD nMOSFETs.

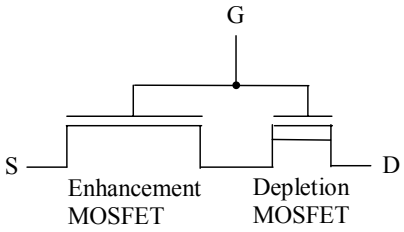

Figure 6.43: Schematic diagram of the equivalent circuit for LDD nMOSFETs after hot-carrier stress.

To explain the degradation of LDD nMOSFETs (fig. 6.42) Goo et al. suggested a three-MOSFET-equivalent circuit, which is comprised of an enhancement-mode MOSFET and two depletion-mode MOSFETs. In that equivalent circuit, each depletion-mode MOSFET acts as a bias-dependent-series resistance [Goo94].

However, in the LDD nMOSFETs, the effect of the source-side resistance as a part of intrinsic channel characteristic does not need to be regarded because the degradation in the n^- region of the source side can be neglected at low gate voltage and in general does not considerably affect the linear drain current. Therefore, a three-MOSFET circuit can be simplified to a two-MOSFET circuit shown in figure 6.43. The generated interface-states in the gate oxide affect the surface scattering. The carrier distribution in the n^- region accumulation layer can be further away from the Si/SiO_2 interface than in the channel inversion layer, and the negative charge due to the stress pushes the current path even deeper into the substrate. Moreover, the generated interface-state charge in the LDD

region is reduced with the stress time because φ_{it}, the critical energy barrier for interface-state generation, is enhanced by interface state charge. Therefore, the mobility degradation has a limit in the n^- region, which determines the saturation level of the hot-carrier induced current degradation [Goo94].

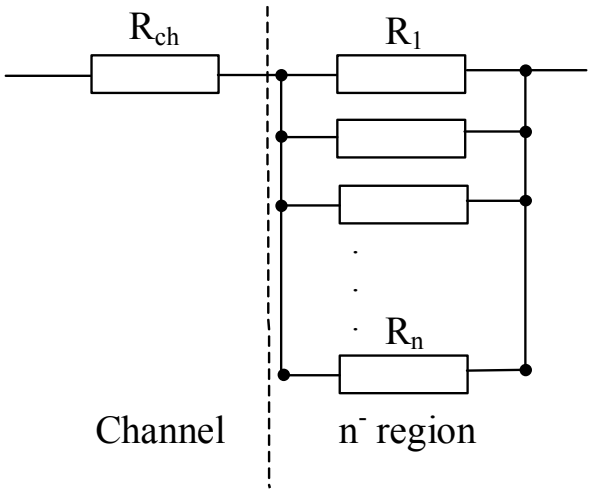

Figure 6.44: Schematic circuit for the channel and the n- region in an LDD nMOSFET subjected to hot-carrier stress at maximum Isub condition.

The model of Dreesen-Croes is based on the Goo model [Goo95]. However, a better physical interpretation is presented in this model to explain the saturation behaviour. After the electrons have proceeded through the channel resistance R_{ch} they reach a parallel connection of resistances R_1 to R_n in the n^- region (fig. 6.44).

For the virgin device, R1 is the smallest of all resistors and thus the mean part of the electrons flow close to the surface into the drain. When interface-states are created, R_1 increases and thus electrons will chose a lower path. After an extensive stress period, all resistances reach a very high value because of the interface-states created by hot-carriers, except R_n, which is unaffected by the interface-states because the distance to the surface of the LDD region is too high. In reality, current is not flowing through a single resistance Rn but through the equivalent resistance R_{eq} of the parallel resistance circuit [Dreesen00]. This describes the saturation behaviour of the mobility degradation. After some calculation, it can be found that:

$$\frac{\Delta I_d}{I_{d0}} = \frac{C_1 . \left(t . \frac{I_d}{W_{eff}} . \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right)^n}{1 + C_2 . \left(t . \frac{I_d}{W_{eff}} . \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right)^n} \tag{6.2}$$

where:

$$C_1 = \frac{C_3 . K_0 . \left(R_{eq}(t=0) / R_{eq}(t=\infty) - 1 \right)}{1 + K_0} \quad C_2 = \frac{C_3 . \left(R_{eq}(t=0) / R_{eq}(t=\infty) + K_0 \right)}{1 + K_0}$$

and *n* are fit constants. According to Chan [Chan95], the hot-carrier degradation of LDD nMOSFETs at maximum substrate condition can be described by a sum of two terms. The first term, represented by equation 6.2 represents the degradation of the spacer oxide. The refined model of Goo can be used to describe this degradation. The second term represents the degradation of the gate oxide. The model of Hu can be used to describe this degradation. In the model of Dreesen-Croes, the total degradation behaviour is described by the following equation:

$$\frac{\Delta I_d}{I_{d0}} = \frac{C_1 . \left(t . \frac{I_d}{W_{eff}} . \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right)^n}{1 + C_2 . \left(t . \frac{I_d}{W_{eff}} . \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right)^n} + C_3 . \left(t . \frac{I_d}{W_{eff}} . \left(\frac{I_{sub}}{I_d} \right)^{\varphi_{it}/\varphi_i} \right)^m \tag{6.3}$$

which has five fit constants: C_1, C_2, C_3, *n* and *m*. This equation is the degradation model for LDD nMOSFETs under hot-carrier stress at maximum substrate current.

6.3.2. Modelling of the linear drain current degradation

A first attempt to model the linear drain current degradation of lateral DMOS transistor is made using the least-square linear equation of Hu [Hu85]:

$$\frac{\Delta I_{d,lin}}{I_{d,lin}} = C.t^{n} \tag{6.4}$$

This simplified equation is obtained from equation 6.1 without the acceleration factor for the voltage dependency. C and n are fit constants. Figure 6.45 shows the linear drain current degradation after stress at V_d=40 V V_g=12 V. The line is the least-square linear fit of the degradation measurement.

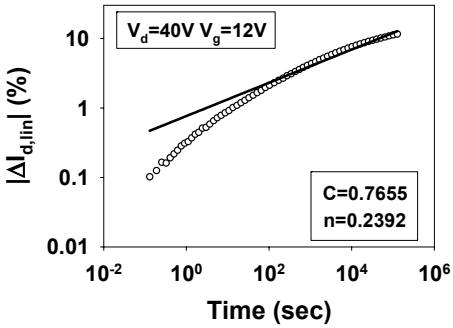

Figure 6.45: Dots: Linear drain current degradation during stress at V_d=40 V V_g=12 V. Line: Least-square linear fit of the degradation measurement with the model of Hu.

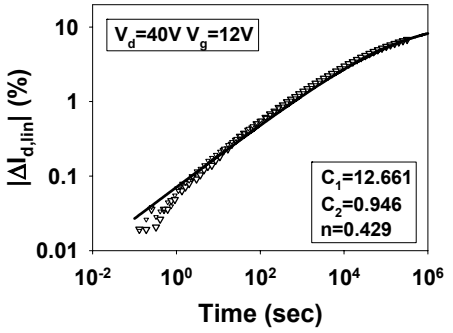

Figure 6.46: Dots: Linear drain current degradation during stress at V_d=40 V V_g=12 V. Line: Least-square non-linear fit of the degradation measurement with the model of Goo.

Although a lifetime prediction can be done, it is clear that the model of Hu cannot be used to properly describe the degradation of power DMOS transistor because the model is not able to describe the degradation measurement. Nevertheless, the model of Hu is still widely used today for lifetime prediction [Hu85]. The model of Goo is the only one able to describe the physical effects observed in the lateral DMOS transistors for higher gate voltage (V_g>3 V) (fig. 6.46). In this device, the degradation mechanism described by Goo occurs in the gate oxide at the drain end of the channel or beyond.

Simultaneous least square non-linear fit of the degradation curves with the model of Goo (equation 6.2) is performed taking in consideration the drain voltage dependency. The maximum substrate current and the drain current are measured at stress condition. As shown in figure 6.47, the model perfectly describes the behaviour of the linear drain current in the complete degradation area from 0.01 % up to more than 10 % for different drain voltages. With the aid of the fit parameters and the measurement of I_{sub} and I_d at the

different stress conditions and at the operating conditions, the degradation behaviour at the stress conditions and at the operating conditions can be calculated. The dots represent the degradation measurements at the different stress conditions. The lines give the calculated degradation behaviour at the different stress conditions and at the operating conditions. When it can be assumed that the degradation model is correct, the high-resolution measurements can be stopped earlier than the classical measurements and thus the test times can be reduced. Moreover, a complete prediction of the degradation behaviour can be obtained for the stress conditions that could require too long testing time. The linear drain current follows a power law and saturates with long stress time. The slope around n=0.4 confirms the presence of fast interface traps [Dreesen00].

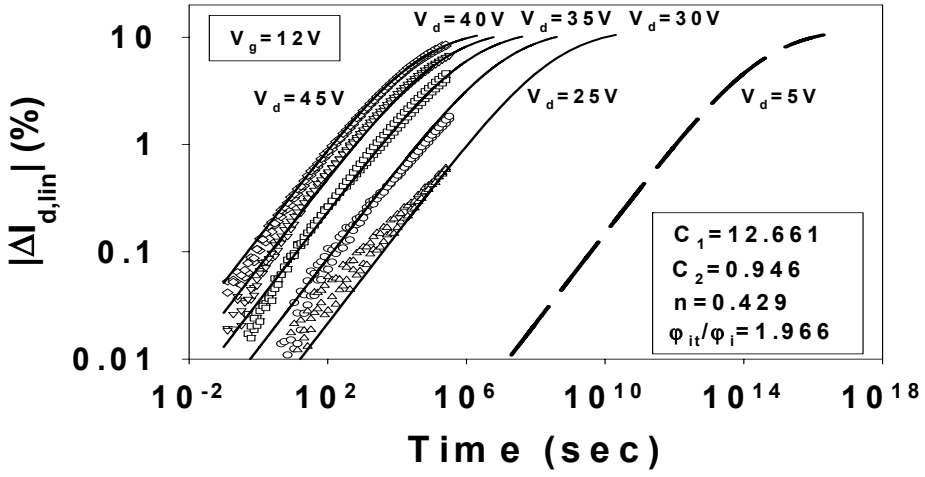

Figure 6.47: Dots: Linear drain current degradation during stress at V_g=12 V and from V_d=45 V to V_d=25 V. Line: simultaneous least square non-linear fit of the degradation measurements with the model of Goo. Dotted line: Prediction of the degradation measurement at operating voltage.

With some modifications the model of Goo can be used to describe the contribution of the hot hole-injection in the gate oxide of the accumulation region. At low gate voltages (V<3V) a second term is added to describe the hot hole-injection mechanism superimposed on the mobility reduction:

$$\frac{\Delta I_d}{I_{d0}} = \frac{C_1.t^n}{1+C_2.t^n} + C_3.t^m \qquad (6.6)$$

which has five fit constants: C_1, C_2, C_3, n and m. The first term describes the mobility reduction in the drift region and takes into account the saturation behaviour of the D_{it} formation. The second term mimics the hot hole-injection and trapping. Eventual saturation behaviour for the second term is not included.

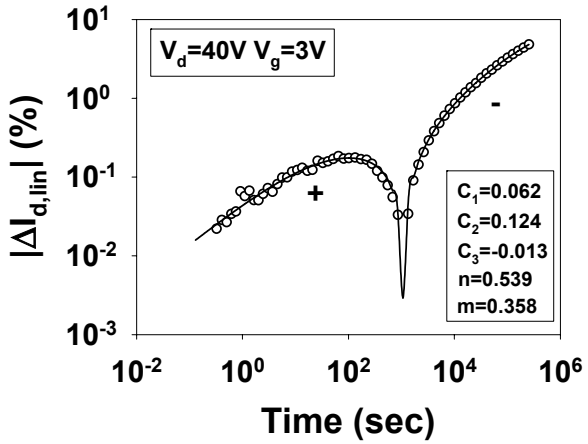

Figure 6.48: Dots: Linear drain current degradation during stress at V_g=3 V and V_d=40 V. Line: simultaneous least square non-linear fit of the degradation measurements with equation 6.6.

Figure 6.48 shows the least-square non-linear fit of the linear drain current with this modified model. The second term of the equation is negative because the two degradation mechanisms, mobility reduction and hot-hole injection, are competing [Moens01]. The slope around n=0.5 of the first term confirms the presence of fast interface traps in the accumulation region. The value m=0.3 of the second term is lower compared to n as expected [Dreesen00].

6.3.3. Modelling of the threshold voltage shift

At high gate voltage ($V_g \geq$ 12 V) and high drain voltage (V_d= 40 V), source side injection is superimposed on the mobility reduction. As a result, a large drift of $I_{d,sat}$ and a large V_t shift can be detected. Under these extreme conditions, the threshold voltage becomes the worst parameter of the lateral DMOS transistor. The V_t-shift usually follows a time power law At^n, where t is the stress duration and A is a parameter, which depends on the drain voltage and on the technology. This relation describes the last part of the V_t-shift due to interface state generation at the source side of the channel. The slope n=0.5 is in

agreement with values found in literature [Dreesen00]. A first order kinetic model can fit the V_t-shift due to electron trapping in the gate oxide of the nLDD region:

$$V_t(t) = V_{t0} + B\left(1 - \exp\left(-\frac{t}{\tau}\right)\right) + At^n \qquad (6.7)$$

where τ is the time necessary to fill the created traps by electronic current, V_{t0} is the threshold voltage before stress and A, B, n fitting constants [Doyle90].

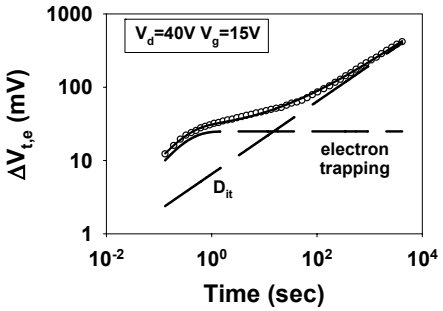

Figure 6.49: Dots: Extrapolated threshold voltage shift during stress at V_g=15 V and V_d=40 V. Line: Fit of the degradation measurements with equation 6.7. Dotted lines: Decomposition of the equation 6.7 in two terms.

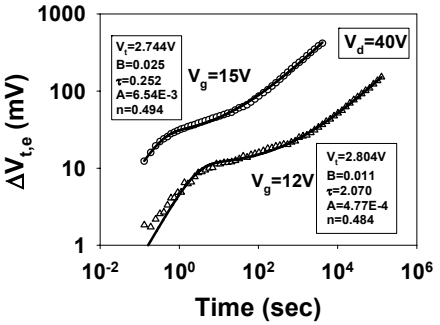

Figure 6.50: Dots: Extrapolated threshold voltage shift during stress at V_g=15 V, V_g=12 V and V_d=40 V. Line: Fit of the degradation measurements with equation 6.7.

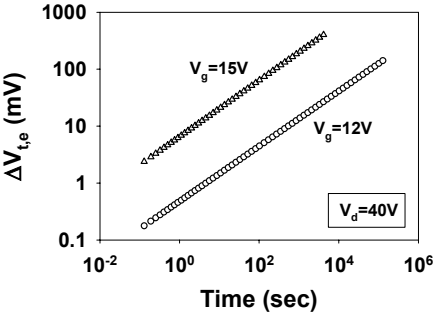

Figure 6.51: Second term of equation 6.7 during stress at V_g=15 V, V_g=12 V and V_d=40 V.

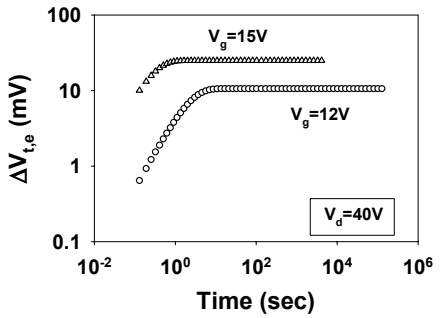

Figure 6.52: First term of equation 6.7 during stress at V_g=15 V, V_g=12 V and V_d=40 V.

Figure 6.49 shows the fitting with equation 6.7 of the extrapolated threshold voltage shift after stress at V_d=40V and V_g=15V. The model has been used to analyse the gate voltage

dependency (fig. 6.50). The decomposition of the two terms of the equation clearly shows that the higher contribution to the large Vt-shift is given by the interface state generation in the oxide at the source side of the channel, as already described in the previous paragraphs of this work (fig. 6.51). At higher gate voltage the increase of the vertical electric field in the channel and the increase of the drop voltage in the nLDD region lead to higher probability of interface state generation in this region, i.e. the source. Figure 6.52 shows the change in the saturation level of the V_t-shift, due to variation of electron trapping in the nLDD region for different gate voltages as already discussed in the previous sections.

6.4. Conclusion

In this work we presented the analysis of the HCI behaviour of a high voltage nDMOS transistor. We describe the effects of hot hole/electron injection in the channel region and/or the gate controlled drift region of DMOS transistors. A first mechanism is attributed to decreased electron mobility due to increased carrier scattering upon D_{it} formation in the channel or beyond whereas a second mechanism occurs in the gate overlapped drift region of the device and is due to hot-hole injection and trapping. The competition of both mechanisms depends strongly on the stress conditions. In addition to these different degradation mechanisms, under high stress conditions source side injection takes place, which leads to rather moderate changes of the linear drain current ($I_{d,lin}$) but significant changes of the saturation drain current ($I_{d,sat}$) and the threshold voltage (V_t).

The mechanisms could be identified by analysis of the electrical data and by performing Charge Pumping (CP) experiments. The experimental results give clear evidence for the existence of a source-side injection degradation component. Higher nLDD dose clearly reduces this effect. The best suitable model has been discussed and adapted to this new technology and detailed TCAD simulations were also performed, supporting the proposed model.

6.5. Reference of the chapter

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7. Conclusions

7.1. Summary

This work deals with two of the most important oxide reliability issues of the last decade, the leakage current in thin oxide and hot carrier degradation on power DMOS transistors. The intention of this work was first to give an overview of the basic terms and definitions important for the oxide reliability study, followed by a discussion of the mechanisms that determine these oxide defects. Afterwards a detailed analysis of hot carrier degradation mechanism on power device and leakage current in thin oxide was performed.

A high-resolution SILC test bench has been developed in this work to perform measurements on thin oxide at ultra-low voltages at speeds in the order of 100 microseconds (chapter 3). Commercial electrometers such as K2400 or K487 were too slow to measure leakage current in thin oxide at the desired spreed. Therefore it was necessary to make our own I/V converter to perform high-speed measurements. The high-resolution SILC measurement system is able to detect small current changes after short stress times. The high-resolution combined with high-speed measurement was used to distinguish the contribution of SILC and charge trapping effects. Through the use of an appropriate model, SILC-related parameters and trapping-related parameters were quantified. The extrapolation of high voltage measurements to operating conditions was still possible taking into account the new results. The refined model of Nigam and co-workers was used with some adaptations to describe the gate current behaviour. An alternative method for the determination of part of the fitting constants was used, fitting the current's derivative instead of the actual current density. The derivative *dJ/dt* showed significant scattering particularly during the initial period of the measurement. Therefore, a smoothing method, based on the least structure method of Cook was applied to the original measured data before taking the derivative. At the end, the physical interpretation of the results and the voltage dependency was discussed (chapter 4).

Performing high-resolution hot-carrier measurements on high power devices is not straightforward. During this work, the test bench had to be protected from environmental influences. The measurement set-up was presented and the measurement procedure was explained in detail in the chapter 5. Afterwards, a complete analysis of the hot carrier degradation of lateral DMOS transistors was shown. Upon hot carrier stress, three different and competing degradation mechanisms occurred. The mechanisms were

identified by analysis of the electrical data and by performing Charge Pumping (CP) experiments and also detailed TCAD simulations. The experimental results were discussed giving a clear evidence for the existence of source-side injection degradation. The best suitable model was used to describe and predict the degradation behaviour of lateral DMOS transistors (chapter 6).

7.2. Future work

The extension of existing smart power technologies towards higher temperature applications is a challenging and demanding task. At higher temperatures, technologies must deal with many issues. Substantial increase in junction leakage leads to a higher risk of latch-up. At high temperature V_{th} is reduced, the sub-threshold leakage increases and the carrier mobility decreases leading to high R_{on}. At these extreme conditions hot carrier degradation is still an important degradation mechanism. Moreover, TDDB and SILC at high temperature become more and more important in the dielectric reliability of thin gate oxides. New characterisation and measurement techniques have to be developed and applied for high temperature applications. The standard CMOS characterisation techniques are not applicable any longer to the integrated power transistors, as the latter operate under different conditions (e.g. characterisation of lattice heating, heat distribution, switching of inductive, capacitive or resistive loads, high temperature…). High voltage transistors are limited in power by electrical and thermal phenomena triggering their internal bipolars and leading in general to the destruction of the device. The electrical effect reflects the intrinsic capability of the device and constitutes its maximum physical limit. The thermal one depends on the conditions applied to the device and reduces the maximum power much below its intrinsic capability. This thermal effect is originating from the heat generated when for instance a high power is forced through the device. Indeed the temperature increases locally in the transistor reducing the built-in potential of the junctions. At the same time, the sheet resistance of the doped regions increases with the increasing temperature and low currents due to thermal generation or impact ionisation are enough to polarise locally a junction in forward triggering internal parasitic bipolars and leading to the destruction of the device. Therefore, the extension of the results of this thesis to high temperatures can be a fundamental drive for future work.

8. Publication list and Awards

Publications

Aresu S., De Ceuninck W., Dreesen R., Croes K., Andries E., Manca J., De Schepper L., Degraeve R., Kaczer B., "High-resolution SILC measurements of thin SiO_2 at ultra low voltages", Microelectronics Reliability, Vol. 42, 2002, pp. 1485-1489. Presented paper ESREF2002 (Italy).

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Awards

Aresu S., De Ceuninck W., Van den bosch G., Groeseneken G., Moens P., Manca J., Wojciechowski D., Gassot P., "Evidence for Source Side Injection hot carrier effects on lateral DMOS transistors", Best Paper Awards ESREF2004 (Zurich).