DOCTORAATSPROEFSCHRIFT

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Increasing the mean grain size in copper films and features

Proefschrift voorgelegd tot het behalen van de graad van
Doctor in de Wetenschappen, richting natuurkunde, te verdedigen door:

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Copromotor: prof. dr. Ward DE Ceuninck

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The true value of accomplishment
is not the accomplishment itself
but the way it has been achieved

Table of contents

Glossary

AFM	Atomic Force Microscopy
ASIC	Application Specific Integrated Circuit
Aspect Ratio (AR)	Ratio height/width of the recesses patterned into the dielectric
BEOL	Back-End-Of-Line comprises the process steps from contact (opening that allows electrical connection between metal and silicon layers) through completion of the wafer prior to electrical test
Blanket film	Unpatterned film
Brightener	Additive used to locally accelerate the electroplating process
BSE	BackScattered Electron
Burgers vector	Vector that represents the magnitude and direction of the lattice distortion of a dislocation in a crystal lattice
CMP	Chemical Mechanical Polishing
CVD	Chemical Vapour Deposition
Damascene	Process for Cu interconnects manufacturing, in which first the dielectric is patterned and subsequently recesses are filled by metallization
DRAM	Dynamic Random Access Memory
DRAM ½ Pitch	Half the distance between cells in a Dynamic Random Access Memory chip
Dry-etch	Etch method where the etch reactants come from a gas or vapour phase and are typically ionized. The atoms or ions from the gas are the reactive species that etch the exposed film. This is different from wet-etch, where the etch reactants come from a liquid source
EBSD	Electron BackScatter Diffraction
EBSP	Electron BackScatter Pattern, also called Kikuchi pattern. An image consisting of relatively intense bands intersecting one another and overlying the normal distribution of backscattered electrons, as a result of the Bragg diffraction of electrons at all atomic planes in the crystal lattice
ECD	Electrochemical Deposition
EM	Electromigration
FCC	Face Centered Cubic
FEG	Field Emission Gun

Adatom	Incoming atoms on the growing film surface during the deposition of a thin film
Gnomonic projection	A gnomonic projection is a non-conformal projection obtained by projecting points which are lying on the surface of a sphere, from the sphere's centre to a point on a plane that is tangent to a certain point S on the sphere. For S, typically the North pole or South pole of the sphere are chosen
HT-XRD	High Temperature X-Ray Diffraction
IC	Integrated Circuit
ICP	Inductively Coupled Plasma
IMP	Ionised Metal Plasma
IPF	Inverse Pole Figure
I-PVD	Ionized plasma Physical Vapour Deposition
Kikuchi pattern	Electron Backscatter Diffraction Patterns are also referred to as backscatter Kikuchi patterns (named after Kikuchi, 1928, who observed similar diffraction patterns in the TEM)
k-value	Relative dielectric constant/permittivity ε_r
Low-k	Low relative permittivity (dielectric constant)
Miller indices	The 3-digit crystallographic indices used to describe crystallographic lattice planes or directions
MPU	MicroProcessor Unit
OC	Orientation Contrast
Pole figure	The spherical projection of crystal directions displayed in a plane representing the upper or lower hemisphere
PVD	Physical Vapour Deposition
RIE	Reactive Ion Etching
SE	Secondary Electron
Self-anneal	Room temperature recrystallization process
SEM	Scanning Electron Microscopy
SGG	Secondary Grain Growth
SSGG	Super Secondary Grain Growth
Superfilling	Bottom-up filling in trenches
Suppressor	Additive used to locally decrease the electroplating process
TEM	Transmission Electron Microscopy
Trench	Recess patterned into the dielectric, to be filled with metallization
XRD	X-Ray Diffraction
Yielding	Deformation mechanisms that may occur in thin films when these films are in the plastic regime
Zener pinning	The influence of small particles on the movement of low and high angle grain boundaries through a polycrystalline material. These particles act to prevent the motion of such boundaries by exerting a pinning pressure which counteracts the driving force pushing the boundaries

List of symbols

Symbol	Units	Description
e^-		Electron
P	W	Dynamic power consumption
C	F	Interconnect capacitance
R	Ω	Interconnect resistance
f	Hz	Frequency for device operation
λ	nm	Electron mean free path
h	nm	Film thickness
ρ	μΩ.cm	Resistivity
V	V	Voltage for device operation
k		Relative permittivity (dielectric constant)
σ	MPa	Film stress
α	1/°C	Thermal expansion coefficient
T	°C	Annealing temperature
m	m^4/Js	Grain boundary mobility
d	nm	Average grain diameter
t	hours	Time
τ	ps	Interconnect signal transmission delay time
κ	1/m	Boundary curvature
γ_{gb}	J/m^2	Grain boundary energy per unit area
M	GPa	Biaxial modulus
E_a	eV	Activation energy
T_m	°C	Melting temperature
T_r		Ratio of the deposition temperature over the melting temperature of a deposited film

Nederlandstalige samenvatting

De zoektocht naar een voortdurende verbetering van de werking van micro-elektronische apparatuur is een drijvende kracht geweest voor onderzoekers uit de halfgeleiderindustrie om de zogezegde wet van Moore te kunnen blijven nastreven. In de jaren zestig nam Moore een exponentiële groei waar van het aantal transistoren op een geïntegreerd circuit en postuleerde hij dat deze trend zich zou blijven voortzetten. Gedurende tientallen jaren is het verkleinen van de afmetingen van de transistoren een zeer doeltreffende manier om aan deze wet te voldoen. Doordat steeds meer transistoren aanwezig zijn op een steeds kleinere chipoppervlakte wordt de rol van de interconnectiebanen belangrijker naarmate men naar kleinere afmetingen gaat. Deze interconnectiebanen zijn fijne geleidende metaalbaantjes die van elkaar gescheiden zijn door een isolerend materiaal en zorgen voor een snelle signaaloverdracht tussen de verschillende delen van het geïntegreerde circuit. Sinds de ontwikkeling van het eerste geïntegreerde circuit door Jack Kilby en Robert Noyce is aluminium, gecombineerd met SiO_2 als isolerend materiaal tussen de metaalbaantjes, het meest gebruikte metaal voor de productie van interconnectiebanen. Om de elektromigratie gerelateerde betrouwbaarheid van de aluminium metaalbaantjes te verhogen worden deze gelegeerd met typisch 0.5% tot 1.0% koper. De voortdurende vraag vanuit de IC industrie naar verdere miniaturisatie en een hogere transistordichtheid brengt tevens een verhoogde dichtheid aan interconnectiebanen met zich mee. Naarmate de afmetingen generatie na generatie blijven verkleinen, wordt de snelheid van het geïntegreerde circuit steeds meer afhankelijk van de eigenschappen van de interconnectiebanen (en de materiaalkeuze hiervoor) dan van de transistoren en wordt het miniaturisatieproces uiteindelijk minder rendabel. Om dit te voorkomen wordt er gezocht naar nieuwe types materialen voor zowel de metaalverbindingen zelf alsook het isolerende materiaal hiertussen. Voor deze laatste werd er afgestapt van het traditionele SiO_2 en overgegaan naar nieuwe materialen met een lagere diëlektrische constante, gaande van SiOC:H tot polymeren. Koper bleek vervolgens een goede kandidaat te zijn ter vervanging van aluminium als interconnectiemateriaal omwille van lagere elektrische weerstand en de

betere elektromigratie gerelateerde betrouwbaarheid vergeleken met aluminium-koper legeringen. Naast deze voordelen bezit koper echter ook enkele nadelige eigenschappen zoals de snelle diffusie in onderliggende Si/SiO_2-lagen en de zeer moeilijke droog etsbaarheid. Dit bemoeilijkte de toepasbaarheid van koper in het conventioneel gebruikte metallisatieproces, waardoor de ontwikkeling van een nieuwe metallisatietechniek zich uiteindelijk opdrong. In tegenstelling tot het conventionele aluminium metallisatieproces, waarbij structuren eerst uit een metaallaag weggeëtst worden om dan vervolgens deze op te vullen met een isolerend materiaal, bestond deze nieuwe koper metallisatietechniek erin om te starten met het wegetsen van structuren in een isolerende diëlektrische laag om deze hierna op te vullen met een diffusiebarrière en koper. Hierdoor kon de ets -en diffusieproblematiek van koper omzeild worden, maar bracht de nieuwe techniek tevens ook nieuwe uitdagingen met zich mee zoals bijvoorbeeld de eis om structuren defectloos kunnen vullen met koper en een grondige kennis van de fysische eigenschappen van dit materiaal in dunne filmen en structuren. Het bleek al vrij snel dat sputteren gevolgd door een elektrochemische afzetting van koper een relatief goedkope manier is om defectloos holtes in het isolerende materiaal op te vullen. De toevoeging van welbepaalde additieven tijdens het afzettingsproces speelt hierbij een cruciale rol, maar levert tevens bijkomstige nadelen, waarvan de belangrijkste ongetwijfeld het optreden van een spontane korrelgroei bij kamertemperatuur is, welke kan plaatsvinden over een periode van weken tot zelfs enkele uren. Deze spontane korrelgroei gaat gepaard met een toename in korrelgrootte, spanningswijzigingen, kristallografische oriëntatieveranderingen en een weerstandsdaling. Om de invloed van spontane korrelgroei op de verschillende opeenvolgende stappen in het metallisatieproces te kunnen controleren en de betrouwbaarheid van de metaalbaantjes te kunnen verbeteren is er een grondige kennis van het spontane korrelgroeiproces in koperfilmen gewenst. Voor elektrochemisch afgezette koperlagen blijkt de uiteindelijke korrelgrootte beperkt te worden door onder andere de filmdikte en de concentratie aan onzuiverheden in de film. Typische korrelgroottes in de orde van micrometers worden hier waargenomen. In fijne metaalbaantjes kan de korrelgrootte zelfs nog verder beperkt worden door de afgenomen fysische afmetingen van de structuur waarin de korrelgroei moet plaatsvinden. De dynamica van het spontane korrelgroeiproces kan mogelijk ook beïnvloed worden door de

veranderende volumefracties van het gesputterde koper en elektrochemisch afgezet koper in de steeds kleinere structuren. Bovendien wanneer de afmetingen van de metaalbaantjes dalen tot in het nanometer regime, worden fundamentele en praktische limieten van een bepaalde materiaalkeuze bereikt. Voor deze kleine afmetingen zal de elektrische weerstand van de metaalbaantjes dramatisch toenemen wanneer afmetingen ervan in de buurt van de vrije weglengte van het elektron komen (~39nm voor bulk koper op kamertemperatuur). Deze toename heeft verschillende bijdragen waaronder bijvoorbeeld een aantal verstrooiingsmechanismen aan de grensvlakken van de film met het substraat en/of isolerende materiaal, het vrije filmoppervlak of aan korrelgrenzen. Het zoeken naar manieren om grotere korrels in metaalbaantjes te krijgen blijft van groot belang, aangezien op deze manier de bijdrage van de verstrooiingsmechanismen aan de korrelgrenzen tot de elektrische weerstand aanzienlijk kan verminderd worden.

Aangezien koperen interconnectiebanen zowel gesputterd als elektrochemisch koper bevatten, zullen we in deze thesis eerst onze aandacht richten naar de studie van het spontane korrelgroeiproces in gesputterde koperlagen en de invloed die verschillende parameters hierop kunnen hebben. Meer specifiek zullen deze parameters geoptimaliseerd worden om op die manier de gemiddelde korrelgrootte in deze filmen aanzienlijk te vergroten. Hierbij zullen alle resultaten besproken worden uitgaande van de verschillende drijvende krachten welke voorradig zijn voor spontane korrelgroei. In een volgende stap zullen deze gesputterde koperlagen gecombineerd worden met elektrochemisch afgezette koperlagen om zo ook hierin de korrelgrootte te doen toenemen. Tot slot zal al deze kennis toegepast worden op de productie van metaalbaantjes, in de hoop de korrelgrootte ook hierin te kunnen vergroten. Al deze onderwerpen zullen besproken worden in zes hoofdstukken.

Hoofdstuk 1 situeert het onderzoek en probeert een duidelijk beeld te schetsen van de huidige problematiek binnen het onderzoeksdomein. Verder wordt het belang en motivatie van het huidige werk toegelicht.

Hoofdstuk 2 geeft een overzicht van de huidige kennis in het vakdomein. Hierbij wordt er vooral toegespitst op korrelgroei en de vorming van textuur in polykristallijne filmen tijdens en na de afzetting en hun mechanische eigenschappen. Dit is noodzakelijk om de belangrijkste

begrippen en terminologie welke in dit werk gebruikt worden te introduceren.

In hoofdstuk 3 wordt een overzicht gegeven van de experimentele technieken welke gebruikt worden voor zowel de productie alsook voor de karakterisatie van de bestudeerde koperfilmen en structuren in dit werk. Hierbij worden de werkingsprincipes, de theoretische achtergrond en experimentele opstellingen grondig uitgelegd. Voor de microstructurele karakterisatie wordt er gebruik gemaakt van zowel raster elektronenmicroscopie (REM), elektron terugverstrooide diffractie (EBSD) en transmissie elektronen microscopie (TEM). Voor de mechanische filmkarakterisatie wordt de spanning in de filmen bepaald aan de hand van metingen van de filmkromming met behulp van de scanning laser methode. Voor de elektrische karakterisatie wordt de filmweerstand opgemeten met behulp van een vierpuntsweerstandsmeting.

In hoofdstuk 4 wordt de microstructuur en textuur van gesputterde dunne filmen bestudeerd voor, tijdens en na spontane korrelgroei. Hierbij wordt de invloed van verschillende parameters onderzocht zoals de filmdikte, de opwarmtemperatuur tijdens de korrelgroei en de aangelegde elektrische spanning bij het sputterproces. De microstructuur van de gesputterde koperlagen direct na afzetting bevat kleine korrels met een gemiddelde korrelgrootte van ongeveer 70nm in het filmvlak. Verder bevat de microstructuur van deze filmen een aantal kolomvormige korrels, welke in de meeste gevallen een groot aantal tweelingen bevatten. De hoeveelheid kolomvormige korrels is afhankelijk van de gekozen afzetparameters van het sputterproces. De initiële textuur kan beschreven worden als een sterke {111} textuur met tevens een zwakkere {113} component volgens de loodrechte van de film. De oriëntatie van de verschillende korrels volgens een richting in het filmvlak is echter willekeurig. Afhankelijk van de aangelegde elektrische spanning aan het substraat tijdens het sputterproces blijken de filmen tevens een andere textuur te bevatten. Voor filmen met een hoger aangelegde elektrische spanning bij afzetting wordt een sterkere {111} textuur en een zwakkere {113} textuur waargenomen vergeleken met filmen met een lager aangelegde elektrische spanning. Deze verschillen in microstructuur en filmtextuur blijken eveneens een invloed te hebben op de verdere microstructurele evolutie van de filmen. Tijdens de spontane korrelgroei in de bestudeerde gesputterde filmen werd er naast de frequent waargenomen secundaire korrelgroei mode een nieuwe

groeimode ontdekt. Deze nieuwe groeimode blijkt een abnormale groeimode te zijn, waarbij de korrels concentrisch groeien tot enkele tientallen micrometers in diameter en hierdoor de oorspronkelijke {111} beginoriëntatie transformeren naar een hoofdzakelijk sterke {100} textuur. Verder wordt er een duidelijke competitie waargenomen tussen beide groeimodes. Hierbij blijkt de nieuwe groeimode sterk afhankelijk te zijn van zowel de filmdikte, de aangelegde elektrische spanning aan het substraat bij de afzetting van de filmen, alsook van de opwarmtemperatuur tijdens het groeiproces. In dit werk wordt aangetoond dat de nieuwe groeimode enkel waargenomen werd in dikke gesputterde koperlagen en dat een verhoogde aangelegde elektrische spanning tijdens de afzetting een duidelijke vertraagde groeisnelheid van het koper bij kamertemperatuur veroorzaakt. Dit verschil in groeisnelheid kan mogelijk verklaard worden door energieverschillen in de korrelgrenzen ten gevolge van een verschillende initiële microstructuur en/of een verschillende defectconcentratie ten gevolge van verschillend aangelegde elektrische spanningen bij afzetting van de filmen. Verder blijkt voor lage aangelegde elektrische spanningen dat de nieuwe groeimode (zowel de uiteindelijke korrelgrootte alsook de fractie) duidelijker aanwezig te zijn bij kamertemperatuur dan bij hogere groeitemperaturen en blijkt deze groeimode voornamelijk aanwezig te zijn wanneer een α-Ta diffusiebarrière gebruikt wordt. In tegenstelling tot de lage aangelegde elektrische spanningen, komt bij de hoger aangelegde elektrische spanningen de nieuwe groeimode duidelijker voor bij hogere temperaturen en blijkt dit onafhankelijk te gebeuren van de samenstelling en/of textuur van de onderliggende diffusiebarrière. De energie voor het activeren van deze nieuwe groeimode werd uit de korrelgroei experimenten afgeschat op ~0.77eV. Deze is wat lager dan de waarde welke voor secundaire korrelgroei in koper teruggevonden wordt (~0.93eV). Verder blijkt de activatie energie voor de nieuwe groeimode onafhankelijk te zijn van de aangelegde spanning tijdens de afzetting van de filmen. Alle waargenomen trends in dit onderzoek werden besproken met behulp van de drijvende krachten voor korrelgroei. Wanneer hierbij de drijvende krachten voor de korrelgroei een homogene bijdrage leveren, dan treedt er normale groei op, terwijl wanneer de drijvende krachten selectief de groei van bepaalde subpopulaties bevoordelen tijdens het groeiproces, dit kan leiden tot abnormale korrelgroei. Één van de hoofdredenen voor deze selectiviteit zijn een anisotropie in de oppervlakte/grensvlak energie en/of

de vervormingsenergie. In dit werk wordt aangetoond dat de minimalisatie van de vervormingsenergiedichtheid de drijvende kracht is voor de nieuwe groeimode in gesputterde koperfilmen.

In hoofdstuk 5 is het hoofddoel ook in elektrochemisch afgezette koperfilmen en structuren de gemiddelde korrelgrootte te vergroten, door de nieuwe groeimode in gesputterde koperfilmen eveneens te introduceren in elektrochemisch afgezet koper. In een eerste fase worden een aantal gesputterde koperfilmen gecombineerd met elektrochemisch afgezette koperlagen van verschillende diktes. Er wordt aangetoond dat de nieuwe groeimode in gesputterd koper zich voortzet vanuit het gesputterde koper in het elektrochemische koper, en op die manier super grote korrels introduceert in het elektrochemisch koper. Een nadeel is dat voor dikkere elektrochemisch afgezette koperlagen, de korrelgrootte van de super grote korrels afneemt. Desondanks blijft de introductie van de superkorrels in elektrochemisch afgezet koper een belangrijke doorbraak. In een volgende stap wordt al deze kennis gebruikt om via enkele aangepaste metallisatieschema's superkorrels te introduceren in structuren. Er wordt aangetoond dat dit succesvol kan gebeuren, maar dat verdere optimalisatie van deze methode noodzakelijk is.

Hoofdstuk 6 geeft een samenvatting weer van de meest relevante resultaten en verwezenlijkingen van dit doctoraatswerk en werpt een blik op de mogelijke experimenten voor de toekomst.

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Kris Vanstreels
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List of publications

Journal papers:

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Chapter 1

Introduction

1.1 Cu replacing Al for IC interconnects

On-chip interconnects comprise a multilevel structure of fine wiring located on top of the transistor circuitry, as shown in figure 1.1. To avoid degradation of circuit speed, the interconnects should permit rapid signal transmission amoung the various parts of the integrated circuits (IC). Since the development of the first IC in 1958 by Jack Kilby and Robert Noyce, the most commonly used metal for fabrication of interconnects has been Al[1], in combination with SiO_2 as the intermetal dielectric (dielectric constant, k = 4) [1].

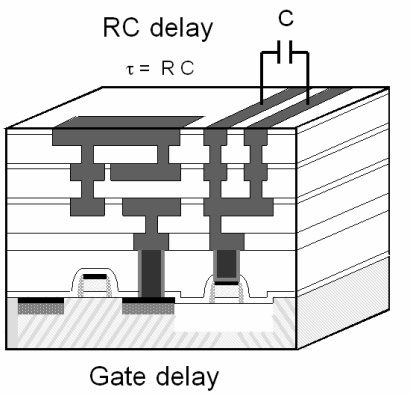

Figure 1.1: A typical chip cross section showing the hierarchical scaling of a multilevel interconnect system. Each interconnect layer comprises one layer of wires and one layer of vias.

The quest for continuous improvement in the performance of microelectronic devices has been the driving force for the semiconductor community for pursuing the so called "Moore's Law". In the sixties,

[1] *In order to enhance the electromigration resistance of Al interconnects, the Al is typically alloyed with 0.5 to 1% Cu*

Moore observed an exponential growth in number of transistors per integrated circuit, and postulated that this trend would continue [2]. For decades, scaling down of transistor sizes has been a very effective means of achieving these goals. The IC industry's continued demand for miniaturization and higher transistor packing density[2], brings along an increase in the interconnect density by reducing metal pitch and increasing the number of interconnect levels. A "roadmap" has been traced (and updated every year) for Si-based semiconductor technology defining the technological milestones of the miniaturization trend for the next decade (Table 1.1) [3]. However, as the technology keeps on improving generation by generation, the scaling of devices becomes less profitable. The limitations of the circuit speed and the maximum functional density become more dependent on the characteristics of the interconnects than on the scaled devices [4]. The integration of low resistivity copper metal wiring and a low-k ($k < 4$) intermetal dielectric has become crucial for next generation IC interconnect technology with low resistance-capacitance delay (RC-delay) and allowing higher current densities. The global shrinking of the dimensions, reflecting also a shrinking of the spacing between the interconnect wires, leads to an increase of the interconnect capacitance (C). This increase leads in return to an increase in the interconnect signal transmission delay τ and dynamic power consumption P:

$$\tau \sim RC \tag{1.1}$$

$$P \sim C f V^2 \tag{1.2}$$

with R the wire resistance, f the frequency and V the voltage for device operation. Downscaling of dimensions in the deep sub-micron range implies considerable challenges for the patterning and deposition technologies, and for thin film/small feature physical characterization. As shown in figure 1.2, when device scales are narrowed down to metal line width and spacings below 0.2μm, the signal propagation speed is dominated by the interconnect RC-delay instead of the transistor switching speed [5]. In this way, the performance and reliability achievable with aluminium alloy metallizations soon reaches practical limits as integrated circuit interconnect dimensions continue to diminish. Copper is an obvious candidate as a successor to aluminium. By adapting a Cu/low-k

[2] *Nowadays, a typical order of magnitude for the number of transistors integrated in microprocessors is 10^7-10^8*

interconnect scheme, as opposed to an Al/SiO_2 one, this trend can be effectively slowed down, mainly due to the lower bulk resistivity of copper and the smaller k-value of the dielectric material (see figure 1.2). Another expected benefit of a good-quality copper interconnect is a superior resistance to stress-voiding and a better resistance to electromigration (EM), thereby allowing it to carry much higher current densities for the same lifetime.

Year of production	2005	2007	2010	2013	2016	2020
DRAM ½ Pitch (nm)	80	65	45	32	22	14
MPU / ASIC ½ PITCH (nm)	90	68	45	32	22	14
Number of metal levels	11	11	12	13	13	14
MPU Physical Gate Length (nm)	32	25	18	13	9	6
Metal 1 wiring						
Metal 1 Wiring Pitch (nm)	180	136	90	64	44	28
Interconnect RC delay 1mm line (ps) for a 1mm metal 1 wire, assumes no scattering and an effective p of 2.2 μΩ-cm	307	486	966	1572	2943	6207
Interconnect RC delay 1mm line (ps) for a 1mm metal 1 wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	440	767	1792	3451	8040	23105
Barrier thickness for intermediate interconnect (nm)	6.5	4.8	3.3	2.4	1.7	1.1
Intermediate Wiring						
Intermediate Wiring Pitch (nm)	200	140	90	64	44	28
Interconnect RC delay 1mm line (ps) for a 1mm intermediate wire, assumes no	254	437	984	1596	2982	6287
Interconnect RC delay 1mm line (ps) for a 1mm intermediate wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	355	682	1825	3504	8147	23405
Barrier thickness for intermediate interconnect (nm)	7.3	5.2	3.3	2.4	1.7	1.1
Jmax (A/cm²) – intermediate wire (at 105°C)	8.91E+05	2.08E+06	5.15E+06	8.08E+06	1.47E+07	2.74E+07
Global Wiring						
Global Wiring Pitch (nm)	300	210	135	96	66	42
Interconnect RC delay 1mm line (ps) for a 1mm global wire, assumes no scattering and an effective p of 2.2 μΩ-cm	96	168	371	611	1157	2370
Interconnect RC delay 1mm line (ps) for a 1mm global wire, assumes width-dependent scattering and a conformal barrier of thickness specified below	111	209	523	977	2210	5795
Barrier thickness for intermediate interconnect (nm)	7.3	5.2	3.3	2,4	1,7	1,1
Bulk k-value	3.6	3.6	3.1	2.7	2.5	2.3
Effective k-value	4.1	4.1	3.4	3.0	2.8	2.6

Table 1.1: International Technology Roadmap for Semiconductors, 2005, interconnect section [3].

The RC-delay of the interconnect system can be reduced in two ways. First, the total resistance of the interconnect line can be lowered by introducing copper as the core metal for the interconnect metallurgy. This can mainly be ascribed to the lower bulk resistivity of copper as compared to aluminium ($\rho_{Cu} \cong 1.67\mu\Omega cm$; $\rho_{Al} \cong 2.65\mu\Omega cm$). Secondly, the side-by-side capacitance of interconnect lines can be reduced by either scaling down the Cu wire cross section or by using dielectric materials which have a lower k-value.

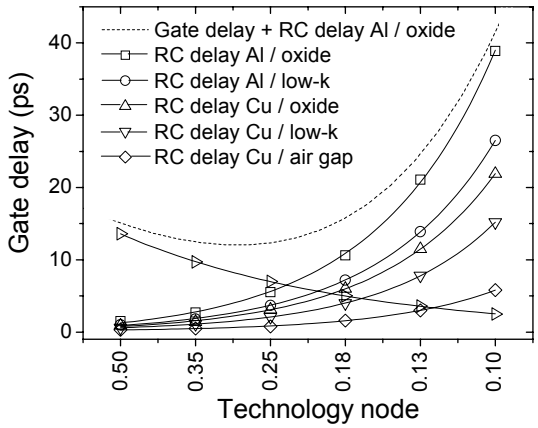

Figure 1.2: On-chip RC delay caused by devices and interconnects as a function of the feature size (in µm), replotted after Bohr [6].

Since copper metallurgy allows the use of smaller lines to carry the same amount of current, a tighter packing density can be achieved per interconnect level, which means that fewer levels of metal are needed in an IC, leading to significantly reduced manufacturing costs. Furthermore, any material change that can decrease the capacitance of all the interconnects will drop the power consumption (for the same current) making it attractive for battery powered portable systems. Other advantages of Cu interconnects, taking into account realistic fabrication processes, have been described in detail [7-8].

1.2 Motivation and outline of this thesis

The transition from aluminium to copper as the metal used in back-end-of-line (BEOL) interconnects was one of the most important changes in materials that the semiconductor industry has experienced since its creation. The introduction of copper as the new interconnect material has necessitated a firm understanding of the physical properties of this material in both thin films and narrow structures. As the dielectric constant (k-value) of the insulator needs to be reduced with each generation of technology, this implies that materials are constantly changing and serious investments need to be made for developing etch processes that are compatible with these new materials that range from SiOC:H to polymers. At the same time a regime has been entered where the metal line width is smaller than its depth. This implies that conformal deposition of copper will result in the formation of seams and voids. It quickly became clear that damascene patterning in combination with a sputter deposited copper seed layer followed by electroplating provided the most advantageous means of deposition in terms of costs, and equally important, defect-free filling of trenches [9-11]. The void-free filling of the trenches can be achieved through the use of several additives in the electroplating chemistry that result in an accelerated growth from the bottom of the trench upward, as described in the curvature-enhanced accelerator coverage (CEAC) model, developed by D. Josell et all [12]. Although the use of these additives in the electroplating chemistries facilitates the filling capability of high aspect ratio (AR) structures, these additives also includes two less desirable phenomena. Firstly, the accelerated 'bottom-up' growth tends to overshoot, producing large hillocks over patterned areas [13]. Secondly, as some additives tend to enhance nucleation of new grains during deposition, this will also lead to a reduction of the as-deposited grain size. Unfortunately the reduction in grain size also renders the deposit subcritical (~tens of nanometers for copper), leading to a grain growth process that proceeds even at room temperature, also known as self-annealing [14-16]. During this process, which can take place over a period of weeks, days, or even hours, secondary grain growth is observed where a few grains grow rapidly at the expense of other normal grains, resulting in a grain size distribution that is bimodal until completion of the transformation [17]. In electroplated thin copper films, the final grain size

for this growth mode is limited by the film thickness [15]. Typical grain sizes of up to several microns are obtained. However, in trenches the grain size can be even further limited by the physical size of the structure in which grain growth has to occur. Moreover, as the dimensions of these interconnects reach the sub-100nm regime, some fundamental and practical limits (e.g. the size effect) are being approached. The size effect refers to a phenomenon in which the electrical resistivity of thin metal films dramatically increases as the film thickness approaches the intrinsic electron mean free path, determined by electron-phonon scattering (~39 nm for bulk copper at room temperature), as shown in figure 1.3. In addition, the size effect embodies several electron scattering mechanisms such as surface scattering, grain boundary scattering and surface roughness which add to the classic electron-phonon scattering in bulk materials and cause a contribution to the resistivity of copper.

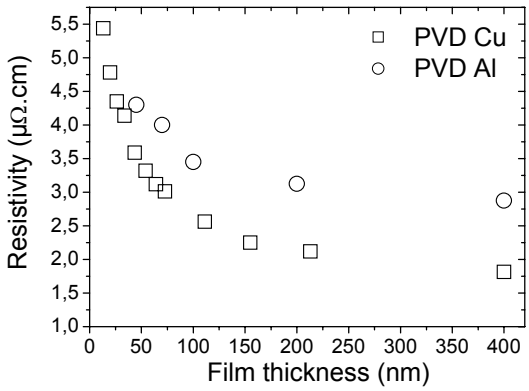

Figure 1.3: Resistivity of as-deposited physical vapour deposited copper and aluminium films versus the film thickness, illustrating the size effect in the ultra thin film regime (with courtesy of W. Zhang, et al.) [18].

As both the grain size and texture of polycrystalline copper thin films and structures are known to be critical factors in determining the electromigration resistance of copper interconnects, the issue of microstructure control of electroplated copper films with different processing parameters has been a focus of interest over the past decades. In order to minimize the impact of self-annealing on consecutive steps in

the processing of multilevel interconnect systems, and on the reliability and yield of Cu features, a firm understanding of this self-annealing phenomenon and textural development in copper films is desirable. More in particular, in case of narrow copper interconnect structures, this becomes even more challenging as the volume fractions of both the electroplated copper and sputtered copper are significantly changed when the features are scaled down and this may influence the self-annealing growth dynamics in those features. Moreover, as grain boundary scattering is one of the contributing factors to the resistivity of copper in small dimensional features, finding ways to increase the grain size is of significant interest.

Because copper interconnect structures contain both sputtered and electroplated copper, we will first focus our efforts in this thesis on understanding the self-annealing process and texture formation in sputtered copper seed layers using different deposition parameters. More specifically, these process parameters will be optimized in order to increase the final grain size in those films. Moreover, all results will be discussed and explained in terms of different self-annealing driving forces. In a next step, we will illustrate that by combining these sputtered copper films with electroplated copper films we can also initiate those very large grain sizes in seed layer/electroplated systems. Finally, the obtained knowledge on a blanket wafer level will be used in order to try to increase the mean grain size in patterned structures, thereby reducing the size effect and thus the interconnect resistance. All these issues will be discussed in the next five chapters.

The second chapter is a general introduction to grain growth in thin polycrystalline films during and after deposition and their mechanical properties. This is necessary for introducing the main concepts and terminology recurrent in this work.

In chapter 3, an overview is given of the experimental techniques we used in this work.

Chapter 4 is dedicated to grain growth and mechanical properties in sputtered copper thin seed layers. Emphasis is put on studying the effect of

the annealing temperature and several processing parameters like the copper sputter bias and copper film thickness on the growth dynamics and texture formation in thin copper films. It will be shown that for certain film thicknesses and copper bias conditions, a new (abnormal) grain growth mode can be obtained in these copper seed layers, named super secondary grain growth (SSGG). This SSGG growth mode drives the system to a {100} texture with grain sizes in the order of several hundreds of microns. Under certain deposition conditions, the appearance of these so-called super grains is strongly dependent on the barrier layer microstructure. Furthermore, it will be shown that strain energy minimization is a very important driving force for this growth mode.

Chapter 5 is dedicated to the introduction of the newly observed SSGG growth mode from the sputtered copper seed layer into the electroplated copper. This is significant as in practice the small features are mainly filled with electroplated copper, and thus it is not only important to initiate super grains in sputtered seed layers, but also check the feasibility of the SSGG growth mode in electroplated copper. It will be shown that super grains can be initiated in electroplated films of different thicknesses on top of thick sputtered seed layers. Moreover, we will show that the growth dynamics of these super grains is influenced by the thickness of the electroplated copper. In a next step this knowledge is used in an attempt to initiate super secondary grains in structures. For this purpose, two different methods are proposed and their efficiency on initiating super grains in structures will be evaluated.

Finally, in chapter 6, the conclusions together with some perspectives are given.

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Chapter 2

State-of-the-art

Polycrystalline thin films are used in a wide variety of applications in electronic, magnetic, chemical, micromechanical devices and in many other systems which are not all mentioned here [1-7]. In these applications, the term thin films is usually taken to apply to films with a thickness of around 1μm or less. Films with these thicknesses often have non-equiaxed grains that span the thickness of the film but have in-plane sizes ranging from much smaller than the film thickness to much larger than the film thickness. Due to their highly constrained microstructural characteristics, the physical properties of thin metal films and interconnects are very sensitive functions of microstructural features like the grain geometry, grain size, grain size distribution and the distribution of grain orientations. This often results in an unusual mechanical behaviour, which in turn affects their properties, performance and reliability. The typical grain structure characteristics of these films are often defined by grain growth occurring during and after film formation [8]. Therefore, an understanding of the different factors that control the microstructural evolution in thin films is necessary for the development and design of reliable, manufacturable interconnect structures, especially in damascene-processed trench interconnects. As a result, in the last decade, grain growth and textural evolution has been the subject of several experimental and theoretical reviews [9-12]. The purpose of this section is to briefly review the general phenomenology, key characteristics and current understanding of microstructural and textural development during and after processing of polycrystalline thin films. Because in this work only copper films are studied, we will specifically focus on face-centered-cubic (FCC) systems. In section 2.1, the microstructural evolution during processing of polycrystalline thin films will be discussed. Section 2.2 describes the different types of stress that can arise in thin films. Section 2.3 focuses on grain growth and textural development during post-deposition processing of polycrystalline thin films and the different available sources of energy to control thin film microstructures during grain growth. Finally, section 2.4 summarizes this chapter.

2.1 Thin film formation

Figure 2.1a shows, in very simple form, the fundamental process through which the grain structure of polycrystalline thin films develops during film deposition. In a first stage of the three-dimensional polycrystalline film formation, isolated crystals or nuclei are formed. This process can be discussed in terms of condensation of a solid film from a vapour phase, the most common case, but similar phenomena also occur during film formation by electrodeposition or other deposition techniques. As adatoms (i.e. incoming atoms on the growing film surface) arrive and adsorb on the substrate surface, they remain adsorbed for a certain time τ. Nucleation occurs when stable clusters of adatoms form and continue to grow rather than dissolving back to smaller clusters and single adatoms. When critical cluster sizes are sufficiently large that the crystallography of the nucleating phase is defined, specific nuclei crystallographic orientations will minimize surface and interface energies at the free surface and film substrate interface [13]. This will then lead to higher nucleation rates for nuclei with energy minimizing orientations. In case of face-centered-cubic materials like copper, this will promote the growth of (111) oriented grains, as for these materials the close-packed (111) surface has the lowest surface energy [14].

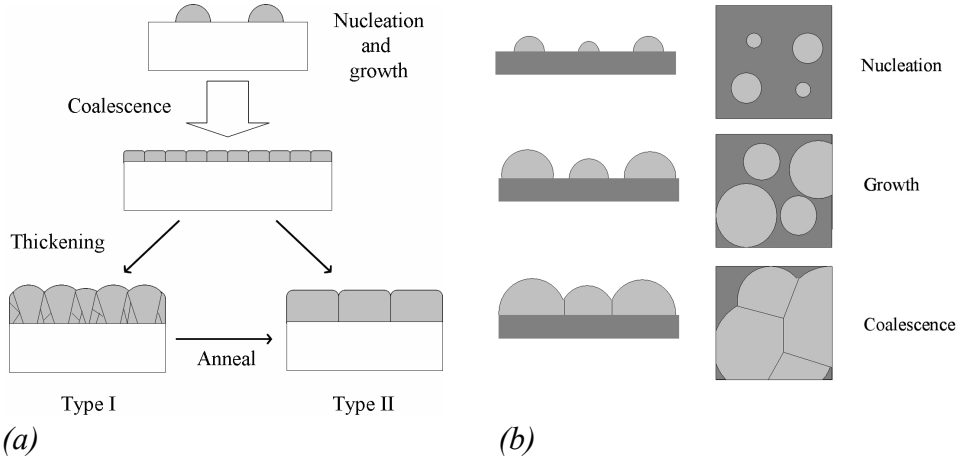

Figure 2.1: (a) schematic cross sectional overview of different stages of formation of a polycrystalline thin film; (b) nucleation, growth, and coalescence to form a continuous thin film.

During further growth of nuclei into islands (both external and lateral), these islands of a given volume will have total energies that vary with their crystallographic orientations relative to the plane of the interface and relative to the atomic level structure and symmetry of the substrate. Eventually, the lateral growth leads to impingement of islands to form a continuous network. This nucleation, growth, impingement, and coalescence process is schematically illustrated in figure 2.1b. During island growth, some islands may often grow at the expense of other islands which have a higher energy per atom. This can occur through detachment of atoms from islands and diffusion of atoms on the surface to attach on other islands, resulting in the shrinkage and even disappearance of some islands and the growth of other islands. Such processes, also called coarsening, would be driven by differences in the average energy per atom for islands of different sizes. In general, the free energy per atom will be a function of the island size and of the total surface and interface energies of the island. Because the surface and interface energies are a strong function of the crystallographic orientation of a certain island relative to the orientation of the substrate and other islands, driving forces for the coarsening process are also orientation dependent. Therefore, pre-coalescence island coarsening favours the growth of islands with specific surface and interface minimizing crystallographic orientations, i.e. (111) orientation for FCC materials. The transition from isolated islands to a continuous macroscopic network can be characterised by a certain threshold film thickness, also called the percolation thickness. For many films this thickness varies around 1-20nm. However, for most applications further thickening of the film is required. Once the percolation thickness is reached, further deposition does not simply increase film thickness. Depending on the interaction energies of substrate atoms and film atoms, the films can grow either layer by layer (Frank-van der Merwe mode), by islands (Volmer-Weber mode), or by a combination of both layers and islands (Stranski-Krastanov mode) [15-17]. In general, it is recognized that thin films show a wide variety of microstructures where the microstructure and properties of a thin film strongly depend on the deposition process and the used process conditions. In case of physical vapour deposition the major process control parameters are substrate temperature (determining the surface mobility), the background gas pressure (determining the mean free path within the plasma, which determines the extent to which the growing film is subjected to bombardment by energetic particles), and the energy, flux and angle of

incidence of the depositing particles (atoms and/or ions). Ordinary microstructures of thin films produced by PVD are usually described by maps, as a function of deposition parameter. These maps are also referred as zone models. In the simplest case, as proposed by Movchan and Demchishin [18], a real structure exists in three zones, depending on the substrate temperature relative to the melting temperature ($T_r=T/T_m$). According to this model, microstructural development is controlled by geometric interactions between the arriving adatoms and the roughness of the growing film surface (zone 1; fine-grained real porous structure), by surface diffusion (zone 2; columnar real structure) and by bulk diffusion (zone 3; equiaxed grained real structure). How low T_r must be to get a zone 1, zone 2 or zone 3 microstructure depends on the grain boundary mobility, which in turn depends on the materials class and the film purity [19-20]. Film purity is affected by deposition conditions like vacuum level and deposition rate. Thornton noted that in sputter deposition, adatom mobilities are affected by the energy with which the atoms arrive at the film surface [21-24]. The energy is affected by the number of collisions the arriving atom has with sputtering gas atoms, which scales with the pressure of the sputtering gas. This basically means that a reduction in gas pressure leads to a more energetic ion bombardment of the film surface. Thornton extended the Movchan and Demchishin model by including the sputter gas pressure as an additional parameter [21-24]. Thornton identified a transition zone between zones 1 and 2 consisting of a dense array of poorly defined fibrous grains. The zone diagrams of Movchan & Demchishin and Thornton are useful tools for semi-quantitatively capturing and illustrating the expectations for structural evolution as a function of process parameters, deposition temperature and pressure. Besides the sputtering gas pressure, the adatom mobility can also be affected by the nature of the vapour species, the used sputter bias voltage and bombardment by energetic particles. Messier included the influence of bombardment by energetic particles into the zone models and showed that this actually can influence the microstructure [25-26]. Grovenor et al. took the influence of the morphology into consideration [27]. Finally, it is also important to recognize that in general, film purity (whether impurities are intentionally added or not) can also significantly affect the T_r values associated with transitions in growth modes in a particular material class. Post-depositional grain growth can occur at room temperature and/or during additional annealing steps with either type of as-deposited structure, as will be further discussed in section 2.3

2.2 Stress in polycrystalline thin films

2.2.1 Intrinsic stress

It is well known that as-deposited thin films often develop large intrinsic stress during their deposition. As most of the growth processes in thin films are kinetically controlled, thin films in general contain many defects of different types, which cause departures from the ideal crystal structure and thus may act as potential sources of stress. Intrinsic stress can either originate from strained regions within the films (grain boundaries, dislocations, voids, impurities, etc…) or from strained regions at the film/substrate (lattice mismatch, different thermal expansion, etc…) and film/vacuum interfaces (surface stress, adsorption, etc…). Since the magnitude of most of these stress contributions is directly related to the film morphology, important structural information can be extracted from measurements of the intrinsic stress. In the past decades, intrinsic stresses have been extensively studied during and after evaporative deposition of thin films [28-31]. It was found that when films were deposited at room temperature, basically two different types of stress behaviour (type I and type II) were found and correlated with two different modes of island growth, depending on the mobility of the studied materials (figures 2.1 and 2.2.).

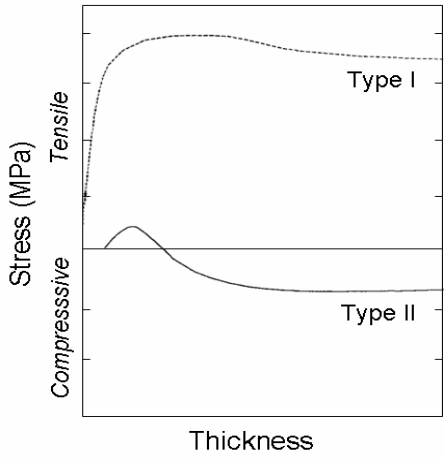

Figure 2.2: comparison of stress evolution for type I and type II materials as a function of the film thickness, based on [30]

For many of Type I materials or low mobility materials like for instance Cr, with typical microstructures such as shown in figure 2.1a, high tensile stresses in sputtered and evaporated thin films have been observed [32]. Hoffmann proposed that tensile stresses in these films develop as islands coalesce, as a result of nearby islands elastically deforming to close up spaces in order to replace the two grain-free surfaces with one grain boundary [33]. Moreover, the maximum stress that can result from this mechanism is strongly dependent on the grain size at coalescence. For sufficiently small grain sizes at coalescence (< 10nm) this can lead to stress values in the order of several GPa. This provided a likely explanation for the observed large tensile stresses in many type I materials. Type II materials or high mobility films, like Al and Cu, develop small tensile stresses as they coalesce, but this stress is then relieved, and even appears to become compressive as the film thickens. According to the stress model of Abermann et al. [34-35], the film forces in the discontinuous films are tensile due to the formation of grain boundaries and grain growth. The origin of the compressive stresses when the films are continuous can be attributed to surface stress effects [28-31]. Moreover, it was found that the nature of intrinsic stresses of polycrystalline films is mainly determined by the mobility of the film atoms [36-37]. A major external parameter to control the film diffusivities is the substrate temperature. If the self-diffusion of the deposited material is high enough, grain growth may occur during and also after film formation. During such processes, all kinds of defects (grain boundaries, voids, point defects, etc...) are eliminated, leading to a shrinkage or densification of the films and a tensile stress contribution. This "densification" strain and stress can be quite high, depending strongly on the grain size at coalescence.

2.2.2 Extrinsic stress

In contrast to the stress mechanisms discussed so far, a possible source for extrinsic stresses can be differential thermal expansion. As thin films on substrates are often deposited at a temperature different from the temperature at which grain growth is observed, and because the film and the substrate in general have different thermal expansion coefficients, this can lead to significant tensile or compressive extrinsic strains. These strains are not the result of the growth process, but usually arise when the

external parameter "temperature" T is changed after the film deposition, because the film-substrate adhesion forces the film to maintain the dimensions of the substrate. As a consequence, thermal strain must be accommodated by elastic and plastic strains. In continuous films, these strains are largely biaxial in the plane of the film when heated at temperatures higher than the deposition temperature. If we only focus on the elastic temperature range, this biaxial strain resulting from the differential thermal expansion of a thin film on a thick substrate leads to a thermal stress approximated by

$$\sigma_{th} = M \int_{Tdep}^{T} (\alpha_S - \alpha_F) dT \cong M(\Delta\alpha)(\Delta T) \qquad (2.1)$$

where $\Delta T = T - T_{dep}$ is the difference between the actual temperature T and the deposition temperature and M is the biaxial modulus of the film. Moreover, α_F and α_S are respectively the thermal expansion coefficients of the film and substrate. Thermal expansion coefficients of most metals are typically one order of magnitude higher than the expansion coefficient of Si. However, when the thermal strains exceed the elastic limit of the film, they are relaxed by various deformation mechanisms including the constrained movement of dislocations, grain boundary diffusion, different strengthening mechanisms or a combination of one or more of the preceding mechanisms. The investigation and understanding of all these complex inelastic mechanisms is not straightforward and is beyond the scope of this work. Here, we will only focus on the elastic regime to explain the textural evolution in the sputtered and electroplated copper films. For more details about the different deformation mechanisms that may occur in polycrystalline thin films, we refer to [38-40].

2.3 Grain growth and textural development during post-deposition processing of thin films

As discussed earlier in section 2.1, grain growth can play a dominant role in defining the texture and grain size distribution during processing of polycrystalline thin films, and therefore also on their mechanical properties in the as-deposited state. After a film is processed with an as-deposited structure A or B on figure 2.3, it can develop to a structure C on

figure 2.3 through grain growth during post-depositional heating or during grain growth at room temperature, also called self-annealing. During this grain growth, the as-deposited texture may change. The evolution of the microstructure and texture during post-depositional processing depends strongly on the experimental parameters used for the film deposition. The current understanding of grain growth in thin films will now be briefly reviewed.

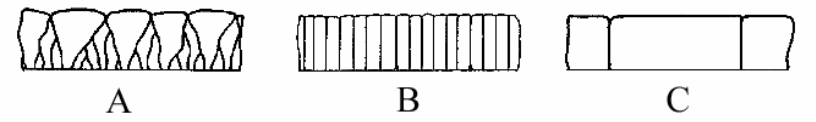

Figure 2.3: schematic cross sectional views of three possible grain structures of as-deposited thin films with thickness less than 1μm

2.3.1 Sources of energy to control thin film microstructure

In literature, the well-known mechanisms for microstructural evolution in bulk systems have been often used to explain microstructural evolution in thin films [41-43]. It is assumed here that the driving force for grain growth is a summation of a term related to the grain boundary energy and mobility, a term related to the difference in elastic or plastic strain energy between neighbouring grains due to external forces and dislocations, a term related to stress anisotropy due to dislocation arrays, and a term related to the difference between surface and interface energies of neighbouring grains. It is usually assumed that a "pinning force" caused by particles or impurities that are present at the grain boundaries (Zener pinning) may oppose all of the aforementioned driving forces [44]. The texture then develops in such a way that the energy of the system can be minimized. The final grain size, grain size distribution and texture depend on the relative magnitudes of the driving forces, which can be influenced by the experimental parameters and by the post-deposition process itself. Discussing grain growth and microstructural evolution in terms of several driving forces responsible for the growth of certain grains or orientations is necessary to determine the kinetics of microstructural evolution [8, 45-46]. However, also a useful comparison of mechanisms may be made by

considering the sources of energy available to drive microstructure changes [47]. For copper films in the range of 0.1-1.0µm, the energy density for several mechanisms that can influence the thin film microstructures can be estimated and are tabulated in Table 2.1.

Mechanism	Equation	Assumption	ΔE in MJ/m³
Grain boundary energy	$E_{gb,2D} = \frac{3}{2} E_{gb,3D} = \frac{2\gamma_{gb}}{d_0}$	d_0= 0.1µm γ_{gb} = 0.625J/m²	$E_{gb,2D}$ ≈ 10-15
			$E_{gb,3D}$ ≈ 15-20
Surface energy	$E_{s,i} = \frac{\Delta\gamma}{h}$	h = 1.0 µm	≈ 0.02
Elastic strain energy	$E_{strain} = 146.4\varepsilon^2$	ε = 0.2%	≈ 1
Dislocations	$E_{disl} = ½ \rho G b^2$	ρ = 10^{12}-10^{13}/cm²	≈ 15-140
Zener pinning	$E_{Zener} = -\frac{3\gamma_{gb}\rho_p}{2r_p}$	ρ_p = 0.2% r_p = 0.1nm	≈ -20

Table 2.1: Sources of energy to control thin film microstructure

A first contribution to grain growth results from the energy that can be gained by eliminating the grain boundary area in the film. In thin films, two-dimensional (columnar) and three-dimensional (non-columnar) grain growth can be distinguished, and the corresponding energy stored in the grain boundaries for both growth modes can be approximated by $E_{gb,2D}$ = 2/3 $E_{gb,3D}$ = $2\gamma_{gb}/d_0$, where γ_{gb} is the grain boundary energy per unit area and d_0 is the initial grain diameter. An upper limit for this driving force

can be calculated assuming that all grain boundaries in the as-deposited film are high-angle grain boundaries with a grain boundary energy per unit area of about 0.625J/m² [48-49]. The energy released is then given by the product of the grain boundary energy and the area of the eliminated grain boundaries. One may also estimate the driving forces for grain growth caused by anisotropic surface/interface and strain energies. The difference between the surface/interface energies of (100) and (111) grains is estimated to be about 20kJ/m³ for 1μm thick Cu films [50]. Moreover, anisotropy in either the thermal expansion and/or the elastic properties of the film will result in a dependence of the elastic strain energy density on the orientation of the grains. These differences can drive or suppress grain growth depending on whether or not strain energy density minimization dominates surface and interface energy minimization. In case of face-centered-cubic materials, the maximum driving force caused by a difference in elastic strain energy between two grains is given by $E_{strain} = 146.4\varepsilon^2$, with ε as the strain [51]. By assuming the strain in the range of 0.2%, this energy can be estimated in the order of 1MJ/m³. The strain energy in the regime of plastic deformation may also provide a driving force for the growth in thin films. This might happen through different deformation mechanisms that occur in these thin films, including the constrained movement of dislocations, grain boundary diffusion, different strengthening mechanism including strain hardening or a combination of the preceding mechanisms. These complex deformation phenomena are referred in literature as yielding. For more details we refer to [38-40]. Another type of defects are dislocations within the as-deposited grains. The strain energy associated with one dislocation may be estimated by $E_{disl} = ½ Gb^2$, with G = 4.21 x 10^{10} N/m² and b = 0.256nm as the Burger's vector along the <110> direction in case of FCC copper. For an areal density ρ of dislocations, the stored energy is then given by $E_{disl} = ½ \rho Gb^2$. Assuming a hypothetical density of around 10^{12}-10^{13}/cm² [52], this leads to an energy release of about 15-140 J/cm³. For completeness, we also include the Zener pinning mechanism because of its importance in electroplated films. The driving force for Zener pinning (actually Zener pinning force) is given by $E_{Zener} = -3 \gamma_{gb}\rho_p/2r_p$, with ρ_p as the volume fraction of pinning particles and r_p as their radius. In table 2.1, the values for these parameters were chosen to illustrate that the pinning force related to the Zener mechanism may actually balance the driving force that originates from eliminating grain-boundary area.

2.3.2 Normal and abnormal grain growth in thin films

Grain growth in polycrystalline thin films may appear either as normal or abnormal grain growth. In case of normal grain growth, the grain growth is basically driven by the reduction in the total grain boundary area and in the corresponding reduction in the total grain boundary energy that accompanies the area decrease. This growth mode is often observed in bulk materials and has been the subject of a number of reviews [9, 53]. When grain boundary energy reduction alone drives grain growth, the average in-plane growth velocity can be written as [53],

$$v = \frac{dr}{dt} \propto \frac{2m\gamma_{gb}}{d} = \frac{m\gamma_{gb}}{r} = m\gamma_{gb}\kappa, \qquad (2.2)$$

hereby assuming that cylindrical grains of radius r and thickness h grow into a uniform matrix characterised by an average grain boundary energy per unit volume E_{gb}. In this equation, r and γ_{gb} are respectively the average grain radius and the average grain boundary energy per unit boundary area. Furthermore, m is the average grain boundary mobility and κ is the average boundary curvature, which in case of a circle is equal to 1/r. From equation (2.2), it is expected that the average grain diameter d changes with time t according to

$$d - d_0 \propto t^{1/2} \qquad (2.3)$$

where d_0 is the average grain diameter at t = 0. Normal grain growth is also characterised by a "steady state" behaviour for which the shape of the grain size distribution is monomodal and will be time-invariant [54-55], meaning that the function describing the distribution of normalised grain sizes (i.e. the grain sizes divided by the median grain size) is time independent. This is illustrated schematically on figure 2.4a, where top views of a hypothetical grain size distribution of grains are shown at several stages of normal grain growth. During normal grain growth, some grains grow and some grains shrink. The corresponding increase in the average grain size leads to a corresponding decrease in the total grain boundary area. This results in a decrease in the energy of the system due to the reduction of the excess free energy associated with grain boundaries. For simplicity, it will be assumed that all grain boundaries

have the same energy per unit boundary area, γ_{gb}, corresponding to the average over the system.

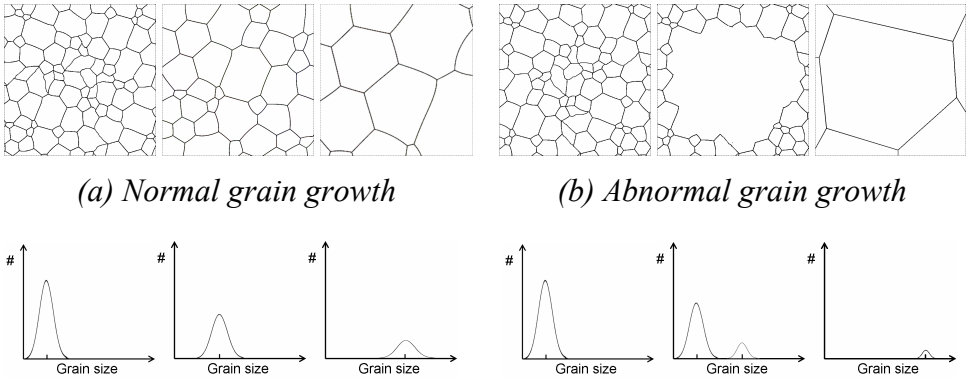

Figure 2.4: top view grain size distribution at different stages of normal and abnormal grain growth.

When the initial structure has a grain size that is not uniform through the film thickness like on figure 2.3A, there will first be an important three-dimensional component to the grain growth until the vast majority of grain boundaries traverse the thickness of the film. Once a quasi two-dimensional structure develops, further grain growth occurs primarily through motion of boundaries in directions lying in the plane of the film. In this case, the mean energy density (energy per unit volume) change associated with a change in average grain size from d_0 to d would be

$$\Delta E_{gb,2D} = \gamma_{gb}\left(\frac{2}{d_0} - \frac{2}{d}\right) = \frac{2}{3}\Delta E_{gb,3D} \qquad (2.4)$$

The subsequent grain growth process can then be modelled as a quasi two-dimensional process. Several computer simulations of two-dimensional grain growth have been reported in literature [56-57]. These simulation experiments all reveal a growth behaviour consistent with the expectations for two-dimensional normal grain growth. Moreover, it has been shown that in this case the time-invariant grain size distribution is well fit by a Weibull distribution function [54]. Despite the fact that two-dimensional normal grain growth can easily be modelled or simulated, and that in

practice thin films with structures as shown in figure 2.4a are very attractive candidates for testing those models, two-dimensional normal grain growth rarely occurs even in films with quasi-2D structures. In practice, grain structures of films that have undergone grain growth do not have grain size distributions that are well fit by Weibull distribution functions, but are instead well fit by lognormal grain size distributions [58-60]. Moreover, when grain growth leads to grain sizes significantly larger than the film thickness, it usually involves the favoured growth of a subpopulation of grains with specific crystallographic textures. In this case, some grains with specific crystallographic texture can grow at faster rates and grow by annihilation of the surrounding normal grains. The shape of the grain size distribution in this case is bimodal and evolves until the portion of the population which is not favoured is eliminated. As illustrated in figure 2.4b, this means that at some point in time, there is a population of small grains and large grains and the shape of the grain size distribution is not time-invariant. In literature, this growth mode is referred as abnormal grain growth and since abnormal grain growth often occurs after significant normal grain growth, it is also known as secondary grain growth [61]. There can be several reasons why in most of the cases abnormal grain growth is observed instead of normal grain growth. In some cases, grooves can be formed where grain boundaries intersect the surfaces of the film due to the balance of the surface energies of neighbouring grains with the energy of the boundary between the grains [62-63]. The formation of these grooves can suppress or even pin grain boundaries and cause stagnation of grain growth for some subpopulations [9, 56, 62]. Sometimes, this can even lead to a complete grain growth stagnation. Simulations have also shown that groove-induced stagnation leads to lognormal size distributions [9, 57-58]. Another possible reason for abnormal grain growth is that there are almost always grain-orientation-specific driving forces for grain growth. These grain-orientation-specific driving forces for grain growth can arise from several different sources like for instance the minimization of both surface and interface energies and/or the minimization of strain energy densities. Both driving forces have been shown to lead to abnormal grain growth and textural evolution in a large number and wide variety of experimental systems.

2.3.3 Surface/interface energy driven abnormal grain growth

As thin films are not two-dimensional, they have top and bottom surfaces that also have excess free energies per unit area. The energy on the top surface of a grain γ_s is determined solely by the texture of the grain, while the film-substrate interface energy γ_i mainly depends on the in-plane orientations of the grain lattice with respect to the substrate lattice, and on the orientation of the interface plane (figure 2.5). Therefore, these free energy differences at top and bottom surfaces between grains with different textures and/or in-plane orientations contribute a large fraction to the total free energy of the film, and thus play significant roles in the grain growth process. Here, grains with low surface and interface energies will absorb the grains with higher energies. Therefore, there are specific grain orientations that can lead to minimum surface energies and other orientations that lead to minimum interface energies. While these are not necessarily the same orientations, one energy will dominate so that there will be grain orientations that minimize the sum of the surface and interface energy, i.e. surface/interface energy minimization. In this case, the local growth velocity v of a grain boundary is dependent on both curvature κ and the out-of plane boundary curvature $\Gamma_{s,i}^{1,2}$ arising from the two grains meeting at the grain boundary. Specifically, the local boundary velocity v and $\Gamma_{s,i}^{1,2}$ are given by

$$v = m\gamma_{gb}(\kappa + \Gamma_{s,i}^{1,2}), \tag{2.5}$$

where

$$\Gamma_{s,i}^{1,2} = \frac{\Delta\gamma_{s,i}^{1,2}}{\gamma_{gb} h} \tag{2.6}$$

Moreover, h is the film thickness and $\Delta\gamma_{s,i}^{1,2}$ is the difference in surface and interface energy per unit boundary area between two grains meeting at the grain boundary. When $\Gamma_{s,i}^{1,2}$ is zero for all boundaries, equation (2.5) is reduced to $v = m\gamma_{gb}\kappa$, and normal grain growth will occur. The mean energy density change arising from surface and interface energy minimization during grain growth is given by

$$\Delta E_{s,i} = \frac{\Delta\gamma_{s,i}}{h} = \frac{\Delta\gamma_s + \Delta\gamma_i}{h} \tag{2.7}$$

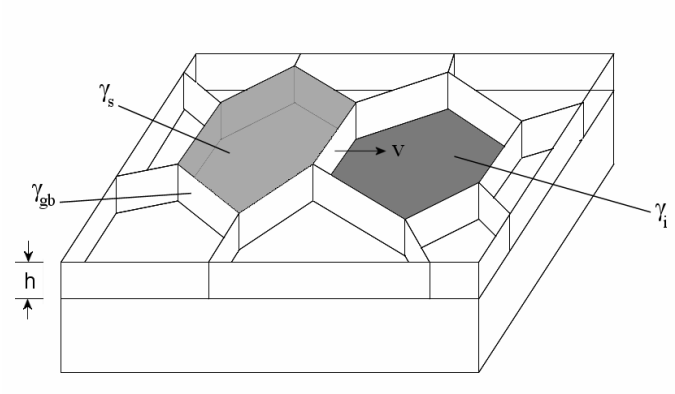

Figure 2.5: schematic overview of a polycrystalline film of thickness h with an equiaxed columnar structure. γ_s, γ_i and γ_{gb} are respectively the surface energy, interface energy and grain boundary energy per unit area.

where $\Delta\gamma_s$ is the difference in the average surface energy of the film per unit area and $\Delta\gamma_i$ is similar defined for the interface. Since the interface energy differences which distinguish grains are only present at the top and bottom surfaces, this energy term is not exactly an energy per unit volume. However, an estimate of its importance may be made by assuming a film of thickness 1µm and calculating the magnitude of the interface energies per unit film volume for this thickness. The net interface energy including the top and bottom interfaces is about 20kJ/m³ for a 1µm thick film (see table 2.1). As can be seen from equation (2.7) the effect of surface and interface differences becomes more important in thinner films. Clearly, if the film thickness is only 0.1µm, the energy density available from interface energy minimization is 10 times higher per unit volume, and can therefore dominate textural evolution. The development of a strong {111} texture typically observed in FCC metal thin films is thought to be due to the minimization of the surface/interface energies at the free surface and film substrate interface, as for all FCC metals, the close-packed (111) surface has the lowest surface energy [14]. This is illustrated in figure 2.6, where the surface energy was calculated with the broken bond model and the energy of 2.610 J/m² was used [64-65]. In this case the (111) orientation is thought to minimize both the surface and interface energies, which means that the growth of grains with {111} texture is generally favoured over growth of grains with other orientations.

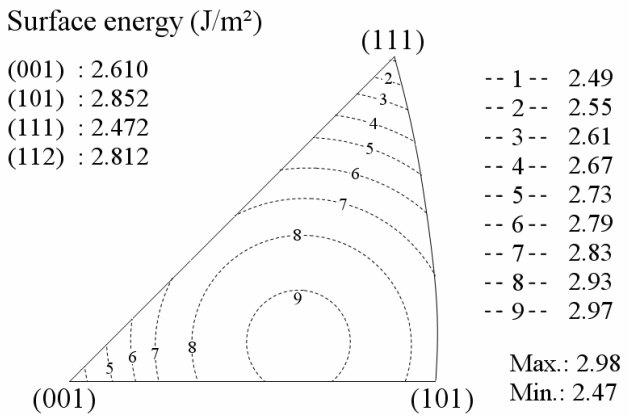

Figure 2.6: Anisotropy of the surface energy of Cu, calculated with the Broken-Bond Model and presented in a stereographic unit triangle [65].

2.3.4 Strain energy driven abnormal grain growth

Another important aspect of the energy driven aspects of grain growth in thin films is that these films are often under high intrinsic or extrinsic stresses. High intrinsic stresses in these films can arise during coalescence. This is because the density of a film is reduced by the presence of grain boundaries. Grain boundaries have an excess free volume per unit area, Δa, when compared to single crystal materials, which in case of FCC materials is around 1Å [66]. As grains grow and coalesce, this free energy volume is redistributed and results in a biaxial strain given by

$$\varepsilon_d = \Delta a \left(\frac{1}{d} - \frac{1}{d_C} \right) \tag{2.8}$$

where d is the grain size and d_c is the grain size when the film coalescence occurs. This "densification" strain can be quite high, depending strongly on d_c. If this strain is elastically accommodated, grain growth can lead to a significant change in the average energy density

$$\Delta E_d = M \varepsilon_d^2 \tag{2.9}$$

where M is the average biaxial modulus. Notice that in this equation M is assumed not to change during grain growth. In addition, an important source for extrinsic stresses is the difference between the thermal expansion coefficients of a thin film and the substrate (see section 2.2). Due to this difference and because most thin films are deposited at temperatures different from the temperature at which grain growth occurs, this can lead to significant tensile or compressive extrinsic strains. In the thermoelastic regime, the biaxial strain resulting from the differential thermal expansion is given by

$$\varepsilon_{th} = \int_{Tdep}^{T} (\alpha_S - \alpha_F) dT \cong (\Delta\alpha)(\Delta T) \tag{2.10}$$

where $\Delta T = T - T_{dep}$, and where α_F and α_S are respectively the thermal expansion coefficients of the film and substrate. Strain in continuous films due to different thermal expansion coefficients is largely biaxial in the plane of the film and can be quite large even for relatively small ΔT's. The anisotropic nature of strain can strongly influence the film microstructure. A thin film on a thick substrate is generally in an equibiaxial strain and equibiaxial plane stress state, mainly due to their attachment to much thicker substrates. Here, grains with different textures will have different in-plane elastic constants, due to elastic anisotropy. In the elastic regime, this will eventually lead to a texture dependent state of stress, and therefore a texture-dependent strain energy density. An elastically deformed grain with a (hkl) orientation subjected to a biaxial strain ε and under plane stress conditions, has an in-plane stress given by

$$\sigma = M_{(hkl)}\, \varepsilon \tag{2.11}$$

where the strain ε is composed of several strain contributions such as the intrinsic strain ε_i, strain due to densification ε_d, and thermal strain ε_{th}:

$$\varepsilon = \varepsilon_{th} + \varepsilon_d + \varepsilon_i \tag{2.12}$$

When elastically accommodated, this results in an elastic strain energy density given by

$$E_\varepsilon = M_{(hkl)}\, \varepsilon^2 \tag{2.13}$$

This strain energy density depends on the magnitude of the strain ε and the orientation of a grain, and therefore varies from grain to grain due to the orientation dependence of the biaxial modulus $M_{(hkl)}$. This orientation dependence can lead to abnormal grain growth in which growth of grains with low strain energy density orientations are favoured over grains with higher strain energy densities. Figure 2.7 shows the strain energy normalised by the square of the biaxial strain, in units of 10^9 J/m³ [51].

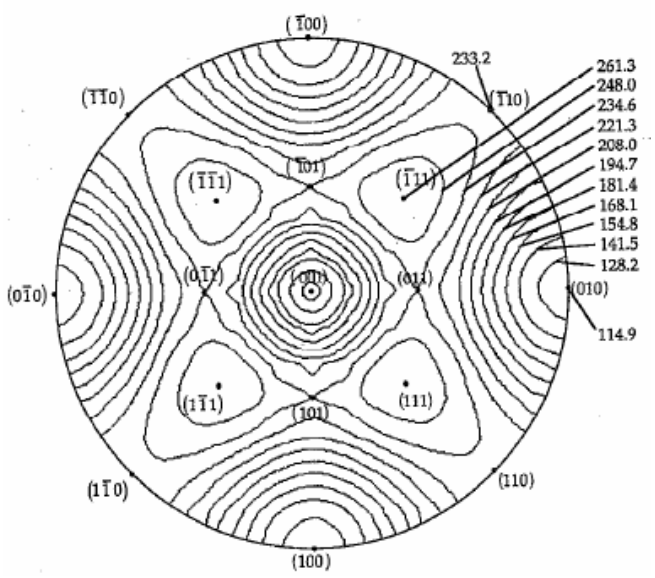

Figure 2.7: strain energy normalised by the square of the biaxial strain, in units of 10^9 J/m³, plotted on a standard (100) stereographic projection. This reveals the energetic advantage of the {100} family of orientations [51].

The stiffness constants used here are c_{11} = 169GPa, c_{12} = 122GPa and c_{44} = 75.3 GPa [67]. As shown, for FCC materials like Cu the strain energy density has a minimum value for grains with {100} texture and a maximum for grains with {111} texture. Moreover, the figure also shows that the strain energy density variation is low as the orientation is varied from (111) to (110), but that it decreases sharply as the orientation is varied from (111) to (100). Therefore, in biaxially strained films, the strain energy differences of grains with different orientations may contribute to

the driving force for secondary grain growth, thereby favouring grains with orientations that minimize the strain energy density. In case of face-centered-cubic metals this will lead to {100} textured films. Taking this into account, equation (2.5) and (2.6) can be further adapted so that the local in-plane growth velocity v of a grain boundary between two adjacent grains with orientations $(h_1k_1l_1)$ and $(h_2k_2l_2)$ is given by

$$v = m\gamma_{gb}(\kappa + \Gamma_{s,i}^{1,2} + \Gamma_{\varepsilon}^{1,2}) \tag{2.14}$$

where

$$\Gamma_{s,i}^{1,2} = \frac{\Delta M_{1,2}\varepsilon^2}{\gamma_{gb}} \tag{2.15}$$

and

$$\Delta M_{1,2} = M_{(h_1k_1l_1)} - M_{(h_2k_2l_2)} \tag{2.16}$$

where ΔM is the difference in the biaxial moduli of grains with textures $(h_1k_1l_1)$ and $(h_2k_2l_2)$ meeting at the grain boundary, and the corresponding strain energy density difference of the two grains is given by

$$\Delta E_{\varepsilon}^{1,2} = \Delta M_{1,2}\varepsilon^2 \tag{2.17}$$

In general, the mean energy density change arising from strain energy density minimization is given by

$$\Delta E_{\varepsilon} = \Delta M\varepsilon^2 = \left(M - M_0\right)\varepsilon^2 \tag{2.18}$$

where ΔM is the difference in the average effective biaxial modulus of the film before and after grain growth. This expression allows for the fact that as texture evolves during grain growth, M will change.

2.3.5 Competition between surface/interface driven and strain energy driven abnormal grain growth

Surface/interface energy and strain energy density minimization lead to an evolution towards specific crystallographic textures in thin films in which anisotropies of these energies exist. Both orientation dependent driving forces are of great importance because they strongly affect the texture of a film as well as the rate of grain growth. However, they do not necessarily have to drive the selective growth of grains towards the same final film textures, even in epitaxial systems [68]. In case of FCC materials like copper, it is thought that surface energy minimization during grain growth is responsible for the development of {111} texture, while the strain energy density selectively drives the growth of a {100} texture [14, 50-51]. Therefore, this may lead to a competition between both driving forces in defining the final texture resulting from grain growth. Given a particular film strain and thickness, these two driving forces are comparable in magnitude, and the final grain orientation in the film is that which minimizes the sum of all the orientation dependent driving forces, the surface, interface and strain energies. A transition in dominant texture due to the competition between both strain and surface/interface minimization will occur when

$$\Delta E_{\varepsilon} = \Delta E_{s,i} \tag{2.19}$$

In case of FCC materials, the largest strain energy density differences are found between the (111) and (100) oriented grains, and therefore these strain energy differences will contribute the most to the strain energy minimizing driving force for secondary grain growth, as compared to other orientations. The strain energy difference between the (111) and (100) oriented grains is then given by $\Delta E_{\varepsilon,\,(111)-(100)} \cong 146.4\ \varepsilon^2$ GJ/m³ (see figure 2.7). Moreover, the difference between the surface/interface energy densities of (100) and (111) grains on the other hand can be estimated about 20kJ/m³ for 1µm thick Cu films [50-51]. In this way, the {111} surface and interface energy minimizing texture will dominate when $\Delta E_{s,i} > \Delta E_{\varepsilon}$, i.e. for films with low thickness, strain ε and temperature excursions. On the other hand, the {100} strain energy minimizing texture dominates when $\Delta E_{s,i} < \Delta E_{\varepsilon}$, i.e. in thicker films with higher elastically accommodated strains and larger temperature excursions. The transition

between these two conditions can be graphically represented in texture maps such as the ones schematically shown in figure 2.8. It can be seen from this figure that differences in strain energy density can drive grain growth and textural evolution in some cases, and oppose grain growth in other cases. When strain energy density minimization dominates over surface and interface energy minimization, grain growth can be a strain relief mechanism.

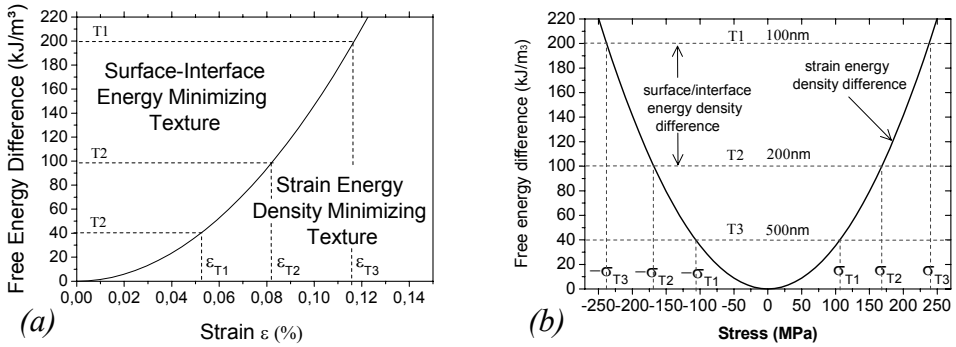

Figure 2.8: free energy difference as a function of strain and stress, revealing the competition between surface/interface and strain energy density minimization. Threshold strains ε_T and stresses σ_T are indicated for films with different thickness and can be obtained from the intersection of the horizontal lines with the parabolic curve.

The use of these texture maps to explain the textural evolution of the studied copper films in this work is justified, because the two main observed orientations during textural evolution were (111) and (100). Dependent on the film thickness h, a threshold strain ε_T can be calculated from equation 2.19, using $\Delta E_{\varepsilon,(111)-(100)} \cong 146.4\ \varepsilon^2$ GJ/m³ and $\Delta E_{s,i} \cong$ 20kJ/m³. This then results in 146.4 x $10^6\ \varepsilon^2 = 20/h$, such that the (100) orientation always has the minimum anisotropic energy. This threshold strain value can be converted into a threshold biaxial stress σ_T, using the measured elastic modulus for the films in this study. The elastic modulus for copper films was extracted from different thermal cycling experiments. Notice that in order to extract the elastic modulus from the thermal cycling experiments, the thermal expansion coefficients of copper, the barrier layer and the silicon substrate are required. For simplicity, the influence of

the barrier layer will not be taken into account. This is mainly due to a lack of information on the thermal expansion coefficients of the barrier layers used in this work, and due to the very thin barrier layer thicknesses as compared to the silicon substrate and the copper films. The magnitude of the threshold stress value is independent of whether the films are under compressive or tensile stress. Therefore, {100} texture is preferred for film stress conditions in which $|\sigma| > |\sigma_T|$, whereas {111} texture is preferred for conditions in which $|\sigma| < |\sigma_T|$ (see figure 2.8b). In order to determine the position of the as-deposited studied copper films on these texture maps, either the initial stress or strain state of these films has to be determined (see figures 2.8a-b). Because in practice the wafer curvature technique allows the determination of film stress values in a non-destructive way and without needing additional information about the mechanical properties of the deposited films (see section 3.2.4), it is more obvious to determine film stress values instead of film strain values. Be aware that by converting the threshold strain into threshold stress values one actually assumes that the elastic modulus is constant during grain growth. This however is only an ideal situation. In reality, the magnitude of the strain energy density, and thus the difference in strain energy density between (111) and (100) oriented grains may change depending on the stress that has developed in the film during grain growth, or by the mismatch of thermal expansion between the film and substrate during thermal annealing. Therefore, the graph on figure 2.8b only shows the ideal situation before actual grain growth and stress relaxation happens and the threshold stress values reveal only an indicative barrier between the two dominating driving forces.

2.3.6 The effects of yielding

In the previous sections, we only restricted to the elastic regime to explain the textural evolution in thin films. Based on these assumptions and theoretical descriptions, the textural changes in the sputtered and electroplated copper films studied in this work could be explained. However, it should be noted that when the thermal strains exceed the elastic limits of the films, yielding may occur. For completeness, we will therefore also briefly discuss the effects of yielding on textural evolution in thin films. Yielding comprises several deformation mechanisms that

may occur in thin films when these films are in the plastic regime, i.e. when the thermal strains due to differences in thermal expansion are not elastically accommodated. These deformation mechanisms include a constrained movement of dislocations, grain boundary diffusion, different strengthening mechanism including strain hardening or a combination of the preceding mechanisms. The investigation and understanding of all these complex inelastic mechanisms is not straightforward and is beyond the scope of this work. For more details about the different deformation mechanisms that may occur in polycrystalline thin films, we refer to [38-40]. The yielding stress can be defined as the stress at which a material begins to plastically deform and dislocations begin first to move. The yielding stress for grains in a polycrystalline film is thought to be dependent on both the grain size d_i and the film thickness h, such that [43, 69]

$$\sigma_Y \approx \frac{C_1}{h} - \frac{C_2}{d_i} \tag{2.20}$$

where both C_1 and C_2 are orientation dependent constants [43, 69]. Once this yield stress is passed some fraction of the deformation will be permanent and non-reversible. It is often very difficult to precisely define yield due to the wide variety of stress-strain behaviours exhibited by real materials. Due to the lack of a clear border between the elastic and plastic regions in many materials, the yield stress is often defined as the stress at some arbitrary plastic strain (typically 0.2%). As polycrystalline thin film have unusually high yield stresses (up to 2GPa), very high strain energy densities can be reached. In the discussion so far, it has been assumed that yield stresses of two adjacent grains are sufficiently high enough that thermal strains are elastically accommodated and are equal for both grains. However, when the thermal strains are not elastically accommodated, the stress in the two grains may be different, so that

$$\Delta E_{\varepsilon}^{1,2} = \frac{\sigma_1^{\,2}}{M_1} - \frac{\sigma_2^{\,2}}{M_2} \tag{2.21}$$

At sufficiently high strains, some of the grains will then yield. If grain 2 yields and grain 1 does not, σ_1 will be given by $\sigma_1 = M_1\varepsilon$, and σ_2 would be to a first approximation the yield stress of grain 2. The yield stress also depends on the orientation [43, 69-70]. Simple models for the flow stress (i.e. the stress required to cause plastic deformation in solid metals) of a

grain in a polycrystalline thin film suggest that for equal-sized grains with a {111}, {100} and {110} texture, the (110) grains have the lowest yield stress, and (111) grains have the highest [43, 69-70]. Therefore, if partial yielding occurs, so that (110) grains will yield before (100) and (111) grains, the (110) grains may have an energetic advantage for further growth, instead of other orientations. Yielding therefore favours the growth of low yield stress grains. When differences in strain energy densities dominate in driving grain growth, grain growth can provide a mechanism for stress relief and can promote plastic yielding.

2.3.7 Self-annealing in electroplated and sputtered copper films

In advanced silicon chip manufacturing, the electroplating technique has become the preferred deposition method for copper interconnect metallization. Aside from the economical benefits, this technique is capable of delivering a void-free and seam-free filling in recessed features with a high aspect ratio [71-72], due to its unique characteristic of bottom-up filling through the use of proprietary additives in the plating bath [73]. Apart from $CuSO_4$ and H_2SO_4 such chemistries typically contain Cl and a minimum of two proprietary additives, known as suppressors and accelerators [73-80]. The use of these additives in the electroplating chemistry can have a great influence on the properties of the deposited copper. For instance, the brightener additives tend to enhance the nucleation of new grains during the deposition, which will eventually lead to a reduction of the as-deposited grain size, a lower surface roughness, and consequently more reflective layers [81]. Unfortunately, the reduction in grain size also renders the deposit subcritical (~tens of nanometers for copper), leading to an inhomogeneous grain growth process which proceeds over a period of weeks, days or even hours and is characterized by selective growth of a few large grains at the expense of other normal grains. This process will then result in a bimodal grain size distribution until completion of the transformation, and is also referred as secondary grain growth (see also section 2.3.2). This remarkable room temperature grain growth, also called self-annealing was first reported by Cook and Richards in 1944, who observed the effect in Cu strips after a cold-roll treatment [82]. They indicated that a reduction of the grain size is essential for inducing this effect, which is in fact also the result of the accelerator

additives in the plating bath. The subject reemerged in a study of thin gold films when Wong, Smith, and Thompson found that a transformation of gold films with a thickness of 5-100nm occurs at only 22% of golds melting point [83]. Several mechanisms that could drive such a transformation have been proposed, including defect, grain-boundary, and surface energies, but also chemical gradients in the material that can cause diffusion-induced grain-boundary migration [84]. During the last decade, microstructural evolution or self-annealing has been observed in electroplated copper films that are stored at room temperature [44, 85-89]. Although this behaviour of electroplated copper is intriguing, the kinetics are hard to study, since the as-deposited grain structure and impurity content of the film strongly depend on the electroplating bath chemistry. Several research groups have reported that the resistivity of as-deposited electroplated copper exceeds the bulk value of 1.67μΩcm by 10-30%, but after a transient period of hours at room temperature, the resistivity decreases to near-bulk values [90-95]. The observed sheet resistance decline during self-annealing is attributed to the elimination of electron scattering at the grain boundaries due to the reducing number of grain boundaries as grain growth proceeds. The observed delay time before the decrease, as well as the actual time in which it occurs depends critically on variables such as seed layer texture, layer thickness, substrate topography, and thus the properties of the plating bath like the plating current and the brightener concentration [44, 89, 96]. The general driving force for secondary grain growth in electroplated copper is the reduction of the total energy. This occurs primarily via grain boundary motion, which reduces the grain boundary area and hence increases the average grain size [44, 97]. Suggested driving forces for the grain growth include the stress, which is accumulated during the plating process, dislocation loops, and interface and grain boundary [95]. The activation energy of secondary grain growth in electroplated copper films has been found to be in the range of 0.8-1.1eV [52, 90, 98-99], which is quite close to grain boundary diffusion energy (~0.9eV) and seems to be independent of thickness [100]. This suggest an average atomic diffusion behaviour that is similar to grain boundary self-diffusion. Contrary to popular belief, the self-annealing phenomenon for Cu is not a unique consequence of the electroplating process. Although there is early work by Patten et al. [101] describing microstructural evolution during the storage of sputtered deposited Cu films, room-temperature, self-annealing has not been widely observed in physical vapour deposited copper [102]. Recently, Rossnagel et al. [103]

and Bernat et al. [104] showed that the resistivity in sputtered deposited copper films (with thickness below 100nm) descreases during storage after deposition. Detavernier et al. observed self-annealing in sputtered deposited films up to 1500nm in thickness, and showed that the phenomenon is very dependent on the deposition parameters like the substrate temperature and sputter gas pressure and hence, on the microstructure of the as-deposited film [105-106]. In discussing the results, they used zone models to characterize the microstructure [107-108]. It was found that by raising the deposition temperature and/or reducing the sputter gas pressure (more energetic ion bombardment), a decrease in the rate of the grain growth could be observed. This could only be explained by taking into account the defect density within the as-deposited films. The defects which were considered, were vacancies and dislocations.

2.4 Summary

Nowadays, polycrystalline thin films are used in a wide variety of applications. For the development and design of reliable films and interconnects, a firm understanding of the different factors that control the microstructural evolution in these films is essential. Grain growth and texture formation is usually abnormal, leading to an increased average grain size and an evolution in the shape of the grain size and grain orientation distributions. This abnormal growth mode, can occur at both room temperature and elevated temperatures. In the former case, this growth mode is also called self-annealing and is extensively observed in electroplated and sputtered copper films. Abnormal grain growth can be driven by minimization of surface, interface or strain energies, depending on film, substrate and film/substrate interface properties (i.e. initial film and substrate textures, film stress due to strained regions within the film or at the film/substrate interface or film stress due to differential thermal expansion). These factors can lead to films with different final textures, depending on which energy dominates. In case of FCC materials like copper, surface energy minimization is responsible for the development of {111} texture, while strain energy density is responsible for the growth of (100) oriented grains.

2.5 References of the chapter

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Chapter 3

Experimental methods

3.1 Metallization

In most advanced silicon chips, a multilevel on-chip interconnect scheme has to be used in order to produce a physical routing network which connects a massive number of transistors. Such a multilevel interconnect scheme sets a stringent requirement on the global planarization after processing each of its levels. A metallization scheme commonly seen today consists of an ionised physical vapour deposition (I-PVD) copper diffusion barrier layer (e.g. TaN, Ta, TaN/Ta, ...), followed by an I-PVD copper seed layer and the electrodeposition of copper in recessed features. The need for a diffusion barrier layer is mainly due to reliability considerations, while copper seed is required to initiate the subsequent electroplating process. Both steps are required to deliver an adequate and smooth sidewall and bottom coverage in recessed features. For copper electrodeposition, the most important objective is to deliver a void-free filling in trenches and vias.

3.1.1 Damascene patterning process

Conventional aluminium interconnects are defined by a subtractive metal etch of a planar PVD deposited aluminium film (figure 3.1): a lithographic process is used to pattern the protective photoresist. The patterned aluminium film is then anisotropically dry-etched by a reactive ion etching (RIE) process and once the metal etch is completed the resist is stripped. Subsequently, a SiO_2 intermetal dielectric layer is deposited over the patterned aluminium layer by chemical vapour deposition (CVD). The intermetal dielectric layer depositon is followed by a chemical-mechanical-polishing (CMP) process to create a globally planar surface. However, using a RIE process to define features in copper is not trivial

because copper is very difficult to dry-etch due to the low vapour pressures of copper chlorides and fluorides [1].

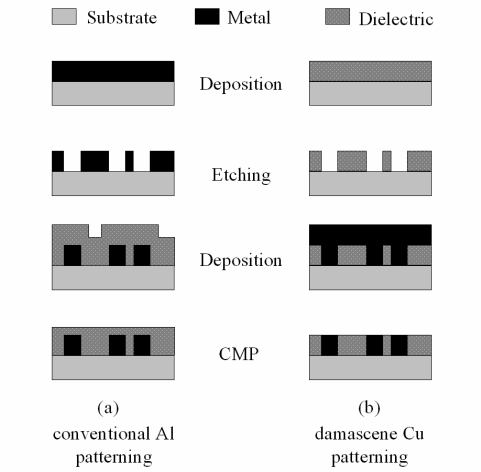


Figure 3.1: comparison of the conventional Al patterning and Cu single damascene patterning process.

Therefore, the use of copper for metallization requires the implementation of a new patterning process, also called damascene patterning, which is named after the resembling practice of creating metal inlays as developed by the artisians of Damascus in the Middle Ages [2-4]. This term was reused by IBM in microelectronics technology in 1990 and refers to the process of etching recessed features in a dielectric layer, followed by the blanket deposition of a diffusion barrier and the interconnect metal into the features. Finally, the metal outside the recesses is removed by chemical mechanical polishing (CMP), as illustrated in figure 3.1. The introduction of dual damascene processing (where a via hole and a trench in the same layer can be patterned and metallized together) greatly reduces the number of process steps in chip fabrication. Moreover, damascene processing avoids the problems associated with etching copper and intermetal dielectric layer gap-fill deposition. But, another challenge arises from the need to fill, in a defect free way, the damascene features with copper.

3.1.2 I-PVD deposition technique

Deposition of thin films by physical vapour deposition (PVD) techniques has found widespread use in many industrial sectors. The field of applications includes integrated circuit (IC) manufacturing applications such as the formation of diffusion barriers and seed layers on the side and bottom of high aspect ratio vias and trenches. Due to the fast development of the microelectronics industry, in which the circuit dimensions shrink steadily and the aspect ratio (i.e. heigth/width ratio of the recesses) increases, successful coverage becomes increasingly more challenging. The increased requirements on coating materials and deposition techniques as well as the opening of new application fields drives the development of enhanced deposition techniques. The latter allow a direct control of the sputtered flux and a further decrease in the deposition temperature, by enhancing the adatom mobility through the momentum transfer to the film and an increased chemical reactivity. Compared to chemical vapour deposition (CVD), PVD has several advantages including high purity deposits and a relatively easier hardware setup. However, one major limitation associated to conventional sputtering deposition is the line-of-sight travel of incident particles. In general, sputtering techniques are low temperature processes based on establishing a glow discharge in an inert gas (often Ar). Here, positively charged ions are created and subsequently accelerated towards the target material, which acts as cathode (cathodic sputtering). By complex mechanisms linked to the momentum transfer from impinging ions to the target particles (ions and neutral atoms), the latter are sputtered towards a substrate to form a continuous film. Chamber pressure, substrate bias and temperature, are among the most important parameters determining film characteristics. Glow discharge methods like magnetron sputtering have the advantage that the ions of the discharge are abundantly available to the deposition process. However, the ions available are mainly the ions of the inert sputtering gas and ions of the sputtered material are rare. Over the past few years various ionised sputtering techniques have appeared that can achieve a high degree of ionization of the sputtered atoms. In copper interconnect fabrication, a lot of effort has been put in the development of upgrades of the conventional sputtering systems in order to improve step coverage of physical vapour depositions. In particular, the most common used PVD technique nowadays to deposit diffusion barriers and copper

seed layers, is the ionised physical vapour deposition technique (I-PVD) [5]. This technique is defined as a deposition process where the flux of depositing species is composed of more ions than neutral atoms. The big advantage of this technique is that both the directionality of the flux of sputtered ions and the energy of the depositing species can be controlled by applying a negative bias to the substrate [6]. In practice, a metal vapour is created with the sputtering process and then ionized when the flux passes the high density argon plasma. The motion of neutral atoms is difficult to control but ions can be collimated by an electrical field. When a substrate surface is immersed in a plasma, a thin positively charged region is formed near this surface. The ions that enter this region are accelerated towards the substrate and collimated due to the electric field across this positively charged region. Furthermore, by applying a certain bias voltage to the substrate, the ion bombardment energy can be controlled. Because of the collimation, the ions may reach the bottom of deep narrow trenches or vias to further enhance the coverage of recess bottom, while the neutral atoms are non-directional and difficult to control, which will eventually lead to a non-uniform PVD layer thickness onto sidewalls, bottom of trenches/recesses and the field regions, since their deposition profile is determined by line-of-sight deposition. In order to further maximize the directionality of the flux of ions, the ionisation of the sputtered material itself has to be enhanced, which is the goal of most magnetron sputtering systems today. A first generation I-PVD technique based on these principles is the Ionised Metal Plasma (IMP^{TM}) technique of Applied Materials [7]. Here, the directionality is achieved by a bias which accelerates the ions. The ions are created by an RF coil, which is immersed into the chamber and is made of copper (ICP chamber). Further improvements in directionality can come from an increased spacing between the target and the substrate (geometrical shaping) and an unbalanced magnet design, leading to a sort of self-collimation. The latter concepts have been implemented in a second generation I-PVD technique and this will contribute to a much better coverage in high aspect ratio structures, and virtually without overhang. An example of this technique is the Self-Ionized Plasma (SIP^{TM}) process of Applied Materials [8-9]. A typical chamber design of the SIP^{TM} technique is shown in figure 3.2. For this technique, the plasma is initiated before the actual sputtering process by Argon gas, and is from that moment on further maintained by the copper ions itself during the entire sputtering process.

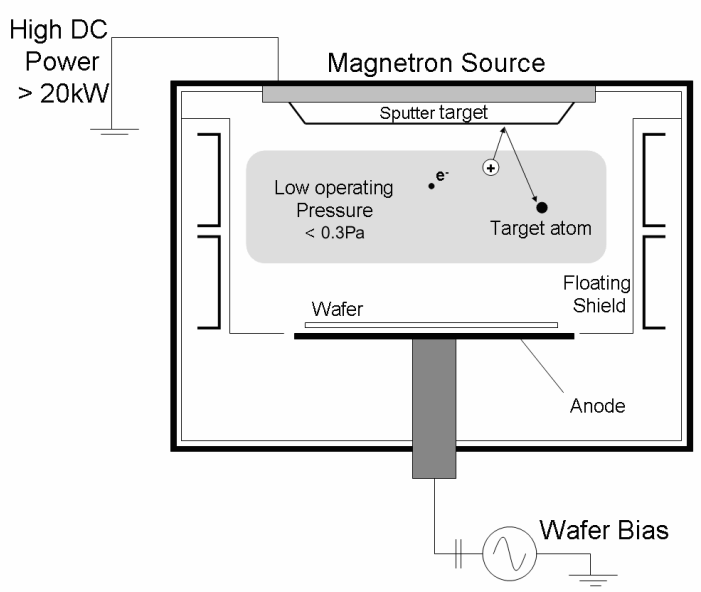


Figure 3.2: diagram of a typical SIP sputtering system, illustrating the sputtering principle. A plasma is excited between two electrodes. Positively charged ions are accelerated towards the cathode (target). Individual atoms can be knocked out when the ions bombard the target. By applying a certain bias condition, the ions can be guided to the wafer

This is in contrast to previous generations of the I-PVD technique, where both initiation and maintenance of the plasma was done using Argon. The advantage of this self maintaining copper plasma is the negligible amount of Argon that is built into the metal deposits. The use of the SIP technology takes advantage of the magnetron source design, which provides an efficient transfer of energy from the secondary electrons to plasma waves in order to increase ionization of the sputtered metal atoms. Moreover, this technique allows low deposition pressures (< 0.3 Pa for SIP, as compared to about 3 Pa for IMP), which increases the mean free path of the ions. This results in less off-normal flux due to scattering. A conformal (i.e. smooth and continuous), overhang-free coverage of copper seed in damascene structures, which can be provided with the SIP process, is a critical requirement for a successful electrodeposition. As all these concepts are aimed to increase directionality and thus achieve better

coverage on the bottom of the recesses, this doesn't neccesarely guarantee a good coverage at the recesses sidewalls. When the recesses become deeper (i.e. the aspect ratio increases), the coverage in the trench will go thinner especially at the lower part of the sidewall. A way to improve the coverage in the trench, is by increasing the kinetic energy of the sputtered ions (by increasing the substrate bias). In this way, an effect of sputter-etching from the horizontal surfaces (i.e. back sputtering) is obtained: materials already deposited on the bottom are re-distributed onto the sidewall of the recess, thereby giving rise to thinner bottom and thicker sidewall coverage. Moreover, the highly energetic ions will also exert a 'beveling' action on the top corners of the recesses, thereby reducing the overhang on the top corners (see figure 3.3). In this work, the SIP^{TM} technique will be used for the deposition of both the barrier layers and copper sputtered seed layers. Typical deposition rates for standard seed layer thickness and bias conditions is 10nm/second.

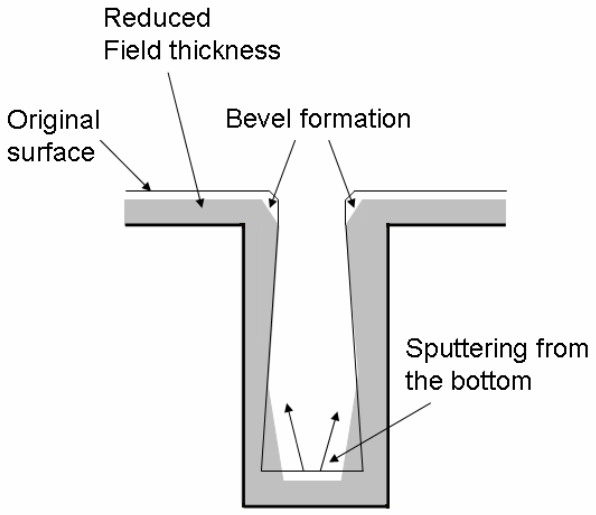


Figure 3.3: Principles for an improved coverage by I-PVD: the increased ionization of the sputtered material in combination with a negatively bias of the substrate helps the coverage of the recesses bottom. Increasing the sputtered ion energies leads to material resputtering from the bottom, therefore improving the sidewall coverage.

3.1.3 Electrodeposition of copper in trenches

Damascene processing avoids the problems with etching Cu and inter-layer-dielectric gap-fill deposition. But, another challenge arises from the need to fill the damascene features with Cu in a defect-free way. Possible ways for the filling profile of deposited Cu to evolve in time are shown schematically in figure 3.4 [10]. In conformal filling, a layer of equal thickness is deposited at all points of the feature. In the ideal case, for straight-walled features, this could result in perfect filling of the cavity. However, small variations in deposition rate and/or an initial slightly re-entrant shape of the profile will result in the creation of a seam or void. Subconformal filling refers to the case of an enhanced deposition rate at the external corners of the cavity. This results in the formation of a void even in straight-walled features. Superconformal deposition occurs in the case of an increased deposition rate along the sides and the bottom of the feature compared to the outside of the cavity.

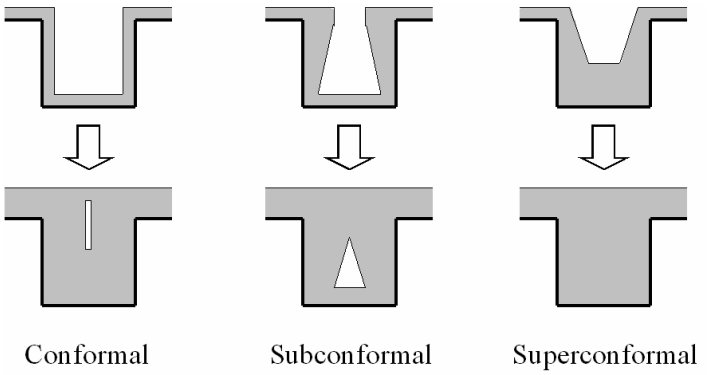


Figure 3.4 : evolution of profile shape during deposition

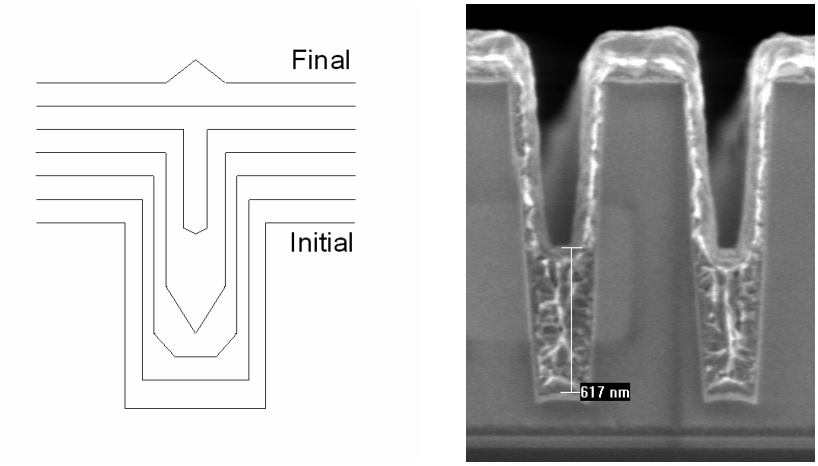
It has been found that electroplating of copper from certain plating solutions that contain special additives, can lead to a superconformal deposition behaviour that eventually produces void-free and seamless structures. This process is also referred in literature as superfilling or bottom-up filling [10]. This term describes a phenomenon in which the

electrodeposition rate at the trench bottom is much faster than on the sidewalls inside a trench, and than that on the field area outside the trench. Due to this superb gap-filling capability and low cost, electrodeposition has emerged as the depostion process of choice for damascene copper interconnect metallization.

Basically, copper electrodeposition is performed by immersed wafers in an aqueous electrolyte. The wafer surface is then electrically connected to the negative terminal of an external power supply as a cathode, while solid copper serves as an anode. Current passes through the wafer surface causing reduction of cupric (Cu^{2+}), with electrons from the external circuit to form copper deposition ($Cu^{2+} + 2e \rightarrow Cu$). In the meantime, an oxidation reaction occurs at the anode, which balances the current flow at the cathode, i.e. Cu^{2+} removed from the solution at the cathode is replaced by dissolution from the copper anode ($Cu - 2e \rightarrow Cu^{2+}$).

Commercially available plating baths for IC interconnect deposition contain a combination of several proprietary additives in proper proportions to achive superfilling, which is particularly usefull in metallization of deep recesses. Apart from $CuSO_4$ and H_2SO_4 such chemistries typically contain Cl and mainly three types of organic additives (accelerators, suppressors and levellers) designed to improve the filling of deep trenches. Polyethers such as polyethylene glycol (PEG) and polypropylene glycol (PPG) are used as a suppressor additive. As indicated by its name, suppressor additives inhibits the deposition of copper. A sulphur based organic molecule such as dithiosulfonacid acts as an accelerator agent and can locally intensify the plating current where they adsorb. This then also leads to a reduction of the as-deposited grain size, lower surface roughness, and consequently more reflective layers. Accelerators play a key role in realizing a bottom-up filling of copper in recessed features. Finally, levellers are a second class of current-suppressing molecules, which are usually added to the plating bath at low temperatures. Benzotriazole (BTA), an aromatic nitrogen based molecule or polymer, usually acts as a levelling agent. According to the type of organic additives added, a plating bath is named as the two-component or three-component plating system [10-11]. Successful filling can be achieved by optimising the concentration of the various additives. However, the exact mechanisms by which the multiple additives interact and influence plating at the wafer surface to achieve superfilling in small features are still not fully understood. The schematic diagram on figure 3.5

illustrates the evolution of electrodeposition in small features. For more details, we refer to [11-17]. After electrodeposition, wafers are usually annealed in situ to stabilize the microstructures of deposited copper. Finally, chemical-mechanical polishing (CMP) is used to remove the excess of copper on the field, leaving copper lines embedded in dielectric.



(a) *(b)*

Figure 3.5: (a) schematic drawing of the deposition profile. First, an increased accelerator concentration is formed in the bottom corners of the trench, leading to accelerated local copper plating. Then a rapid bottom-up filling leads to a void-less filling. Finally a hillock is formed as a result of continued accelerated plating; (b) cross sectional Focused Ion Beam (FIB) image perpendicular to a copper wire, illustrating the superfilling process in narrow features.

3.2 Main analysis techniques

In this work, sputtered copper thin films of different thickness and copper sputter bias conditions are characterised to investigate stress, resistance and textural evolution involved in the transition of the microstructure during self-annealing at room temperature and elevated temperatures. This is done in order to gain a clear insight into the origin, mechanism, and correlation of film and stress evolution in sputtered copper thin films of different thickness and copper sputter bias conditions. For the microstructural characterization, we restrict to Scanning Electron Microscopy (SEM) and Electron Backscatter Diffraction (EBSD) as the main analysis methods, since these techniques yield a high lateral resolution without specimen preparation requirements. For the mechanical characterization of the studied films, stress measurements were carried out using the wafer curvature technique, while the electrical characterization was done using a four point probe.

3.2.1 Microstructural characterisation: SEM

A scanning electron microscope (SEM) is a versatile instrument which is used in many fields. In comparison to an optical microscope a SEM has a greater resolution and greater depth of field allowing investigation of non-flat samples at higher magnifications. In addition, compositional and orientation data can also be obtained. Basically, in a scanning electron microscope a small beam of electrons (in the order of ~10nm) scans the surface of a sample, while the subsequent interactions of the electrons with this sample are further analysed by several detectors. This information is then used to form an image of the sample surface. The source of electrons is usually a tungsten filament or a field emission gun. The electrons emitted are focused by a series of electromagnetic lenses and accelerated to an energy which is in the range of 1-30 keV. Subsequently, the beam is deflected by scan coils to direct it to a specific position on the sample. The interaction of the high energy electrons with a sample is quite diverse, as can be seen on figure 3.6. This can be explained by the fact that in a sample the primary electrons experience both elastic and inelastic scattering. Inelastic scattering of electrons refers to various processes, which have the common feature that a primary electron loses a detectable amount of energy. Through subsequent scattering, an electron can finally

be captured by the solid, thus limiting the range of travel of the electron within the solid. Most of the kinetic energy of the primary electron will be transferred into heat, whereas some of the energy can leave the sample as X-rays, light, secondary electrons and backscattered electrons. The secondary electrons usually have an energy loss less than 50eV. Secondary electrons, which result from inelastic scatterings of the electron beam with valence electrons of the target atoms, are generated from different regions underneath the sample surface, but only those electrons very close to the surface (typically several nm) can actually leave the sample again due to their limited energy and thus give a topographical contrast.

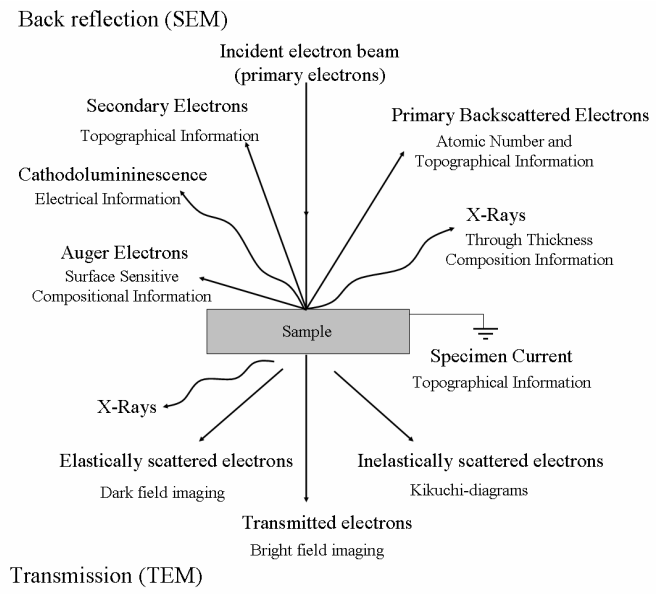


Figure 3.6: different emitted signals from the interaction of high energy electrons with matter in an electron microscope

When elastic scattering occurs, a primary electron interacts with the nucleus and all the electrons of an atom where the electrostatic charges play a major role (i.e. Rutherford scattering). An elastically scattered electron might proceed in a direction different to the primary electron, however its energy is the same (in the order of several keV).

Backscattered electrons, are electrons which result from the elastic collisions of the electron beam with the nuclei of the target atoms, which are partially screened by the bound electrons. Subsequently, these collisions cause the beam electrons to deviate from their original direction of travel, causing them to "diffuse" through the solid. The backscatter electron yield is a function of the elemental atomic number of the scattering atom (Z-contrast), while the angular distribution of the backscatter electrons is a function of the angle between the impinging electron beam and the surface. Hence, the analysis of backscattered electrons can yield a compositional contrast if a sample consists of atoms with a sufficient difference in the atomic number. Notice that the angular distribution is assymetrical due to the specimen tilt, as illustrated in figure 3.7a.

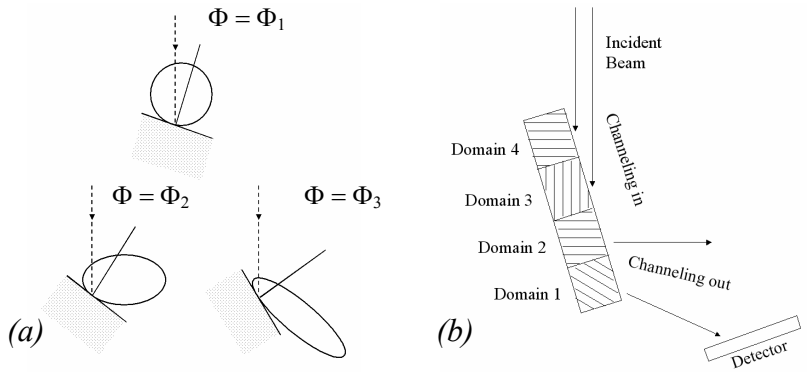
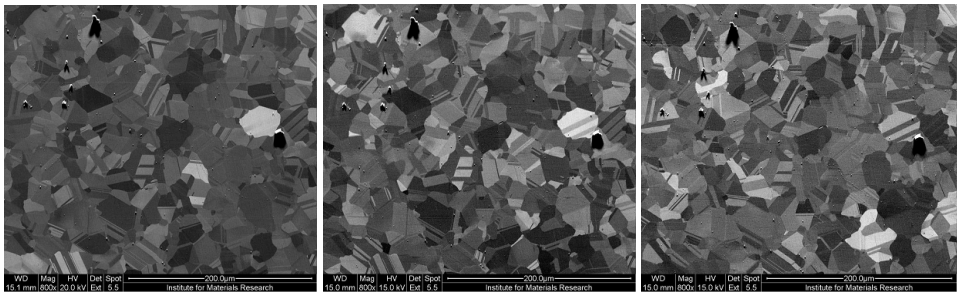


Figure 3.7: (a) angular distribution of the backscattered electrons for 3 specimen tilts Φ_1, Φ_2 and Φ_3, with $\Phi_1 < \Phi_2 < \Phi_3$. (b) schematic simplyfied diagram to show how both channeling-in and channeling-out can give rise to orientation contrast (OC) images.

As the tilt angle of a specimen is increased, the interaction volume becomes smaller, due to the tendency of the electrons to undergo forward scattering in any individual scattering event. Due to this assymmetrical distribution, the backscattered electrons also have a strong dependence on the surface topography. Besides the Z contrast and topographical contrast, backscattered electrons are also mainly responsible for diffraction patterns. As diffraction depends on the crystallography of a sample, the

analysis of electron backscatter patterns can yield a crystallographic contrast. This effect is also known as orientation contrast (OC) or channeling contrast, i.e. a contrast which is due to different crystallographic orientation. The extent to which electrons can penetrate into (or exit) a material is a very strong function of both the wavelength of the electrons (which is related to the applied accelerating voltage) and the angle of incidence. This effect is also referred in literature as channelling-in and channelling-out. Both channelling effects contribute to the formation of OC images (see figure 3.7b), although the relative contribution from the two effects remains unclear. Figures 3.8 show some examples of OC images of the same region on a polished diamond sample, but taken with different accelerating voltages (figures 3.8a-b) and different specimen tilt conditions (figure 3.8b-c). Because a diamond sample was used, Z-contrast doesn't contribute to the image formation. Moreover, because the sample was polished, also the influence of topography on the image formation could be excluded. Therefore, only pure orientation contrast is observed on figures 3.8a-c.



(a) 20kV, 70° (b) 15kV, 70° (c) 15kV, 68°

Figure 3.8: three OC images of a certain region on a diamond sample, taken with different accelerating voltages and specimen tilt angles.

These images show that the intensity of the forward backscattered electrons changes with both the accelerating voltage and tilt angle, therefore indicating that the obtained orientational contrast is non-quantitative, as the intensity of the forward backscattered electrons can not be related to the orientation. A more quantitative crystallographic information can be obtained with other characterization techniques like transmission electron microscopy (TEM), X-ray diffraction (XRD) and

electron backscatter diffraction (EBSD). In this work, we will mainly use the EBSD technique due to its high lateral resolution and no specimen preparation requirements, compared to other techniques like TEM and XRD.

3.2.2 Microstructural characterisation: EBSD

The ability to obtain microstructure-level orientation information or microtexture requires that the probe size available from the exploring radiation must be smaller than the size of the microstructural units themselves. Electrons are therefore ideal for such combined microstructural/crystallographic studies. Depending on the desired resolution, the diameter of the electron beam can be changed. Typical diameters for electron beams are in the order of ~10nm.
Until the 1980s, transmission electron microscopy (TEM), was one of the major techniques used for such work, with some input from Laue X-ray diffraction and orientation contrast in the scanning electron microscope (SEM). The main advantage of the TEM technique is its high lateral resolution and the ability to study microtextures using Kikuchi bands. One of the biggest disadvantages however is the rather tedious and difficult sample preparation. X-ray diffraction can also provide quantitative texture information. However, due tot the very limited lateral resolution of this technique, this information is merely global. And as mentioned in the previous section, orientation contrast in the SEM gives only non-quantitative texture information.
Since the 1980s, an enhanced SEM-based technique for microtexture has been developed and is known as electron backcatter diffraction (EBSD). This technique combines the benefits of both TEM and XRD. One of the advantages of this technique is the capability to perform automatic diffraction analysis of Kikuchi patterns and in this way obtain crystallographic data and imaging with a spatial resolution of less than 0.05μm. Moreover this technique can also be combined with the regular capabilities of a SEM such as simultaneous chemical analysis. The new generation of field emission gun SEMs (FEG-SEM) offer much better resolution ($\geq$ 10nm) that now challenges that available by TEM ($\approx$ Å). However, since EBSD only occurs in a region very close to the surface (10-50nm), it is a surface sensitive technique and does not give volume

information. By analysing the directional distribution of backscattered electrons, information on the crystallographic structure of a sample can be gained. The analysis is based on the interpretation of Kikuchi patterns. On figure 3.9, a schematic overview of the origin of these Kikuchi lines is illustrated. When the primary electron beam touches the sample, the interaction mainly behaves like a point source that scatters electrons incoherently (with little loss of energy but loss of phase coherence) in all directions. These electrons then interfere by diffraction at a lattice plane (hkl) under a certain Bragg angle θ, which then produces Kossel cones located at either sides of the (hkl) planes (figure 3.9). As the wavelength of electrons is very short (e.g. 0.009nm for electrons with 20keV) the Bragg angles at which diffraction occurs are very small, i.e. smaller than 2°. Therefore, the apex angle of the cones (180°-θ) are very close to 180°, so its gnomonic projection on a plane phosphor screen will be very close to a straight line. Every lattice plane which fulfils the Bragg condition will produce a pair of lines (Kikuchi band) and hence a complex pattern is formed on a screen which is suitably positioned. Notice that the spacing between these pairs of lines is an angular distance 2θ, which is in turn proportional to the interplanar spacing (figure 3.9a).

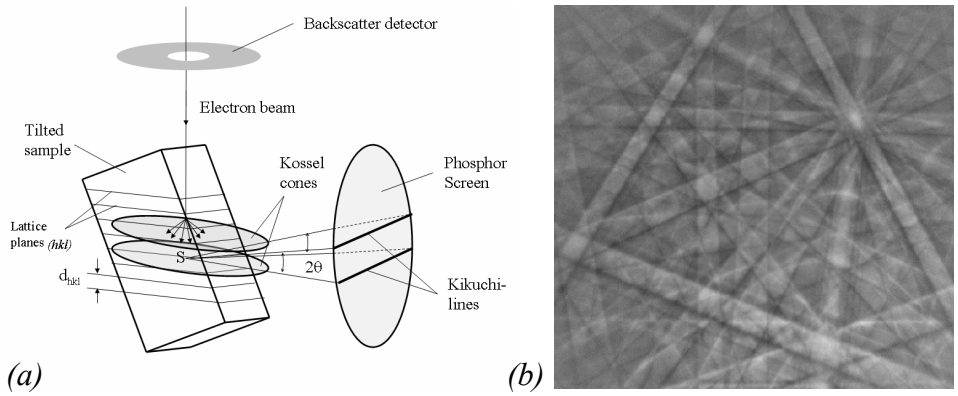


Figure 3.9: (a) schematic overview of the origin of Kikuchi lines form the EBSD (i.e., tilted specimen) perspective and (b) a typical Kikuchi pattern

The arrangement of these bands is dependent on the orientation of the crystal with respect to the incident electron beam and the crystal structure itself. Therefore, a Kikuchi pattern essentially embodies all the angular

relationships in a crystal, and hence contains the crystal symmetry, with exception of some deformations due to the gnomonic projection. An example of a Kikuchi pattern recorded in a SEM is shown in figure 3.9b. The working principle of the EBSD technique relies on positioning the specimen within the SEM such that a small angle, typical 20°, is made between the incident electron beam and the specimen surface, as shown in figure 3.10. If the crystal structure and the lattice constants of the phases investigated are known, the resulting Kikuchi diffraction pattern as described above can then be captured on a phosphorous screen and indexed, i.e. the lines can be related to the corresponding lattice planes. Since begin 1990s, the arrangement of the Kikuchi bands can be obtained, indexed and stored automatically using computer algorithms. Sequential analysis of EBSD patterns obtained from sampling points on some predefined raster allows to map the crystal orientations and phases at fast rates (currently up to 100 patterns per second). This operation is called orientation mapping or automated electron backscatter diffraction.

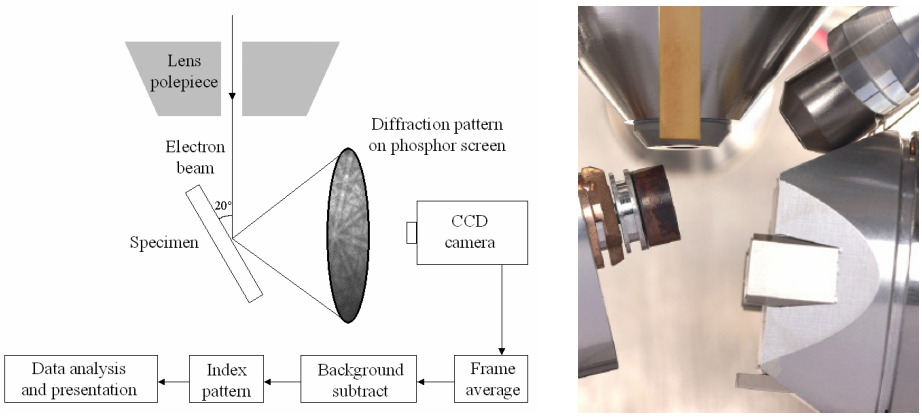
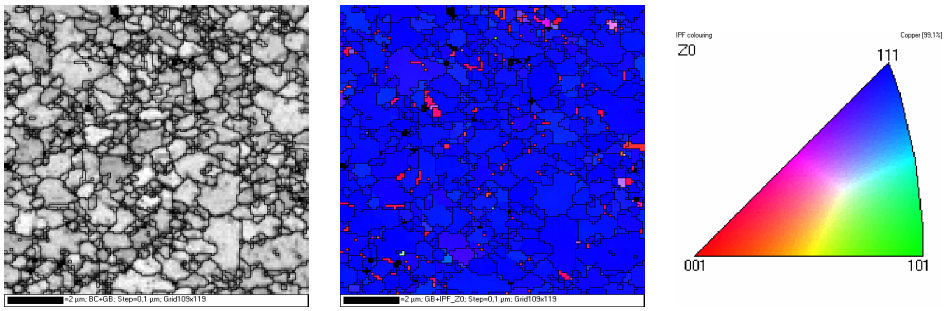


Figure 3.10: Schematic overview of a typical EBSD setup and the used sample-detector configuration

A modern EBSD system collects several parameters for every measurement point: orientation, coordinates, indexing confidence indicator, phase identity and pattern quality. The orientation of individual measurement points can be identified with an accuracy better than 1°. A graphical representation of the EBSD results, also called mapping, proves

to be very useful and intuitive: for each measured data point, the coordinates, orientation and other parameters can be determined. Depending on the specific orientation of each data point, a colour can be attributed according to a unit triangle colouring scheme. Other parameters can also be mapped in a similar way. A typical example is shown in figures 3.11. Figure 3.11a shows the variation in diffraction pattern quality across the scanning area, thereby illustrating the general microstructural characteristics. Figure 3.11b on the other hand shows the corresponding orientation map, with colours corresponding to the crystallographic orientation of each point as defined by the unit triangle colouring scheme as shown in figure 3.11c.



(a) *(b)* *(c)*

Figure 3.11: top view EBSD mappings of a Cu film. (a) Band contrast mapping, revealing the diffraction pattern quality across the scanning area. The bright regions correspond to good pattern quality areas, while darker regions correspond to a poor pattern quality. (b) IPF // Z mapping, showing the crystallographic orientation with respect to the film normal direction (Z-direction) and (c) unit triangle colouring scheme

By looking at the orientation differences between several points for example grain boundaries or orientation variations within a grain can be identified. The quality of indexing procedure is assessed by a number called confidence index, which has a value between 0 and 1 for every point. The closer this value is to 0 the more doubtful the result is. Moreover, the sharpness of the Kikuchi lines gives an indication of the distortion of the lattice which can be due to defects (e.g. dislocations) or lattice deformation. Furthermore, the representation of textures by their

proximity to one or more ideal orientations is the most commonly used method of texture description and provides a concise way to describe common and/or important textures. The display method appropriate to the ideal orientation description is the pole figure, which is a representation of chosen families of planes (usually {100}, {111} and {110} for FCC materials like Cu) on a stereographic projection whose axes are parallel to the specimen axes. The formation of a microtexture pole figure is shown schematically in figures 3.12a-d. These figures illustrate the intersection with the reference sphere of {100} poles from a single grain within a specimen and the subsequent stereographic projection of these poles onto the equatorial plane. Since the axes of the reference sphere are made to coincide with those of the specimen, figure 3.12b is the {100} pole figure of this particular grain and figure 3.12c is a microtexture pole figure of 16 grains which have an orientation close to that of the grain in figure 3.12a.

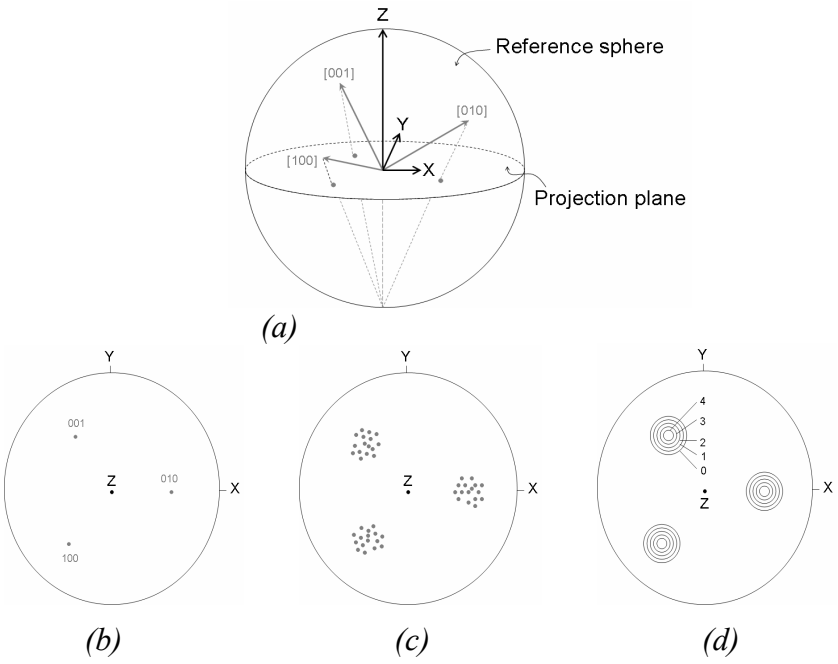


Figure 3.12: illustration of the formation of a {100} microtexture pole figure (a) intersection of {100} poles with the reference sphere having the axis of the specimen; (b) projection of poles from one grain; (c) projection of poles from 16 grains; (d) density contour equivalent of (c)

3.2.3 In-situ SEM: real-time monitoring

In order to gain a more clear insight into dynamical processes, more in particular the grain growth dynamics during self-annealing in sputtered and electroplated copper thin films at room temperature and elevated temperatures, detailed microstructural information of the same area on the sample versus time is desirable. Therefore, a Philips XL30-FEG SEM has been redesigned to enable to grain growth monitoring in "real-time" at room temperature and at elevated temperatures up to 300°C by taking backscattered electron (BSE) images of particular regions on the sample at well defined moments in time. In this way, it is possible to construct grain growth "movies" and study the dynamic behaviour during the self-annealing process. As already mentioned in a previous section, backscattered electrons are very useful to reveal orientation contrast. However, we need to keep in mind that these images only give non quantitative information about the grain orientations. An overview of the in-situ "real-time" SEM setup is shown in figure 3.13.

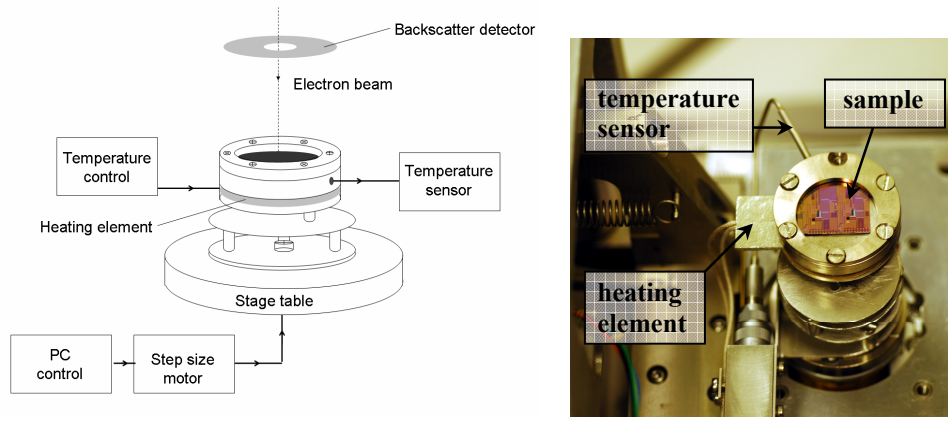


Figure 3.13: (a) overview of the in-situ "real-time" SEM setup, showing respectively the temperature and PC control, step size motor, stage table, heating element and temperature sensor.

The PC control sends the stage table to certain predetermined regions on the sample. For these regions, BSE images are subsequently taken at well defined moments in time. This setup can be used at both room temperature

and elevated temperatures. Both temperature sensor and temperature control enable to either perform a thermal cycle, i.e. heating up the sample at a constant rate (typical 3°C/min) to a predetermined temperature (typically in the range 25-200°C) and then cool down again to room temperature, or to heat up the sample to a predetermined constant temperature. For the latter case, a temperature stability up to 0.01°C can be achieved once the predetermined temperature is reached.

3.2.4 Stress measurements by wafer curvature technique

Copper and low-k materials have coefficients of thermal expansion that differ widely from those of the silicon substrate. Therefore, when the temperature changes during both processing and in service, this will result in a certain film stress. In addition, many deposition processes also result in films with a large intrinsic stress (stress in addition to that which can be accounted by differences in thermal expansion) because of defects or structural mismatch between the film and substrate. Stresses in thin films can be measured using different techniques like X-ray diffraction to measure the lattice spacing, cantilevered bending beams and other not mentioned methods. However, one of the most accurate and simplest ways to measure the in-plane stress of thin films on substrates at wafer level is using the wafer curvature technique.

The wafer curvature technique is based on the fact that the stress in a film on a substrate will lead to a curvature of the film-substrate composite. This curvature can be measured with a laser scanning apparatus: basically, a laser beam is reflected from the surface of the wafer. When the correct optical settings are used, the displacement of the reflected beam is proportional to the change in the angle between the incident laser beam and the wafer surface. For a perfectly flat wafer, the position of the reflected beam would remain constant as the mirror moves. If the wafer is curved, the position of the beam varies and the change in the displacement of the reflected beam is proportional to the change in the angle between the incident laser beam and the wafer surface. In this way, the curvature of the wafer is determined from the position of the reflected laser spot on a position-sensitive photo cell. With the given material properties and geometrical dimensions of the film-substrate system, the measured

curvature before and after deposition of a film can be measured and converted into a stress value for the deposited film, by using the Stoney equation [20-22].

$$\sigma_{film} = -\frac{E_{sub}}{6\left[1-\nu_{sub}\right]}\frac{t_{sub}^{2}}{t_{film}}\left(\frac{1}{R}-\frac{1}{R_0}\right) \qquad (3.1)$$

Where σ_{film} is the in-plane stress of the thin film, E_{sub} and ν_{sub} are the elastic modulus and Poisson's ratio for the substrate, t_{sub} and t_{film} are the substrate and film thickness, R_0 is the initial radius of curvature before film deposition, and R is the measured radius of curvature after film deposition. This relation is only valid if: (i) both the film thickness and substrate thicknesses are small compared to the lateral dimensions; (ii) the film is much thinner than the substrate; (iii) the substrate material is homogeneous, isotropic and linearly elastic and the film material is elastically isotropic. Notice that this calculation requires a change in the radius of curvature, the elastic properties of the substrate, and the thickness of the substrate and film. It is however not necessary to know the mechanical properties of the deposited film, assuming it is uniform of thickness, which indicates that independent of composition and microstructure, stress can still be obtained. The resulting measured in-plane film stress is then analysed and modelled based on any known mechanical properties. More details about this technique can be found in literature [18-20]. The main advantage of this technique is that the wafer remains intact. This is beneficial as it allows measurements of sheet resistance to be taken over the same period of time.

3.3 References of the chapter

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Chapter 4

Microstructural and textural development in sputtered copper films

4.1 Introduction

The microstructural and textural development in thin copper films depends on many parameters like the film thickness, heat treatment and specific deposition conditions. These textures can be understood as those which lower the total energy of the system during processing or afterwards. Important contributions to the driving force for grain growth in thin films are the reduction in free energy due to a reduction in grain boundary area, the anisotropy of surface and interface energies, and the anisotropy of the elastic strain energy density [1-2]. Other driving forces can be pinning due to contamination within the film (i.e. chemical gradients can cause diffusion-induced grain boundary migration) [3] and defect energy within the grains (i.e. annihilation of defects) [4-5]. Grain growth in thin films may appear as normal or abnormal growth. If the driving forces act homogeneously, normal grain growth is observed, while if they act selectively, abnormal grain growth can occur. The main reason for such selectivity is an anisotropy of surface energy, interface energy, and/or strain energy. In general, for face-centered-cubic (FCC) materials like copper, surface/interface energy minimization promotes the {111} planes parallel to the film surface [6-8]. On the other hand, the preferred texture is {100} for conditions that favour strain energy minimization. Normal grain growth often develops a lognormal grain size distribution, leading to grain sizes of two to three times the film thickness [9-10]. Abnormal grain growth on the other hand results in a bimodal grain size distribution in the course of the growth process, leading to a final average grain diameter of many times the film thickness [11-12]. The microstructural evolution in electroplated copper films during self-annealing has been reported by many researchers [13-17]. During self-annealing, both physical and

electrical properties change dramatically. As reported, the grain size increases by an order of magnitude, accompanied by a reduction in sheet resistance by about 20% [18-20], and the development of stress in either tensile direction [21-23] or compressive direction [17]. Contrary to popular belief, the self-annealing phenomenon of copper is not a unique consequence of the electroplating process. Although in some earlier studies some reference is made to microstructural evolution during the storage of sputtered copper films at room temperature [24], self-annealing is not widely observed in physical vapour deposited copper [25]. In this chapter we will focus on the microstructural evolution of sputtered copper films at room temperature and elevated temperatures, using the real-time SEM monitoring technique, and by performing both sheet resistance and stress measurements at different moments in time. The textural development will be discussed in terms of mainly two driving forces: the minimization of surface/interface energy and the minimization of strain energy.
A schematic drawing of the typical layer build-up of the studied copper films is illustrated in figure 4.1. As shown, pure copper films were produced on 200 mm Si(100) wafers with standard layers of 50nm Si_3N_4 and 500nm SiO_2.

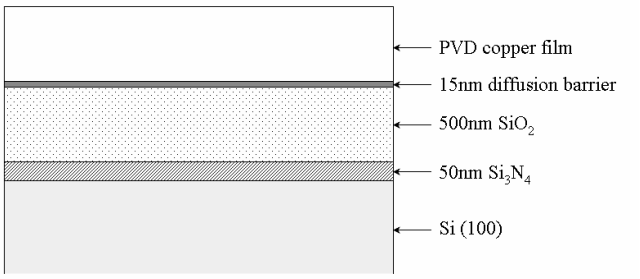


Figure 4.1: schematic illustration of the layer build-up of the investigated sputtered copper films.

The standard layers are followed by SIP (Self Ionised Plasma) deposition of a 15nm diffusion barrier and a 100-500nm thick Cu seed layer. These barrier layers are used to improve adhesion and to prevent intermixing between Cu and Si at elevated temperatures. For more details about the sample preparation, we refer to chapter 3. For most of the experiments presented in this work, we used a 10nm TaN/5nm α-Ta barrier layer. In

order to investigate the influence of both the barrier composition and structure on the microstructural evolution in these copper films, two other barrier layers (i.e. 15nm amorphous TaN and 15nm β-Ta as determined by XRD) were taken. The electrical and stress measurements on thin films are made with a KLA-Tencor RS75 four point probe and KLA-Tencor Flexus curvature measurement. The sheet resistance measurements were used to monitor changes during the self-anneal and reflect the average of 49 points distributed evenly over the wafer surface. The microstructural properties of the films were studied primarily with a scanning electron microscope. A Philips XL-30 FEG scanning electron microscope (SEM) with sample heater has been redesigned to enable real-time SEM monitoring of the microstructural evolution at elevated temperatures up to 300°C by taking backscattered electron (BSE) images of a certain region on the sample at well defined moments in time. Moreover, using correlation functions it is also possible to take a large number of detailed overlapping images and construct a detailed overall image of a large area. In this way, it is possible to construct grain growth "movies" on both blanket wafer level and in narrow features. Additionally, this technique is combined with an automated EBSD (electron backscatter diffraction) system, so that additional information about the crystallographic orientation of the grown copper grains can be obtained. The orientation mapping of Cu films was carried out during self-annealing and before and after heat treatments. In the following, a detailed record of the experimental results is presented.

Section 4.2. discusses the microstructure and texture of as-deposited thin copper films on a 10nm TaN/5nm α-Ta barrier using different sputter bias conditions.

In section 4.3, we examine the self-annealing of a standard 50W sputtered copper film on a 10nm TaN/5nm α-Ta barrier at room temperature. As will be shown, a new growth mode, also called super secondary grain growth (SSGG), was found in thick copper seed layers besides the frequently observed secondary grain growth mode (SGG), driving the system to a more {100} texture with grain sizes in the order of 50μm.

Section 4.4 focuses on the effect of the annealing temperature on the textural evolution in a 50W sputtered 500nm thin copper film on a 10nm TaN/5nm α-Ta barrier.

Section 4.5 discusses the influence of the copper sputter bias conditions on the microstructural and textural evolution in thin copper films at room temperature and elevated temperatures. All these experiments were carried out with a 10nm TaN/5nm α-Ta barrier layer underneath the copper films. Remark that the sputter bias conditions used in this work actually correspond to certain voltage applied to the substrate. The correlation between the bias conditions and the applied voltage depends on several parameters like the chamber pressure and the specific chamber design. The exact relationship is not known to us, because this confidential information was not released by the manufacturer of the sputter tool. In any case, it should be noted that a rough estimation of this relationship can still be made. First of all, we should notice that a 0W bias condition doesn't correspond to a zero voltage condition, but rather to some low negative voltage, due to capacitive coupling (see figure 3.2; chapter 3). Secondly, for higher sputter bias conditions, the negative voltage applied to the substrate will first increase sharply with increasing bias conditions and gradually relaxes towards a certain negative voltage. Finally, the voltage corresponding to a 250W bias condition can be roughly estimated to be of the order of -50V to -100V.

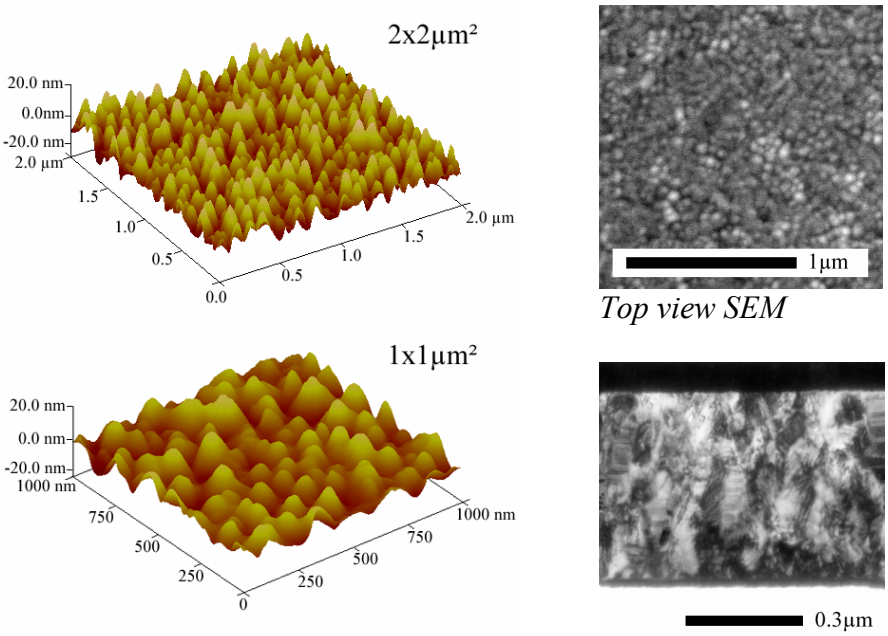
In section 4.6, the influence of the layer thickness on the textural and microstructural changes during self-annealing at room temperature in sputtered copper films will be investigated. More in particular, the impact on both the SSGG and SGG growth modes will be discussed.

Section 4.7 shows the impact of different barrier compositions and textures on the appearance of the SSGG growth mode.

Section 4.8 summarizes the main results of this chapter

4.2 Grain structure and texture after deposition

Figures 4.2 show respectively a top view atomic force microscopy (AFM) image, a top view secondary electron SEM image and a cross sectional TEM image (bright field) of an as-deposited 500nm thick sputtered copper film on top of a 10nmTaN/5nm α-Ta barrier. The used sputter bias conditions for the copper film and diffusion barrier are respectively 50W and 100W. As shown by AFM, the sputtered copper film is continuous with a roughness of about 3-4nm. Moreover, both the top view SEM and cross sectional TEM images reveal the fine grained microstructure of the as-deposited copper film. From both surface and cross sectional images, the in-plane grain size is estimated in the order of 50-100nm. As illustrated on the cross sectional TEM image, a number of columnar grains appear in the as-deposited copper film. These columnar grains usually contain a lot of twins (parallel to the film substrate surface) and do not always span the entire film thickness.



Atomic Force Microscopy (AFM)

Top view SEM

X-TEM

Figure 4.2: Atomic Force Microscopy (AFM) images, top view SEM image and cross sectional TEM (bright field) image of an as-deposited 500nm (50W) sputtered copper film on a 10nmTaN/5nm α-Ta barrier layer.

The number of columnar grains is dependent on the deposition process parameters and the actual film thickness. In general, with increasing film thickness the columnar area decreases, resulting in a more three dimensional grain structure (i.e., non-columnar). However, thick films are difficult to fabricate using physical vapour deposition in view of heating effect of the sputtering process and the poor thermal conduction in a vacuum environment. An insufficient cooling of the substrate during deposition may result in microstructural changes during film formation [26]. In order to avoid this, we only focused on copper film thicknesses where sufficient active cooling of the substrate was guaranteed (i.e. the substrate temperature during deposition is kept in the temperature range between -5°C and 0°C, while the film thickness is varied from 100nm to a maximum of 500nm). To determine a more accurate value for the initial grain size and to reveal both the grain size distribution and orientation distribution of the as-deposited film shown in figure 4.2, orientation mappings were carried out using the EBSD technique. Figure 4.3 shows the grain size distribution for the as-deposited 500nm copper film, as determined with the EBSD technique.

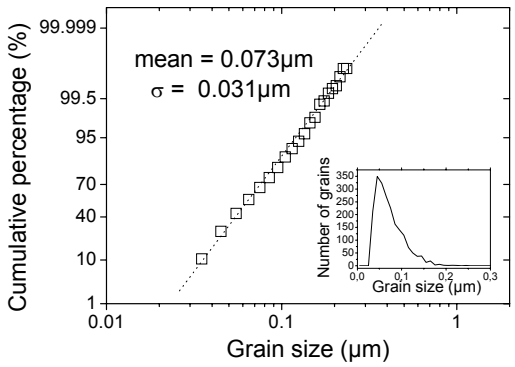
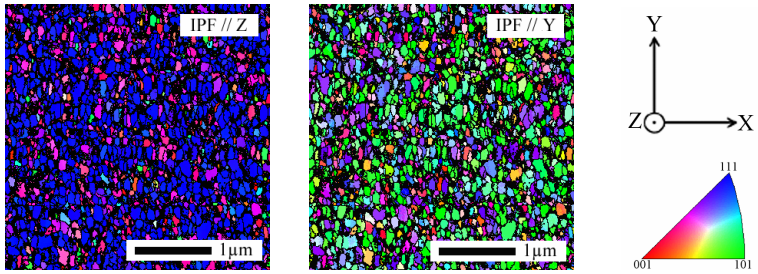


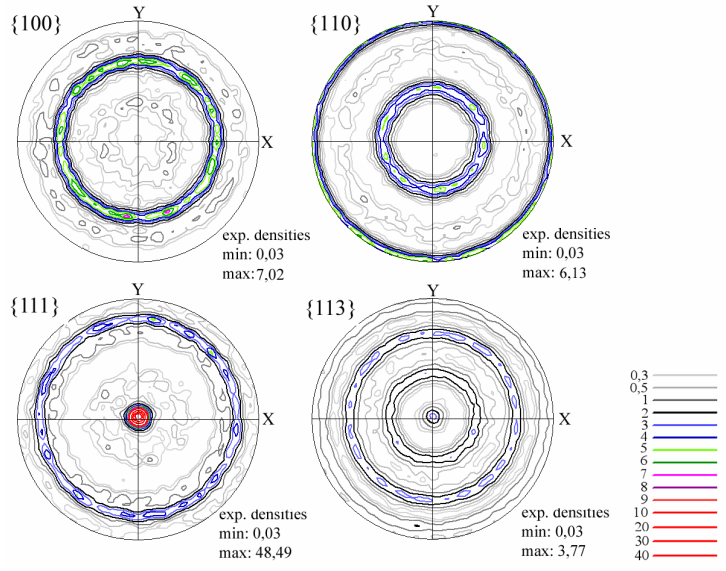
Figure 4.3.: grain size distribution of a 500nm (50W) thick PVD copper film on a 10nmTaN/5nm α-Ta barrier layer. The grain size distribution was determined using a step size of 10nm during the EBSD measurement.

The mean grain size is about ~70nm with a standard deviation of 30nm. This agrees with the estimated value based on the SEM surface images and cross sectional TEM images. Notice that the linear course of the data points on the cumulative grain size distribution plot (figure 4.3) suggests a lognormal grain size distribution. Figures 4.4a-c show the grain texture with respect to the film normal direction (IPF // Z) and an in-plane

direction (IPF // Y) for a 500nm thick as-deposited copper film. The step size (i.e. the distance between two measured data points) used in these mappings was 10nm. The colour of each point in both maps corresponds to the crystallographic orientation with respect to a certain direction (in this case the Y and Z direction) and is defined by the stereographic unit triangle colouring scheme, as indicated on figure 4.4a. In these mappings, the badly indexed or non-indexed points, which are identified using the confidence index of the software, are coloured black.



(a)

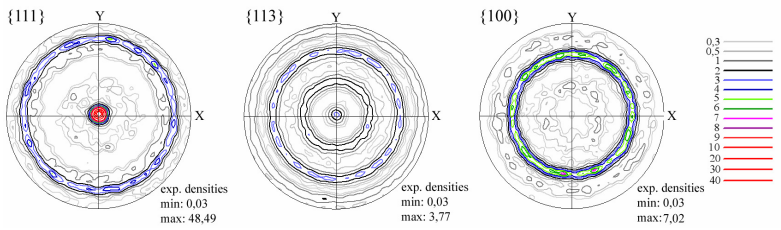


(b)

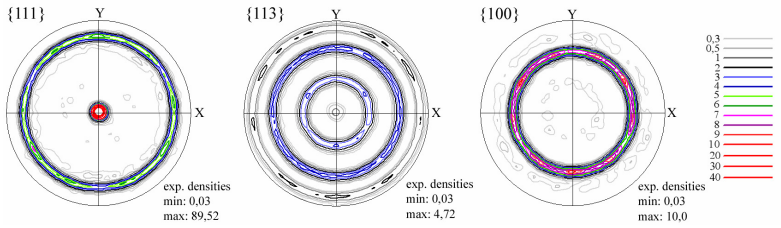
Figure 4.4: (a) top view EBSD maps of the initial texture of a 500nm thick PVD copper film on a 10nm TaN/5nm α-Ta barrier, revealing the texture with respect to the film normal (IPF // Z) and the in-plane Y-direction (IPF // Y). (b) {100}, {110}, {111} and {113} pole figure contour plots with respect to the film normal (Z-direction).

Badly indexed or non-indexed points can have several origins. Destructive interferences between diffraction patterns may for instance occur when the grain sizes of the investigated microstructure are too small compared to the spatial resolution limit of the beam, or when the lattice is locally deformed due to for instance high internal stress. Even when the grain sizes are big enough compared to the chosen step size, still some overlap of diffraction patterns occurs in the surrounding area of grain boundaries. Moreover, inside grain boundaries itself, no diffraction patterns are detected. For more details about the EBSD technique and data retrieval, we refer to section 3.2.2. As can be seen from figure 4.4a, most of the grains in the as-deposited copper film have the {111} planes parallel to the film surface (i.e. the blue coloured grains for the IPF // Z map), but can have different in-plane orientations (IPF // Y map). A more appropriate way to present the texture of the as-deposited 500nm sputtered copper film is on pole figure contour plots as shown on figure 4.4b. The pole figures are shown for the {100}, {110}, {111} and {113} planes. The appearance of a high grain density in the centre of the {111} pole figures and the circular grain density around the centres of {100}, {110}, {111} and {113} pole figures at respectively 54.7°, 35.3°/90°, 70.5° and 29.5°/58.5°/80.0° suggest a strong {111} out-of-plane texture (~50 times as strong as random texture) with a random in-plane orientation, also known as a strong {111} fiber type texture to the film normal direction. This strong {111} fiber texture is often observed in FCC materials like copper, as for these materials the close-packed (111) surface has the lowest surface energy. Besides this strong {111} fiber type texture to the film normal direction, also a weaker {113} texture is found with respect to the film normal (~4 times as strong as random texture), as illustrated by the higher grain density in the centre of the {113} pole figure. The influence of the copper sputter bias conditions on the as-deposited texture is illustrated on figures 4.5a-c. For these copper films, the barrier sputter bias and film thickness were kept constant at respectively 100W and 500nm. For all sputter bias conditions, the sputter gas pressure, substrate temperature and the particle flux coming from the sputter target were kept constant during deposition. Therefore, the only parameter that was changed during the deposition of these films was the sputter bias voltage applied to the film substrates. Figures 4.5a-b show the {100}, {113} and {111} pole figures in case of a 50W and 250W sputtered copper film, while figure 4.5c shows the orientation fraction for the (111) and (113) texture components as a function of the misorientation angle. This figure

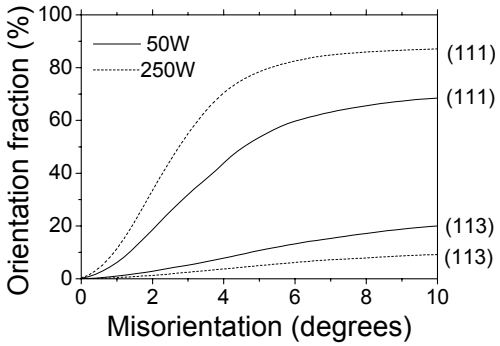
shows that the as-deposited 50W sputtered copper film has the smallest volume fraction of the (111) component and the highest volume fraction of the (113) component. Within the frame of this work, this kind of texture will be called “low {111}”. In contrast, the texture of a 250W sputtered copper film will be called “high {111}” since it has a higher amount of (111) component and smaller amounts of the (113) component.



(a) 50W sputtered as-deposited film



(b) 250W sputtered as-deposited film



(c) Orientation fraction as a function of the misorientation angle

Figure 4.5: {100}, {113} and {111} pole figures of respectively (a) 50W and (b) 250W 500nm thick sputtered copper films. (c) shows the orientation fraction of the (111) and (113) texture components as a function of the misorientation angle.

When taking into account all the grains with a misorientation below 10°, the orientation fraction of the (113) component decreases from about 20% for the 50W sputtered copper films to about 10% for 250W sputtered copper films. Moreover, figure 4.5c also reveals that the (111) grains in a 250W as-deposited texture deviate less from the ideal (111), as compared to lower bias conditions. This is also reflected in the observed texture strength of a 50W and 250W copper film, respectively 50 and 90 times as strong as random oriented grains (see pole figures on figures 4.5a-b). Figure 4.6 shows cross sectional TEM images (Bright Field and Dark Field modes) of a 500nm sputtered copper film using respectively 0W and 250W sputter bias conditions. The dark field TEM images are generated using the (111) diffraction spot of the corresponding diffraction pattern (indicated with an arrow on figure 4.6).

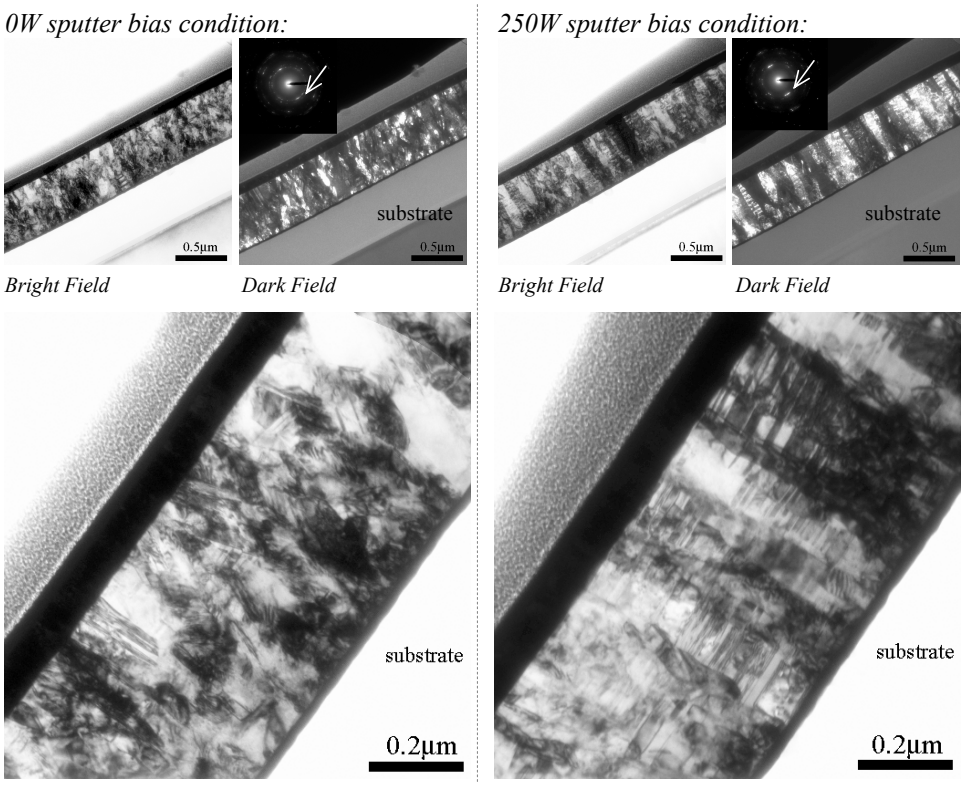


Figure 4.6: Bright and Dark Field TEM images of a 500nm sputtered copper film on a 10nm TaN/5nm α-Ta barrier layer, using either 0W or 250W sputter bias conditions. These images show a clear difference in the as-deposited microstructure and texture.

The position of these diffraction spots with respect to the film normal illustrates the {111} texture for both copper films. These TEM images illustrate a clear difference in the initial grain microstructure and texture between both sputter bias conditions. As shown, a stronger {111} texture (with respect to the film normal) is found in case of a 250W sputtered copper film. This is in agreement with the EBSD measurements, where the same phenomenon was observed (figure 4.5). For both sputter bias conditions, columnar grains can be found. The number of columnar grains and their mean in-plane grain size increases for higher sputter bias conditions. Notice that in case of high sputter bias conditions these columnar grains often span the entire film thickness and contain a lot of twins parallel to the film surface.

In literature, atomistic modelling of physical vapour deposited copper films indicated that during growth of a {111} texture, adatoms occupied either parent or twin surface lattice sites with almost equal probability, thereby resulting in a high nucleation density of twin domains [27]. Because larger bias voltages result in an increased energetic ion bombardment of the growing film, this may also result in higher adatom mobilities during deposition, thereby increasing the probability of occupying twin surface lattices and resulting in a higher number of twins in the as-deposited film. It is likely that due to this increased probability, the grain size and grain shape near the film/substrate interface are maintained during further deposition, thereby resulting in a more pronounced columnar structure. Moreover, higher adatom mobilities may be responsible for the observed increased in-plane grain size for higher sputter bias conditions. Besides the higher adatom mobilities, the increased energetic ion bombardment also results in a resputtering effect of the adsorbed material during thin film formation. It is plausible that due to this resputtering effect, some orientations are removed at the expense of others. Because the {111} planes are the close-packed planes for FCC materials, it is more likely that other orientations are resputtered during deposition. This might explain the decreased {113} and increased {111} texture strength for higher sputter bias conditions. Another explanation for the occurrence of twins inside these columnar grains may be attributed to stress relief/strain relaxation inside the copper films during deposition. An increased energetic ion bombardment of the growing film for higher sputter bias voltages may also result in larger internal strains, therefore also increase the possibility of subsequent stress/strain relaxation in the film normal direction by means of twin formation. This does not

necessarily mean that the magnitude of the as-deposited film in-plane stress also decreases with increasing sputter bias conditions. On the contrary, as illustrated on figure 4.7, the in-plane film stress increases in size for higher sputter bias conditions. This may be attributed to the increased number of columnar grains for higher sputter bias conditions. In this case, the grain boundary volume is more located in the neighbourhood of the columnar grain boundaries, while for lower sputter bias conditions (and less columnar grains) a part of the grain boundary volume is also located in grain boundaries which are not parallel to the film normal. In this way, the in-plane stress can more easily be relaxed in the case of low bias conditions, as compared to the more columnar structure for high sputter bias conditions.

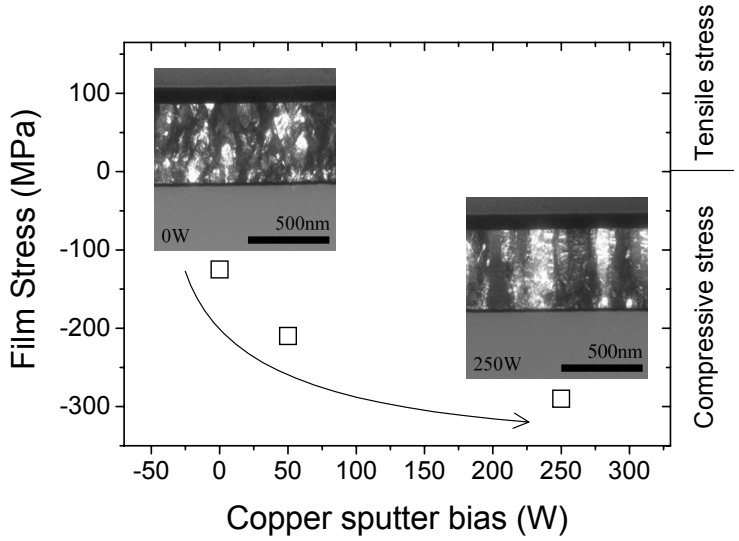
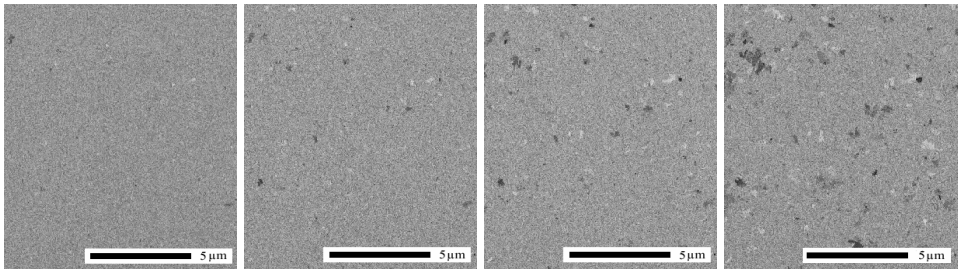


Figure 4.7: initial in-plane film stress and microstructure as a function of the copper sputter bias, revealing the strong correlation between stress, microstructure and texture of the 500nm as-deposited copper films.

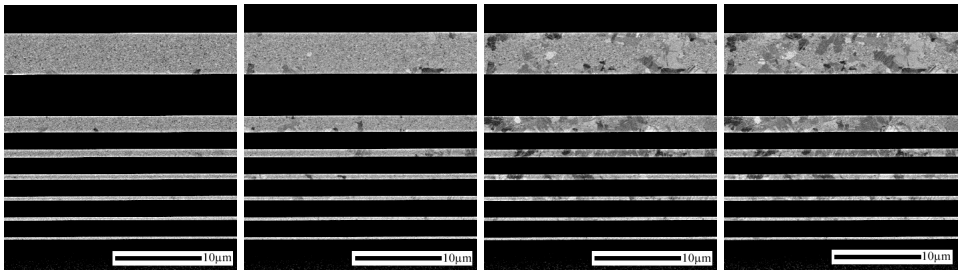
The influence of the initial microstructure/texture on the further self-annealing behaviour of these sputtered copper films will be discussed in the following sections. Here, we will focus on the growth dynamics, growth velocity, final grain size and grain size distributions and grain textures in 500nm thick sputtered copper films on a 10nm TaN/5nm α-Ta barrier.

4.3 Abnormal growth of giant grains during textural evolution in sputtered copper films: Super Secondary Grain Growth

In the previous section, we discussed the initial microstructure, grain texture and grain size distribution of as-deposited 500nm copper thin films on a 10nm TaN/5nm α-Ta barrier layer. In this section we will further focus on the microstructural evolution of a standard 50W sputtered copper film at room temperature, using the real-time SEM monitoring technique, the EBSD technique and by performing both sheet resistance and stress measurements at different moments in time. The observed trends will be compared with the behavior seen in most of the Self-Ionized Plasma (SIP) deposited seed layers and electrodeposited copper films known today. Before discussing the microstructural evolution in sputtered copper films, we will first briefly describe the self-annealing behaviour of electroplated copper films and structures.



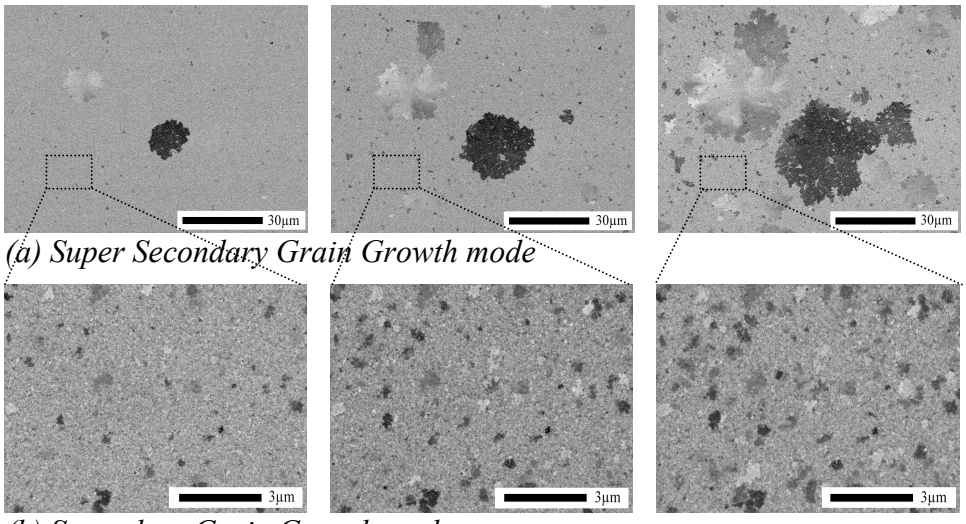
(a) blanket film



(b) patterned structure

Figure 4.8: (a) microstructural evolution of a 500nm electroplated copper blanket film and (b) a patterned wafer with a line depth of 500nm and line widths varying from 5µm (top) to 300nm (bottom).

Figures 4.8a-b show the microstructural evolution in respectively a 500nm thick electroplated copper blanket or unpatterned film (figure 4.8a), and in narrow structures with a line depth of 500nm and line widths varying from 300nm to 5μm (figure 4.8b). Notice that these electroplated copper films were produced using a 10nm TaN/5nm α-Ta barrier layer and a 70nm thick sputtered copper seed layer underneath to ensure electrical contact during electroplating. By taking backscattered images at well defined moments in time of the same region on the film, these real-time experiments reveal that secondary grain growth (SGG) in electroplated (ECD) copper blanket layers and narrow structures happens rather erratically. In literature, this observed trend is believed to be strongly influenced by the additive concentrations as determined by the plating process [28-29]. Typical final grain sizes are in the order of several microns. A very similar behaviour is also seen in SIP deposited copper seed layers on most barrier layers used today [26, 30].



(a) Super Secondary Grain Growth mode

(b) Secondary Grain Growth mode

Figure 4.9: backscattered images taken after 4 days, 1 week and 2 weeks after deposition (from left to right), revealing two different growth modes at room temperature in a 500nm sputtered copper film.

Figures 4.9a-b show the microstructural evolution of a 500nm thick copper film on a 10nm TaN/5nm α-Ta barrier layer at room temperature. These real-time experiments reveal that the grain growth in this copper

film is strikingly dominated by grains that grow much more rapidly and to very large sizes in the order of ~50µm (figure 4.9a). Additionally, the growth is highly concentric, as the grains grow almost circular until the grain boundaries meet those of other super grains. This behaviour is rather unusual in SIP deposited copper layers and differs from the commonly observed Secondary Grain Growth (SGG) in electroplated copper and SIP deposited copper films on most barriers used today [17, 26-30]. In this work, we will name this new highly concentric grain growth mode Super Secondary Grain Growth (SSGG). It should however be noticed that besides this SSGG-mode, the Secondary Grain Growth mode (SGG) is still observed in between these super grains (figure 4.9b). Be aware that both growth modes happen at different scales. Because backscattered electron images give no quantitative texture information, a more detailed real-time EBSD study of this novel SSGG-mode was carried out at room temperature as shown on figure 4.10.

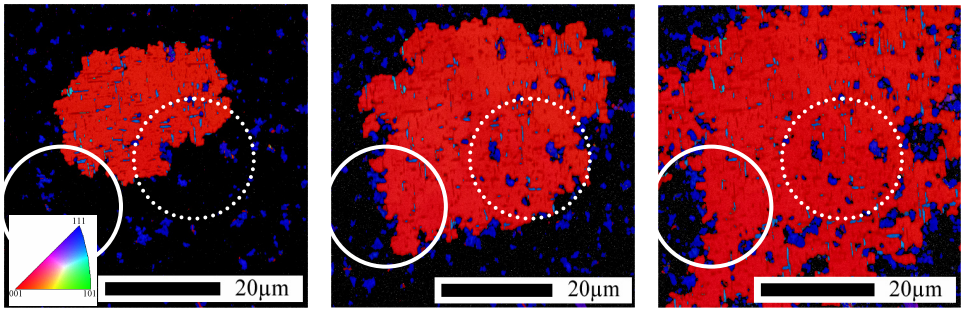


Figure 4.10: top view EBSD maps of a 500nm Cu seedlayer (50W) on a 10nm TaN/5nm α-Ta barrier (100W) taken respectively 4 days, 1 week and 2 weeks after deposition.

This figure shows the grain orientations with respect to the film normal direction (or Z-direction) at respectively 4 days, 1 week and 2 weeks after deposition of the same region on a 500nm copper film. The step size for these maps, i.e. the distance between two adjacent indexed points on the map, was taken at 100nm. The orientations correspond to the colours defined by the stereographic unit triangle colouring scheme. The black regions are positions on the film where no indexation was possible, due to either lattice deformation, grain boundaries or the rather small initial grain sizes (~70nm) as compared to the used step size. As can be seen from figure 4.10, the highly concentric super grains are mainly (100) oriented

and contain a lot of twin structures inside. On the other hand, the SGG-mode mainly contains (111) oriented grains. Moreover, as can be seen from these EBSD measurements, there is a clear rivalry between these two growth modes (SSGG and SGG).

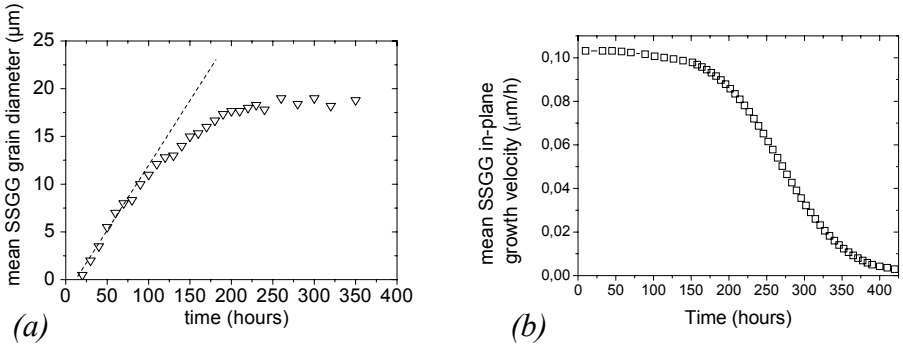


Figure 4.11: (a) the mean grain diameter and (b) the mean in-plane growth velocity of SSGG grains as a function of time. The grain diameter was calculated from real-time grain growth experiments on a 500nm (50W) sputtered copper film.

During the SSGG growth process, these (100) oriented super grains can grow around (111) oriented SGG grains (see dotted circles on figure 4.10) until these super grains eventually collide with other super grains or until a sufficiently high density of SGG grains is reached. In the latter case, these super grains can also be blocked by the (111) oriented SGG as shown in the non dotted area on figure 4.10. The stagnation of the SSGG growth mode can also be illustrated in another way by plotting the mean SSGG grain diameter as a function of time during the self-annealing process (figure 4.11a). Using these data points, the mean in-plane growth velocity for the SSGG grains can be deduced by calculating the derivative of the curve shown on figure 4.11a. In order to quantify the SSGG in-plane growth velocity, the SSGG grain diameter can be estimated by a linear fitted curve during the first steps of the self-annealing process, as illustrated on figure 4.11a. Notice that this is only a simplified estimation, as the actual mean grain diameter gradually deviates from this linear behaviour during the self-annealing process and eventually leads to a to a stagnation of the SSGG growth mode, illustrated by the decreased mean SSGG in-plain growth velocity on figure 4.11b. In any case, this method

already gives a good quantification of the SSGG in-plane growth velocity and enables us to compare the SSGG in-plane growth velocities for different deposition conditions and post-deposition annealing temperatures further on in this work (see sections 4.4 and 4.5). During all real-time grain growth experiments discussed in this work, the in-plane growth velocity was always determined from the linear diameter versus time behaviour.

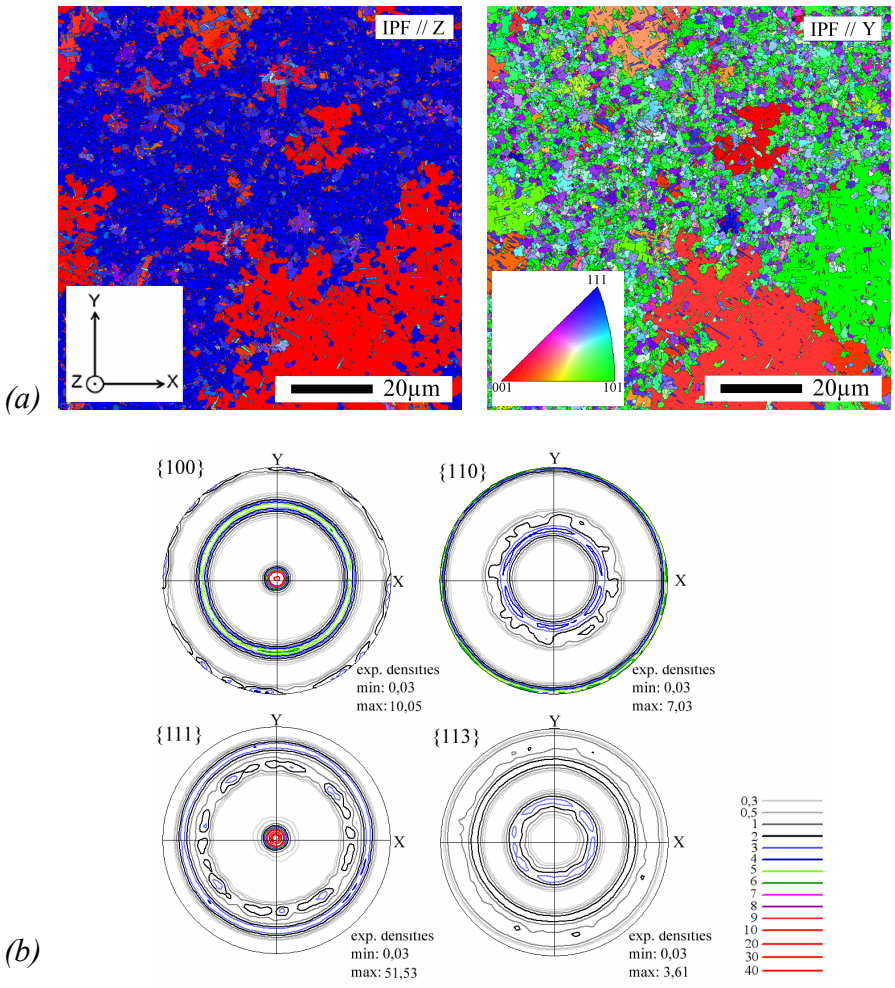


Figure 4.12: (a) top view EBSD measurements of a 500 nm PVD copper film on a 10nm TaN/5nm α-Ta barrier layer and (b) {111}, {110}, {113} and {100} pole figure contour plots.

Figure 4.12 shows the final film texture of a 500nm thick copper film with respect to the film normal direction (left) and an in-plane direction (right) after self-annealing 3 months at room temperature. The super grains (around ~50µm in diameter) are all (100) oriented with respect to the film normal and are located in a matrix of smaller (111) oriented grains (around ~1µm in diameter). Moreover, the IPF // Y map shows that these super grains have different in-plane orientations, demonstrating the fiber type texture for the SSGG growth mode.

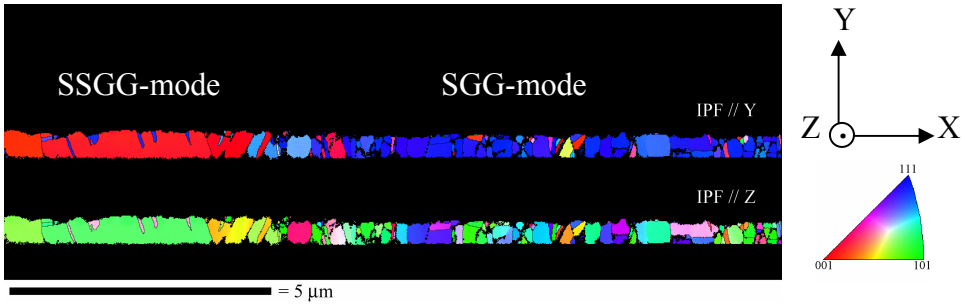
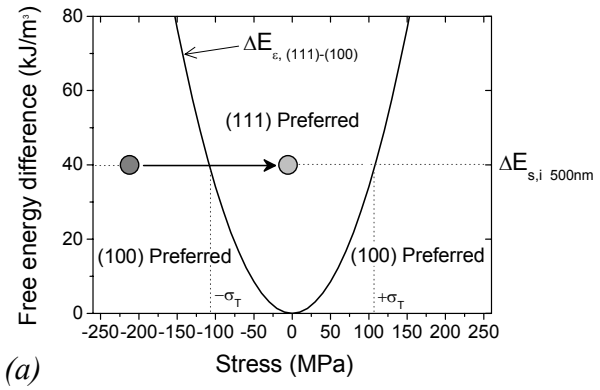


Figure 4.13: cross sectional EBSD measurement of a 500 nm PVD copper film on a 10nm TaN/5nm α-Ta barrier layer. The upper image shows the grain orientation along the Y direction (film normal), while the lower image shows the orientation along the Z direction.

As illustrated on the cross sectional EBSD measurements after self-annealing on figure 4.13, these super grains have all grown in a columnar way throughout the film thickness, while this is not always the case for some of the smaller (111) oriented secondary grains. On figure 4.13, the grain orientation is shown with respect to the film normal (IPF // Y) and an in-plane direction (IPF // Z). In this way, we may conclude that the initial strong {111} fiber texture with grain sizes of about 50-100nm transforms in a time period of three months at room temperature to a mixture of strong {100} and {111} fiber textures, i.e. a strong texture with respect to the film normal and a random in-plane texture. The appearance of the (100) orientation for the super grains together with the observation of twin structures inside these grains hints at a stress driven grain growth mode [1]. To further explain the textural evolution in this film during self-annealing, the surface/interface energy density difference $\Delta E_{s,i}$ and strain energy density difference ΔE_{ε} between the two mainly observed

orientations, i.e. (111) and (100), can be plotted as a function of stress on a so called texture map, as illustrated on figure 4.14a, hereby using $\Delta E_{(111)-(100)} \cong 146.4\ \varepsilon^2$ GJ/m³ (see figure 2.7; chapter 2) and the measured elastic modulus M of about 204GPa (as determined from thermal cycling experiments) to convert strain to stress values. Notice that in order to extract the elastic modulus from the thermal cycling experiments, we use the difference in thermal expansion coefficients between copper and the silicon substrate, i.e. $\Delta\alpha_{Cu\text{-}Si} \cong 14.1 \times 10^{-6}$/°C [31]. For simplicity, the influence of the barrier layer on the thermal expansion coefficients between copper and the silicon substrate will not be taken into account.



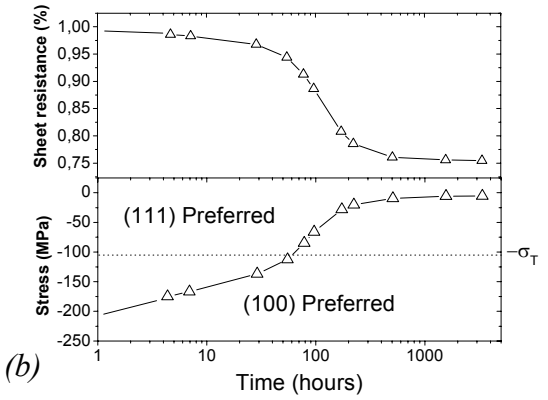


Figure 4.14: (a) difference in surface/interface energy density $\Delta E_{s,i}$ and strain energy density between (111) and (100) oriented grains $\Delta E_{\varepsilon,\ (111)-(100)}$ (b) resistance and stress change over time for a 500nm copper film on a 10nm TaN/5nm α-Ta barrier layer. Data were averaged from 49 points across the whole wafer.

However, as will be shown further on in this work, both barrier composition and texture can influence the self-annealing behaviour of copper films (see section 4.7). Be aware that by converting the strain into stress values it is assumed that the elastic modulus of the film is constant during grain growth. This is only the ideal situation. In reality, the elastic modulus of the film may change during grain growth and therefore may also have an influence on the difference in strain energy density between (111) and (100) oriented grains. Therefore, figure 4.14a shows only the initial situation before any grain growth and stress relaxation occurs and the threshold stress values from this graph describe only an indicative barrier between the two dominating driving forces for the initial situation. For a 1µm thick Cu film the surface/interface energy difference between (111) and (100) grains can be estimated at ~20kJ/m³ [32]. As the surface/interface energy density difference is inversely proportional to the film thickness, the value for a 500nm thick copper layer can be estimated at ~40kJ/m^3 (see equation 2.7; chapter 2). This then leads to a threshold stress σ_T of about 105MPa in size, either tensile of compressive, as indicated on the figure as a dotted line. For stress values above the threshold stress $|\sigma_T|$, the difference in strain energy density exceeds the difference in surface/interface energy density, and the minimization of the strain energy is the dominant driving force for textural evolution in these films. Therefore, in figure 4.14a, a {111} texture is favoured in the regime above the strain energy density curve, whereas a {100} texture is favoured in the regime beneath the strain energy density curve. Both the film stress and sheet resistance were monitored over time during the self-annealing process and compared with the obtained microstructural/textural evolution using the real-time SEM monitoring technique and EBSD technique. Sheet resistance measurements were performed using the four probe method at room temperature immediately after deposition. The stress measurements were done by wafer curvature measurements. The threshold stress value for the initial situation before grain growth is determined from figure 4.14a and is indicated on the stress versus time plot. As can be seen from figure 4.14b, there is a strong correlation between the stress evolution from its initial tensile stress value of -212 MPa (also indicated on figure 4.14a) to a final film stress value of about -5MPa, and the decrease of almost 25% in sheet resistance during self-annealing. This suggests that the tensile trend of the stress is mainly induced by grain growth during the self-annealing process (SSGG and SGG growth modes). Since the initial film texture can be described as a strong {111} fiber texture and the initial

stress value before grain growth is far below the threshold stress value of -105MPa on figure 4.14, grain growth will start from a region on the texture map where strain energy density minimization is favoured over surface/interface energy minimization as the dominating driving force ($\Delta E_{s,i} > \Delta E_{\varepsilon}$). Therefore, during the first stages of grain growth, the (100) grain orientations are favoured to grow at the expense of other orientations [1]. However, despite this advantage this does not mean that no (111) oriented grains will develop during these first stages of grain growth, but rather that a lot of grains have the energetic advantage to change into the energetic favourable (100) orientation under these stress conditions. This agrees well with the real-time SEM/EBSD experiments on figures 4.9 and 4.10, which revealed the presence of both SGG and SSGG grains during this period. Besides the super grains also (111) oriented SGG grains were observed. Notice that during the self-annealing process, the impact of the strain energy minimizing driving force is decreased when the stress relaxes in the tensile direction (figure 4.14b) and therefore the film stress on the texture map shifts more towards the region where surface/interface energy minimization is dominating the film textural evolution (figure 4.14a), thereby favouring more the growth of (111) oriented grains. This is in good agreement with the gradually decreased SSGG in-plain growth velocity during self-annealing (see figures 4.11). Moreover, we need to keep in mind that the threshold stress value is only valid for the initial situation before grain growth occurs, so this is merely an indicative barrier between the two different dominating driving forces during grain growth. In other words, the observed SSGG growth mode will not stop instantaneously once the measured in-plane film stress has crossed the threshold stress, nor will the SGG growth mode be absent for in-plane stress values below the threshold stress. This is mainly because only the global in-plane film stress is measured with the wafer curvature technique (see chapter 3, section 3.2.4), while in reality, there can still exist some large local stress variations between different grains, as illustrated by [33-36]. In this way, it is plausible that some SSGG grains can locally grow further even when the global film stress is above the threshold stress. In any case, the position of the threshold stress on the texture map, somewhere halfway between the initial and final film stress value on figure 4.14 is in good agreement with the clearly observed competition between the two different growth modes during the self-annealing process and the observed mixture of both {100} and {111} fiber textures after 3 months of self-annealing.

4.4 Influence of the annealing temperature on the textural evolution in sputtered copper films.

In the previous sections, we discussed the textural evolution of a 500nm thick sputtered copper film on a 10nm TaN/5nm α-Ta barrier layer at room temperature and explained the observed trends in terms of surface/interface energy minimization and strain energy density minimization. In these sections, we observed a new growth mode (SSGG) in thick sputtered copper films, which leads to a highly concentric growth of super grains of many tens of microns in diameter and drives the system more towards a {100} texture. Moreover, a clear rivalry between this SSGG growth mode and the regularly observed Secondary Grain Growth (SGG) mode in sputtered copper films was found, where the latter drives the system to a more {111} texture. In order to investigate what the influence of the annealing temperature is on the textural evolution in a 500nm copper thin film on a 10nm TaN/5nm α-Ta barrier layer, this film was annealed at 4 different temperatures ranging from room temperature to 80°C. During these annealing steps, the microstructural evolution is studied using the real-time SEM monitoring technique and the EBSD technique. Figures 4.15a-c illustrate the final texture and grain size in case of 4 different annealing temperatures. As can be seen from these figures, a clear change in the ratio of the (100) and (111) fraction is noticeable, meaning that as the annealing temperature increases, there is a clear change in competition between the driving forces for the SGG and SSGG, i.e. respectively surface/interface energy minimization and strain energy density minimization. This change results in a decrease of the final SSGG grain size and SSGG film coverage with increasing annealing temperature, while the opposite trend can be found for the SGG mode. Possible explanations for these observed trends can be either a lower initiation rate of the SSGG growth mode for elevated temperatures, compared to room temperature, or a difference in thermal activation of the SSGG growth mode compared to the SGG growth mode, thereby inhibiting extensive SSGG. As can be seen on table 4.1, the number of (100) oriented grains with a diameter above 10μm decreases for increasing temperatures, as well as the maximum and mean grain diameter of these grains. However, the total number of (100) oriented grains is more or less constant for all annealing temperatures, meaning that annealing does not change the number of nucleated SSGG grains in the film, but only their final

diameter. This will then lead to the observed reduced (100) orientation fraction for higher annealing temperatures. This suggests that the SSGG initiation rate is comparable for different annealing temperatures.

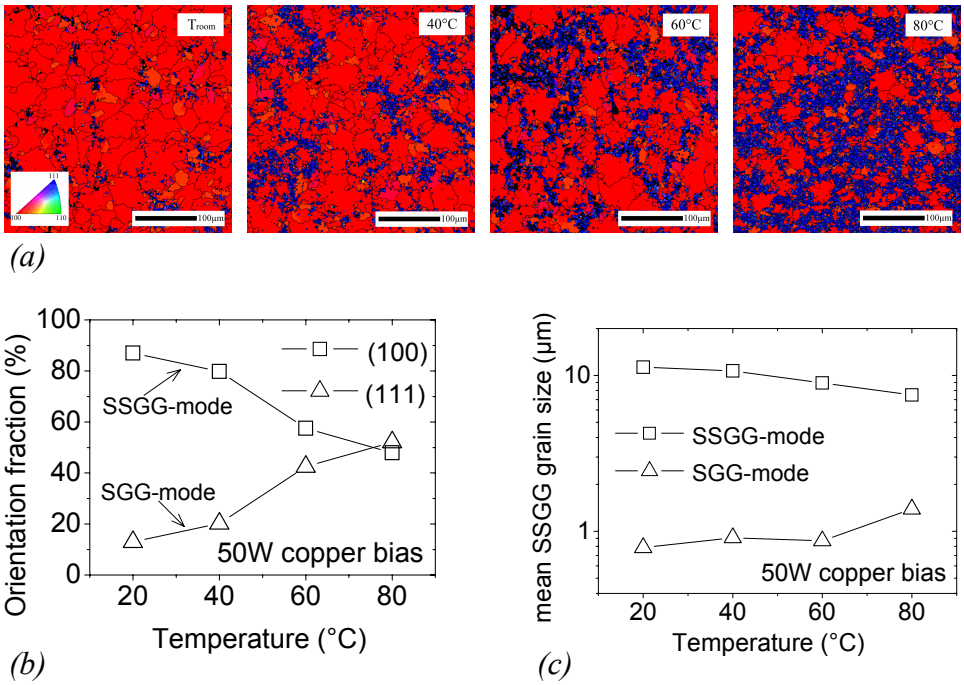


Figure 4.15: (a) EBSD mappings of a 500nm copper film as a function of the annealing temperature. (b) influence of the annealing temperature on the orientation fraction and (c) SSGG and SGG grain size as a function of the annealing temperature. The (100) and (111) orientation fractions were determined taking into account all the grains with a misorientation below 15° compared to the ideal (100) and (111) orientations.

In order to determine the activation energy for the SSGG growth mode, we use the real-time SEM monitoring technique. Because the super grains grow concentrically, this can easily be done by determining the mean grain diameter as a function of time. In this way, the mean in-plane SSGG growth velocities for different temperatures can be determined and the activation energy can be extracted when the determined velocities are plotted in an Arrhenius-plot as shown on figure 4.16. In this representation, the activation energy E_a is proportional to the slope. It is

found that the SSGG growth process is thermally activated with an activation energy of about ~0.77eV ± 0.05eV. This is somewhat lower than the activation energy for SGG in ECD copper found in literature (~0.93eV), which corresponds to copper grain boundary self-diffusion [37-38]. The slopes corresponding to both activation energies are illustrated on figure 4.16. Notice that both slopes were normalised to the same grain growth velocity at room temperature. In this way, the growth velocity for both growth modes can be compared at elevated temperatures (see figure 4.16b).

SSGG growth mode	Troom	40°C	60°C	80°C
total # of grains	4781	4859	4829	4748
# of grains < 10µm	2858	3171	3372	3322
# of grains > 10µm	1923	1687	1457	1426
(100) fraction	87	79.8	57.5	47.9
maximum diameter	86	82	73	50
mean diameter	11.3	10.7	8.9	7.5

Table 4.1: overview of the number of grains, grain diameter, and orientation fraction for the SSGG growth mode. These values were calculated using EBSD maps of 1000 x 1000 µm² and a step size of 1µm.

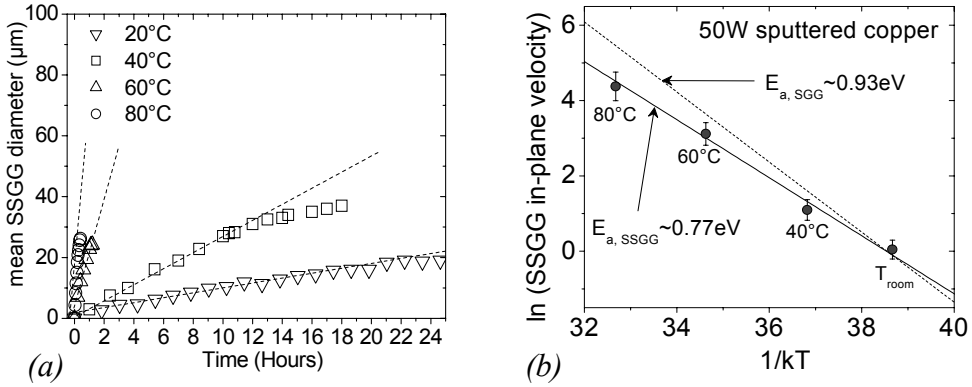


Figure 4.16: (a) mean grain diameter as a function of time determined using the real-time SEM monitoring technique and different annealing steps (b) Arrhenius-plot for the determination of the SSGG activation energy, using the SSGG in-plane growth velocity.

In the previous sections, we already showed that the two observed growth modes (SSGG and SGG) in these copper films lower the energy of the total system by means of mainly two different driving forces, i.e. strain energy density minimization for the SSGG growth mode and surface/interface energy minimization for SGG growth mode. In general, these minimization processes happen faster at elevated temperatures. However, due to the observed lower activation energy for super grains (i.e. $E_{SSGG} \sim 0.77eV$; $E_{SGG} \sim 0.93eV$), the energy minimization by the SGG growth mode will respond faster at elevated temperatures as compared to the SSGG growth mode. In this way, the chance that super grains encounter energetically unfavourable material during their growth increases severely, thereby blocking those super grains from growing further in size. This will eventually lead to a decreased SSGG grain size and orientation fraction for copper films annealed at elevated temperatures, even though the number of nucleated super grains can be the same for different annealing temperatures, as observed.

4.5 Influence of the sputter bias on the appearance of Super Secondary Grain Growth in sputtered copper films.

In the previous section we examined the influence of the annealing temperature on the textural evolution in sputtered copper films on a 10nm TaN/5nm α-Ta barrier, using standard Cu and barrier sputter bias conditions. In this section, we will further investigate the effects of different copper sputter bias conditions on the textural evolution in sputtered copper films at room temperature and elevated temperatures.

4.5.1 Room temperature behaviour:

Figure 4.17a shows the mean in-plane growth velocity for the SSGG growth mode at room temperature as a function of the copper sputter bias conditions for a 500nm copper seed layer on a 10nm TaN/5nm α-Ta barrier. These velocities were calculated using the mean SSGG diameter evolution versus time as derived from real-time experiments. By increasing the copper sputter bias conditions, a clear increase in self-annealing time of the super grains at room temperature is observed. This is

also reflected in the normalised sheet resistance versus time graphs (see figure 4.17b). As shown on these figures, the biggest difference in self-annealing time can be found between a 0W and a 50W bias, while the difference between the 150W and 250W is much smaller. This decrease in self-annealing time correlates very well with the change in applied voltage on the wafer substrate for different bias conditions during the deposition process.

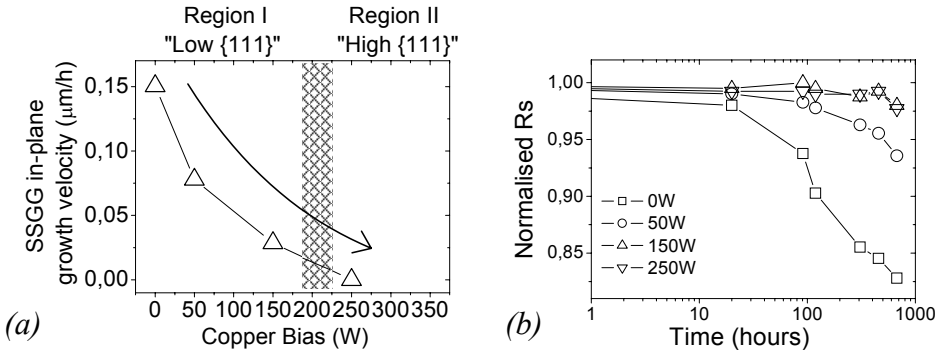
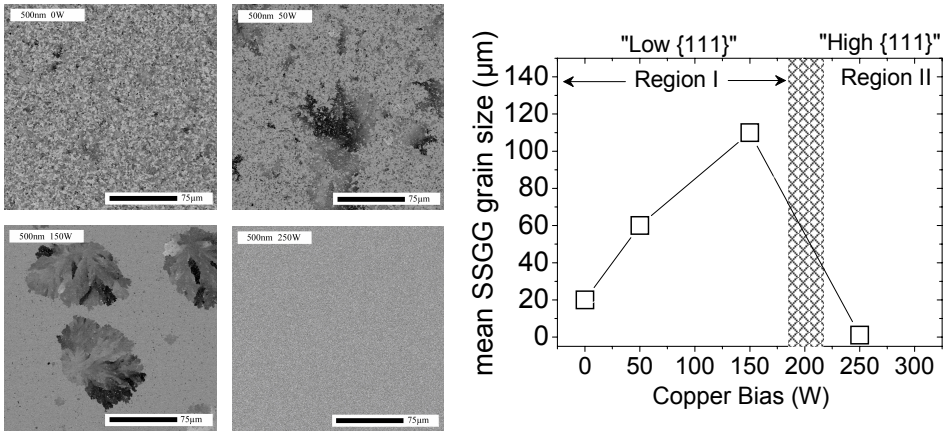


Figure 4.17: (a) influence of the copper bias on the SSGG in-plane growth velocity and (b) the normalised sheet resistance versus time for different Cu bias conditions. The SSGG in-plane growth velocities were extracted from real-time grain growth experiments by determining the mean SSGG grain diameter as a function of time.

Here, also the biggest change in applied voltage can be found between the 0W and the 50W bias, while for higher bias conditions, the applied voltage saturates gradually towards a certain value. Moreover, as already mentioned in section 4.2, also differences in the as-deposited microstructure and texture as a function of the used copper sputter bias condition were found (figures 4.5 and 4.7). Clearly, in case of a 0W sputtered copper film, real-time experiments revealed already super grains after one day, while in case of a 150W sputtered copper film it took up to 6 months to observe considerable super grain growth. Moreover, bias conditions from 0W to 150W, the mean SSGG grain size increases with increasing sputter bias, as illustrated in figure 4.18. This correlates very well with the increased initial film stress observed for higher copper sputter bias conditions (see figure 4.7) and the strain energy minimizing driving force for the SSGG growth mode (see sections 4.3 an 4.4). In this

way, the impact of the strain energy minimizing driving force just after deposition increases with higher initial film stress values. During the subsequent microstructural and textural evolution of the films, this then leads to an increased mean SSGG grain size for higher sputter bias conditions. However, in case of a 250W sputtered copper film, no considerable super secondary grain growth was observed even after 6 months self-annealing at room temperature (see figure 4.18a).



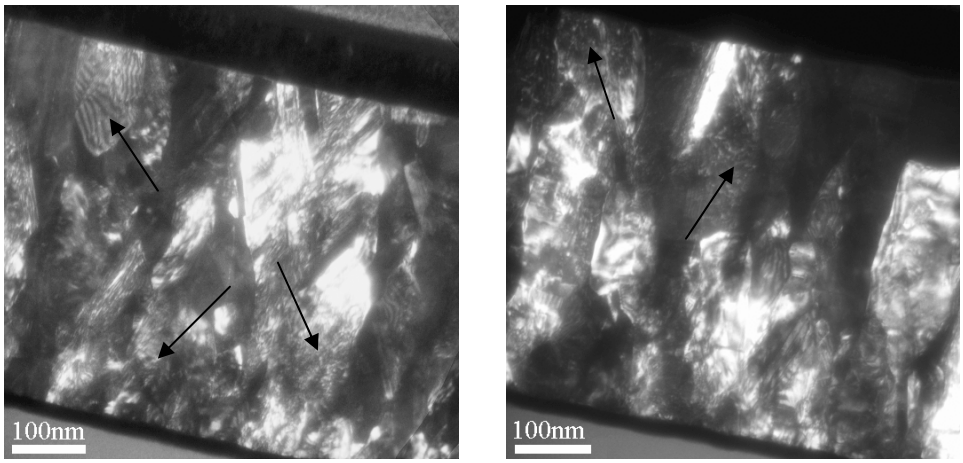
(a) *(b)*

Figure 4.18: (a) top view backscattered images of 500nm Cu films deposited with different Cu sputter bias conditions varying from 0W to 250W. (b) mean SSGG grain size as a function of the copper sputter bias. The images and grain sizes were taken 6 months after room temperature storage.

The absence of the SSGG growth mode for a 250W sputtered copper film stored at room temperature for 6 months can be mainly ascribed to the increased self-annealing time. There can be several explanations for this observed difference in self-annealing time. As grain boundary energy may be one of the possible driving forces for grain growth (see chapter 2), one of the possibilities is that this difference in self-annealing time may be linked to differences in grain boundary energies. Higher bias voltages may possibly result in more relaxed (or low energy) boundaries. This seems plausible, as for low sputter bias conditions the observed as-deposited grains are less columnar and their grain size is smaller as compare to higher sputter bias conditions, therefore leading to higher grain boundary

energies (see table 2.1; chapter 2) and hence may lead to a faster grain growth rate. The fact that different as-deposited microstructures and textures are observed for different sputter bias conditions hints at the fact that the microstructure, texture and grain boundaries play an important role in the self-annealing behaviour (figure 4.6). Another explanation may be due to different concentrations of defects arising from various bias conditions. Higher bias voltages applied to the substrate result in more energetic ion bombardments of the growing film, which in turn, make the surface atoms more mobile, whereby the concentration of defects in form of vacancies decreases. The defect concentration in the sputtered copper films might then act as a driving force for grain growth [30]. Defects within the as-deposited grains may affect the growth kinetics in several ways. First, the presence of for instance dislocations can provide the necessary driving force ΔE (see table 2.1). The movement of a grain boundary can then be driven by the energy released by the annihilation of defects in the as-deposited grains. Secondly, another explanation could be based on the fact that the defects that are built into the film could change the mobility. It is known that diffusion can be significantly enhanced if the density of point defects is higher than the equilibrium value at a given temperature. A non-equilibrium concentration of point defects can be achieved by non-thermal processes such as ion bombardment or irradiation [39-40]. It is possible that defects generated during the low-temperature deposition process could play a similar role in copper films. In this way, a smaller defect concentration (due to higher sputter bias conditions) will lead to a decreased driving force for grain growth. Instead of raising the sputter bias conditions, Detavernier et al. [30] raised the deposition temperature and/or reduced the sputter gas pressure, whereby they also observed a decrease in the rate of grain growth. Similar to raising the bias conditions, the increase in deposition temperature or reduction in gas pressure (more energetic ion bombardment) resulted in a decreasing defect concentration, i.e., a smaller driving force for grain growth. In order to confirm the hypothesis of different defect densities, techniques like TEM or positron annihilation can be used to compare the defect concentrations in the as-deposited films. The preferred technique in this work is TEM due to the very short self-annealing time of the 0W sputtered copper films (self-annealing is already completed 1-2days after deposition) and the impossibility to measure these low sputtered copper films with positron annihilation before self-annealing itself has completed in those films. Figures 4.19a-b show TEM images (Dark Field mode) for

0W and 250W sputter bias conditions. For both sputter bias conditions a number of defects inside the as-deposited grains can be found (see arrows). The appearance of these defects inside the copper grains supports the idea that annihilation of defects inside the grains may drive grain growth in those films. However, it is very complicated to compare the amounts of defects inside the grains for both sputter bias conditions, because of the very small as-deposited grain sizes and the fact that the TEM preparation itself also may generate an additional amount of defects inside the as-deposited copper films. Therefore, no clear conclusions could be made concerning differences in defect densities for different sputter bias conditions.



0W *250W*

Figure 4.19: TEM images (bright field mode) of a 500nm sputtered copper film, using either 0W or 250W sputter bias conditions. Substrate and barrier layer are on the left side of the images. These images reveal an amount of unidentified defects inside the as-deposited grains (arrows).

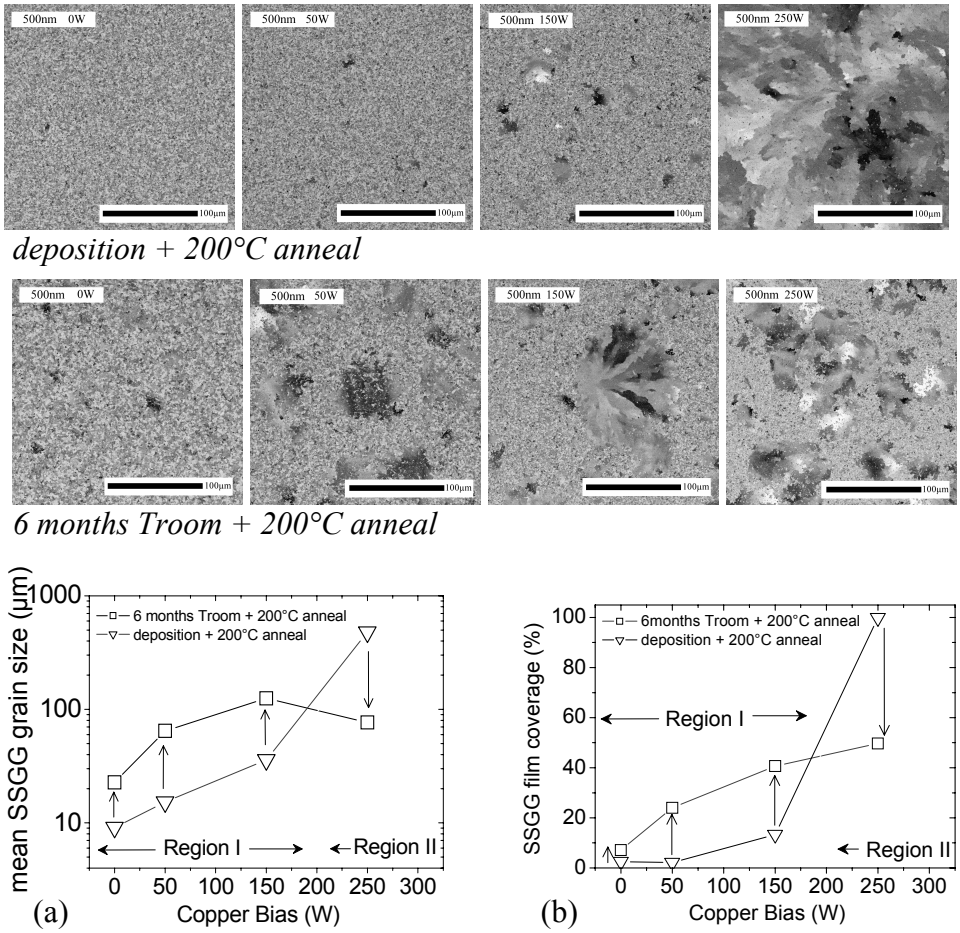
Finally, also the amount of Argon atoms that are built into thin films during film formation can change the rate of grain growth in those films. However, due to the low amount of Ar in the copper films deposited with the self-ionised plasma (SIP) technique, it is unlikely that a significant number of Ar atoms was segregated to the grain boundaries and played a role in the decrease of the grain growth rate. Segregation of a small amount in the film deposited with 250W bias conditions can however not be entirely ruled out. Due to the observed increased self-annealing time for

higher bias conditions, we can distinguish two different regions on figures 4.17a and 4.18b. Region I indicates the copper bias conditions where the SSGG mode is still observed at room temperature within a reasonable time frame and where the mean super grain size clearly increases with increasing bias conditions. For these films, there is also a clear rivalry between the two different observed growth modes (SGG and SSGG), where the SSGG-mode is pronouncedly present at room temperature and drives the system towards a more {100} texture. In case of region II, no SSGG was observed at room temperature within a period of 6 months. Be aware that the "transition" between these two regions is merely indicatively shown as a broad transition area on figures 4.17a and 4.18b. This is mainly due to the lack of data points between 150W and 250W. In fact, one can not actually speak of a real transition, because the SSGG growth velocity gradually decreases with increasing sputter bias instead of abruptly. In any case, the split up between regions with or without room temperature grain growth (within a reasonable time frame) already provides a good and efficient way to describe and understand the observed trends.

4.5.2 Behaviour at elevated temperatures:

Figure 4.20 shows the influence of the copper sputter bias on the final SSGG grain size and film coverage in case of two different annealing conditions: in the first case, a 200°C anneal for 5 hours was carried out just after deposition. Secondly, a 200°C anneal for 5 hours was carried out after 6 months self-annealing at room temperature. As shown from these figures, the mean SSGG grain size and (100) orientation fraction mainly increases with increasing copper bias conditions. This is in agreement with the increased initial film stress observed for higher copper sputter bias conditions (i.e. -122MPa for a 0W, -212MPa for a 50W and -290MPa for a 250W sputtered copper film). The initial film stress values for different copper bias conditions are illustrated in the texture maps on figure 4.21. In these maps both the surface/interface energy density difference $\Delta E_{s,i}$ and strain energy density difference ΔE_{ε} between the two mainly observed orientations, i.e. (111) and (100), are plotted as a function of the film stress. Since the thickness for all sputtered copper films was kept constant at 500nm, the surface/interface energy difference between the (111) and (100) grains is the same for all copper films. Notice however that instead of plotting all initial film stress values in only 1 texture map, we introduce an additional axis (i.e. copper bias). This is because a strong correlation is

found between the as-deposited microstructure/texture and the initial film stress (figure 4.7). For each copper bias condition, the microstructural and textural evolution of the film starts from a different initial microstructure, texture and stress state. Therefore, the impact of the strain energy minimizing driving force is also different. For higher initial film stress values, the impact of the strain energy minimizing driving force increases, thereby favouring the growth of (100) super grains during the post depositional microstructural/textural evolution of the films.



Figures 4.20: influence of the copper bias conditions on (a) the mean SSGG grain size and (b) the SSGG orientation fraction. The samples were given an additional anneal just after deposition (triangles) or after 6 months self-annealing at room temperature (squares).

For copper sputter bias conditions from region I on figure 4.20 (i.e. bias conditions ~0W-150W), the largest SSGG grain sizes and largest (100) orientation fraction can be found when the films are annealed after 6 months self-annealing at room temperature. One of the possible explanations for this trend can be the lower observed SSGG activation energy as compared to the activation energy for SGG (see section 4.4) for these sputter bias conditions. The opposite trend is observed in the case of sputter bias conditions from region II (i.e. ~250W). Remarkably, despite the fact that for these bias conditions no super grains were observed even after 6 months room temperature storage, an additional annealing step lead to an almost complete film coverage with super grains in the order of 500µm in diameter.

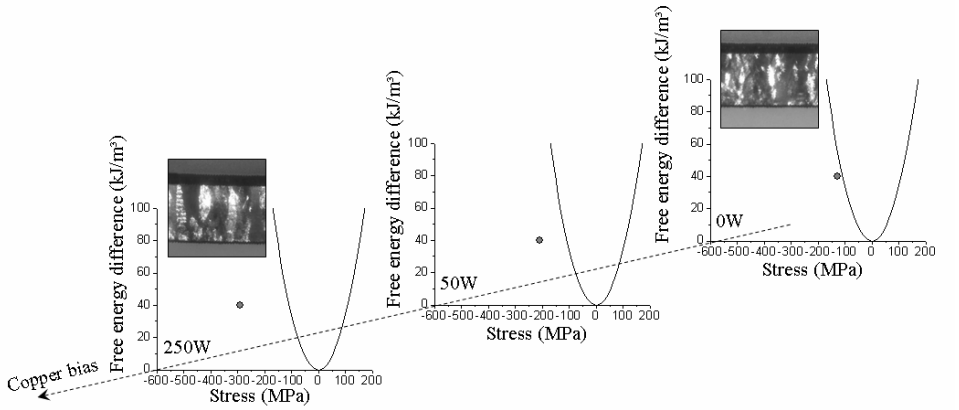


Figure 4.21: texture maps of 500nm thick sputtered copper films using different sputter bias conditions. As shown, there is a strong correlation between the initial film stress and the as-deposited microstructure and texture.

This suggests that in this bias range, the SSGG growth mode is more pronouncedly present at elevated temperatures instead of room temperature. Interestingly, this slightly deviant behaviour of 250W sputtered copper films at room temperature and elevated temperatures also correlates very well with the observed difference in the as-deposited film microstructures and textures of 50W and 250W sputtered copper films (see figure 4.5 and 4.6). For bias conditions from region I (0W-150W), a fine grained as-deposited microstructure with a "low {111}" initial texture is observed and the subsequent super secondary grain growth occurs at

room temperature leading to grain sizes in the order of 50-100µm and an incomplete SSGG film coverage. For bias conditions from region II, the as-deposited microstructure contains more columnar grains with a "high (111)" initial texture. The SSGG growth mode only occurred after a sufficient annealing step, leading to grain size up to 500µm and an almost complete film coverage. In order to further understand the growth dynamics and the observed grain sizes and orientation fractions for sputtered copper films with sputter bias conditions from region II, the activation energy for the SSGG growth mode was determined in case of a 250W sputtered copper film and compared with the value determined for a 50W film. On figure 4.22a, the mean grain diameter evolution during an annealing step at 200°C is illustrated, revealing mean SSGG in-plane growth velocity of 200 ± 30 µm/h. The results for both bias conditions are illustrated in an Arrhenius plot on figure 4.22b.

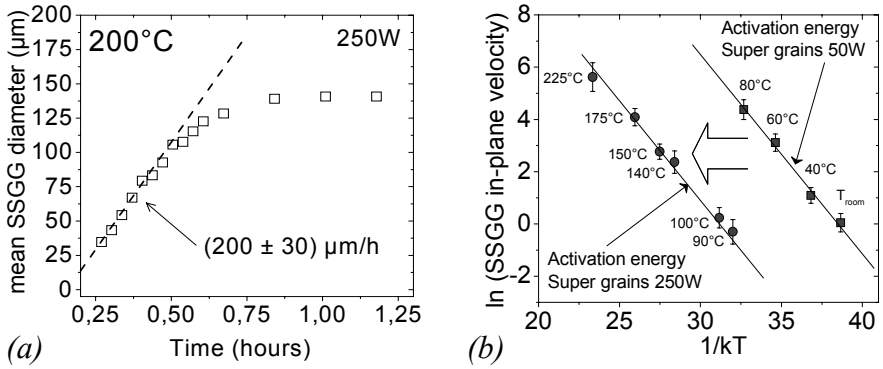
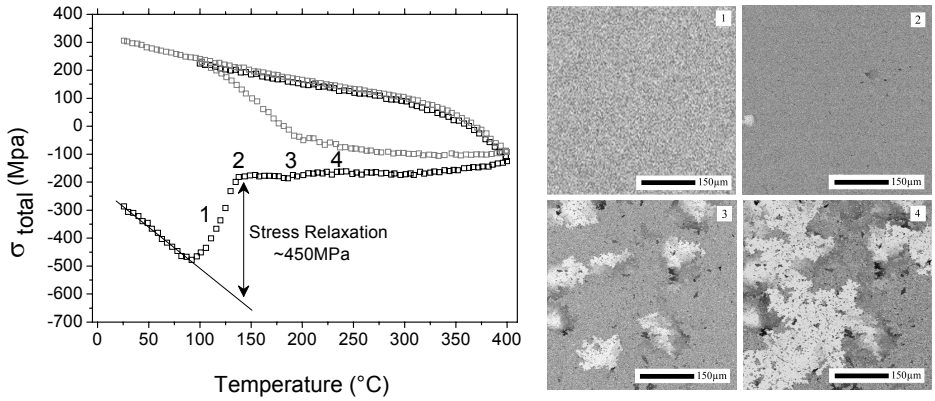


Figure 4.22: (a) grain diameter versus time during an anneal at 200°C of a 500nm thick copper film using 250W sputtering bias conditions. (b) Arrhenius-plot for 50W and a 250W sputtered copper films, determining the activation energy of the super grains. In case of a 50W the activation energy was 0.77eV ± 0,05eV, while in case of a 250W the activation energy was 0.79± 0,05eV.

Notice that the slopes of the curves for a 50W and a 250W sputtered film are comparable, meaning that both systems have the same activation energy for the super grains and thus the in-plane SSGG growth velocity reacts in a similar way to relative temperature changes. This seems plausible, as only the bias conditions were changed while the film thickness (and thus also the available copper volume) remained the same.

However, the curve for a 250W sputtered film is shifted towards the higher temperature area, meaning that although these super grains have the same activation energy as 50W super grains, they are activated at a higher temperature. A possible explanation for this shift in the Arrhenius plot is a decrease in grain boundary motion, which is a consequence of the reduced driving force for grain growth for increasing sputter bias. This in turn has a strong correlation with the as-deposited film microstructure/texture. In order to determine the temperature at which the super grains are activated, and further study the correlation between stress and microstructure in case of a 250W sputtered copper film, in-situ heating experiments were carried out.

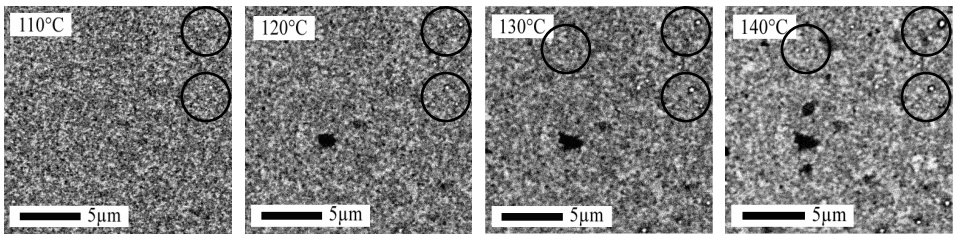


(a) *(b)*

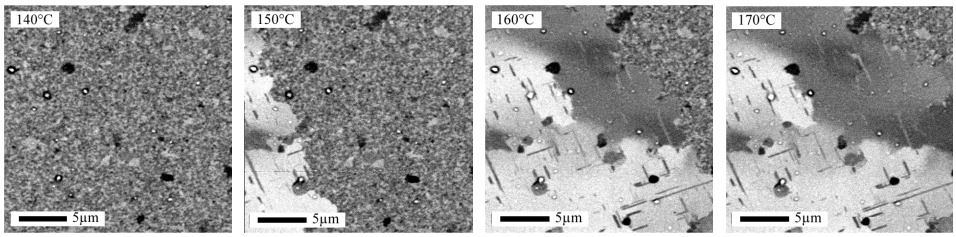
Figure 4.23: (a) thermal cycling experiment just after deposition (1st cycle: black dots; 2nd cycle: grey dots) on a 500nm copper seed layer with 250W copper bias (b) real-time SEM images during the heating of the film using the same temperature profile, and revealing super secondary grain growth.

Figure 4.23 shows the results of a thermal cycling experiment just after deposition of a 500nm copper film using 250W copper bias conditions, and annealing the film at 3°C/minute in 2 heating/cooling cycles up to 400°C. During this thermal cycling experiment, the film stress was monitored using wave curvature measurements. Moreover, in-situ real-time experiments using the same heating profile were performed to reveal the microstructural changes during the thermal cycling. During the 1st cycle, the stress follows the thermoelastic line up to 90°C with a slope of

about –3.0 MPa/°C due to the difference in thermal expansion coefficients of copper and silicon ($\Delta\alpha_{Cu\text{-}Si}$ = 14.1 x 10^{-6}/°C) [31]. No severe microstructural changes were observed during the thermoelastic line up to 90°C, using the simultaneously performed real-time SEM monitoring heating experiments. This results in a value of about 204GPa for the biaxial modulus M. At temperatures above 90°C, a clear deviation of the thermoelastic line is observed, revealing a huge stress relaxation in the order of 450MPa between 90-140°C, followed by a large stress plateau. During this stress plateau, the stress remains nearly constant even though the temperature is increased up to 400°C. This suggests that during this period the stress is continuously relaxed. Notice that no super grains were observed at the copper surface during the large stress relaxation around 90-140°C. Moreover, high temperature X-ray diffraction measurements using the same temperature profile as during the thermal cycling experiment revealed no considerable increase in the (100) texture component before the temperature range 140-150°C. This suggests that the contribution of the onset of SSGG nucleation points in the copper film to the observed large stress relaxation between 90-140°C is negligible, and therefore another mechanism must be responsible for the huge stress relaxation.



(a) hillock formation



(b) super secondary grain growth

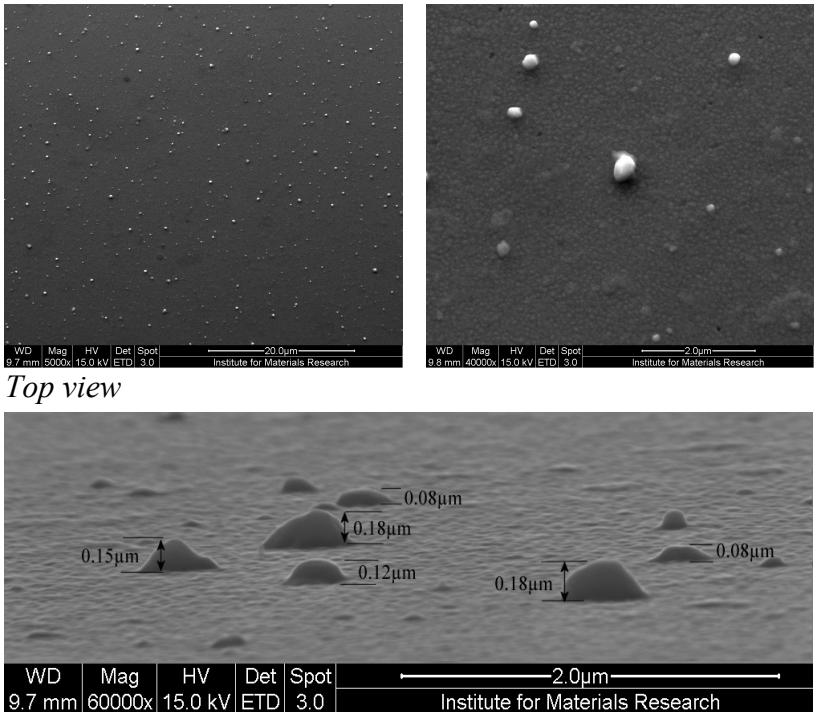
Figure 4.24: real-time top SEM images during a termal cycling experiment, revealing hillock formation. During these experiments, hillocks are first formed (a), then afterwards super grains cover the film surface (b).

The first super grains were only observed for the first time at the copper surface around 140-150°C and continued to grow from this point on eventually covering the whole film. The continuous stress relaxation between 150-400°C agrees very well with the idea of a strain energy density minimizing driving force for the super grains. In order to investigate the origin of this large stress relaxation, several more detailed in-situ SEM heating experiments were carried out in the temperature range between 90-140°C. These experiments revealed the formation of a considerable amount of hillocks at elevated temperatures. These hillocks were only observed at elevated temperatures and not at room temperature. Figure 4.24a shows the backscattered electron images of the in-situ hillock observation, showing the sequence of hillock formation (dotted circles) during the anneal at 3°C/minute. In these real-time experiments, the first hillocks were found around 100-110°C. As the time elapsed during heating, the hillock size increases and ultimately saturates upon annealing at 140°C. No hillock formation was observed after the huge stress relaxation. Using the EBSD technique, no preferential orientation could be linked to the hillocks. Moreover, these experiments also show that the hillock formation always happened before the development of the SSGG growth mode. Once these hillocks are formed, super grains could subsequently surround them and cover the entire film surface as shown on figure 4.24b. It is known from literature that hillock formation can provide a manner for stress relief in thin films [40]. The observation of hillocks in the temperature range 90-140°C suggests that this huge stress relief during the thermal cycling experiments is mainly caused by the formation of hillocks. In order to confirm this statement, we will attempt to estimate the amount of stress relief caused by the formation of hillocks in these films. This stress relief can be approximated by [41]

$$\Delta\sigma = \tfrac{1}{2}\frac{M\, V_{hillock}}{h\, A_{film}} \cong \tfrac{1}{2} M \cdot \left(\frac{A_{hillock}}{A_{film}}\right) \cdot \left(\frac{d_{hillock}}{h}\right) \qquad (4.1)$$

Where M is the biaxial modulus and h the thickness of the film, which in this case is h = 0.5μm. $V_{hillock}$ is the total hillock excess volume in the measured film area A_{film}. The value for the biaxial modulus can be extracted from the slope of the thermoelastic line on figure 4.23, using equations (2.9) and (2.10) and a difference between the thermal expansion coefficients of a copper film and a Silicon substrate of about $\Delta\alpha_{Cu\text{-}Si}$ = 14.1 x 10^{-6}/°C [31]. This results in a value of about 204GPa for the biaxial

modulus M. We can further estimate the total excess hillock volume $V_{hillock}$ as the product of $A_{hillock}$ with $d_{hillock}$, where $A_{hillock}$ is the total observed area of the hillocks and $d_{hillock}$ is the average excess height of the hillocks. The area fraction of hillocks, i.e. $A_{hillock}/ A_{film}$ can be extracted from top view SEM images, while the value for $d_{hillock}$ is estimated at about 0.15μm from side down SEM images (figure 4.25). Using these values, we obtain a stress relief of the total stress due to hillock formation of approximately 355MPa.



Top view

Side view

Figure 4.25: top and side view secondary electron images revealing severe hillock formation in 500nm thick sputtered films after annealing at a constant rate of 3°C/minute to 400°C.

This value is reasonable in view of the total observed stress relief (approximately 450MPa), inferred from the stress measurements during thermal cycling, as shown on figure 4.23. Therefore, we may conclude that hillock formation is most likely responsible for the huge stress relaxation during thermal cycling. After the hillock formation, the SSGG

growth mode is responsible for the observed continuous stress relaxation, thereby preventing a severe stress build-up in these films at elevated temperatures. In order to understand the texture formation during this thermal cycling experiment, we now focus on the position of the initial stress and subsequent stress evolution on a texture map as shown on figure 4.26 during the thermal cycling experiments. Notice that we only restrict to the stress evolution during the 1st heating cycle, since by the end of the first heating cycle, super grains have covered the entire film surface. On figure 4.26, the initial film stress value just after deposition is located far below the threshold stress value of -105MPa for a 500nm copper film (position 1 on figure 4.26). Because the real-time experiments show that relaxation mechanisms like hillock formation (region 2-3) and the SSGG growth mode (region 3-4) only occur in a temperature range above 90°C for these films, the film stress value can be further increased in size before both relaxation mechanisms take place due to the thermal mismatch between the copper film and the silicon substrate, i.e. region 1-2 on figures 4.26a-b (thermoelastic regime).

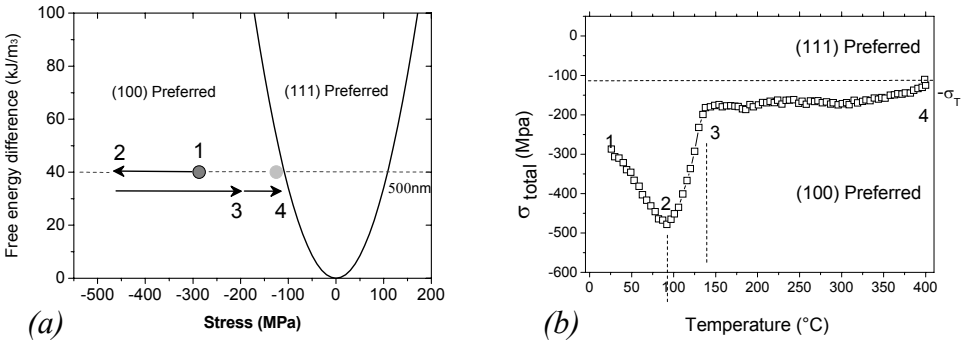
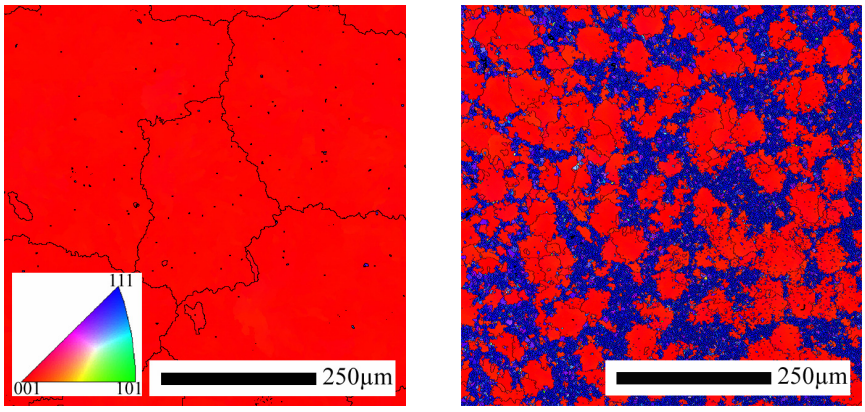


Figure 4.26: (a) difference in surface/interface energy density and strain energy density between (111) and (100) oriented grains and (b) stress evolution in case of a 250W sputtered copper film just after deposition.

In this way, the impact of strain energy minimization on the subsequent textural evolution/film stress relaxation also increases before SSGG occurs (see arrow between positions 1 and 2 on figure 4.26a). This agrees very well with the increased SSGG grain size, compared to films with lower sputter bias conditions (figure 4.20a). During the subsequent stress relaxation that occurs when the temperature is increased (i.e. hillock formation, growth of super grains; regions 2-3 and 3-4 on figures 4.26a-b),

the stress evolves towards a stress plateau at -150MPa. This value is below the critical stress value of -105MPa that defines the difference between surface/interface energy minimization and strain energy density minimization driving forces for textural evolution in this film. The position of this stress plateau is in agreement with the almost full film coverage observed in these films (figure 4.27a). Instead of performing a thermal annealing step just after deposition, the as-deposited copper film can also be stored at room temperature for 6 months and then subsequently annealed. As shown in figure 4.27, a decrease in both grain size and SSGG film coverage was observed. It is found that during 6 months room temperature storage the film stress relaxes towards the tensile stress direction, as observed for all studied copper films of different bias conditions and thickness. Moreover, the temperature at which the SSGG growth mode is activated is found to be around 140-150°C and unchanged after 6 months room temperature storage as demonstrated with high temperature XRD measurements (not shown). Using these two facts, the film stress after 6 months room temperature storage has shifted on the texture map more towards the direction of the region where surface/interface energy minimization is the dominating driving force (see figure 4.26). In this line of thought, this will result in a decreased influence of the strain energy density minimization driving force during a subsequent annealing step and therefore to a decreased final SSGG grain size and (100) orientation fraction as observed shown on figure 4.27.



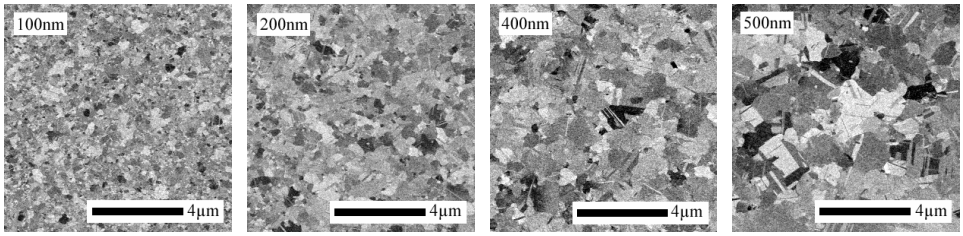
(a) anneal after deposition *(b) anneal after 6 months at T_{room}*

Figure 4.27: EBSD mappings of a 500nm 250W sputtered copper film annealed directly after deposition (a) and after 6 months room temperature storage (b)

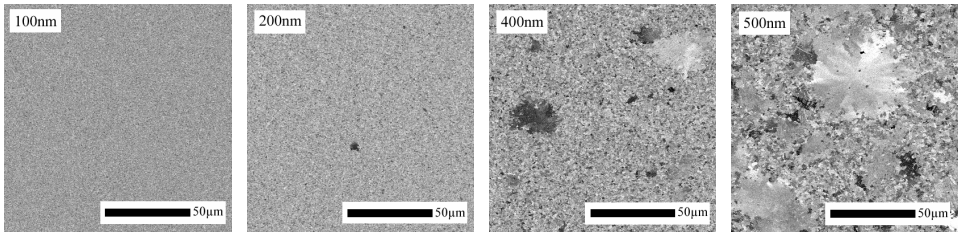
4.6 Influence of the layer thickness on the appearance of Super Secondary Grain Growth in sputtered copper films

In order to investigate the influence of the film thickness on the textural development at room temperature, several copper films of different thickness varying from 100nm to 500nm were deposited onto a 10nm TaN/5nm α-Ta barrier layer and further analysed with the real-time SEM monitoring technique, the EBSD technique and by performing both sheet resistance and stress measurements at different moments in time. Figure 4.28 shows backscattered electron images of respectively a 100nm, 200nm, 400nm and 500nm thick sputtered copper films at low and higher magnifications, revealing the influence of the film thickness on the grain size of the SGG and SSGG growth mode after 3 months self-annealing at room temperature. For both growth modes, the grain size increases with increasing film thickness. Using the EBSD technique, the SGG mean grain size increases linearly with increasing film thickness, while the SSGG mean grain size increases in a nonlinear way with the film thickness. The cumulative grain size distributions for the two observed growth modes (SGG and SSGG) are shown on figure 4.29 for films with different thickness. Notice that in case of the SSGG growth mode no data was shown for thickness below 400nm, due to the decreased grain statistics, i.e. a lower number of detected super grains for thinner films. The linear behaviour of the cumulative grain size distribution plots on figure 4.29 suggest a lognormal grain size distribution for both growth modes and all different layer thickness. Moreover, the median grain size, d_{50}, increases with growing film thickness as indicated, while the lognormal standard deviation, σ, is equal for all film thickness as illustrated by the equal slope of each distribution on figures 4.29. There is also a strong correlation between the increased appearance of the SSGG growth mode in thicker films (figure 4.28b) and the increased (100) orientation fraction for thicker films, as determined with the EBSD technique (figure 4.30a). Due to the strong dependence of the film thickness on the initial film stress (figure 4.30b), the appearance of the SSGG growth mode can also be related to the increased initial compressive film stress. On figure 4.31, this is illustrated in a more appropriate way on a so called texture map. This figure plots the surface/interface and strain energy density difference between (111) and (100) oriented grains as a function of stress in Cu films

of different thickness. Because the difference between the surface/interface energies of (100) and (111) oriented grains is inversely proportional to the film thickness (equation 2.7), the threshold stress which separates (100) preferred growth from (111) preferred growth also varies with the film thickness.



(a) Secondary Grain Growth mode



(b) Super Secondary Grain Growth mode

Figure 4.28: Backscattered electron images for a 100nm, 200nm, 400nm and 500nm sputtered copper film revealing the two different growth modes after 3 month at room temperature.

For Cu films in our study with thickness of 100nm, 200nm and 500nm, this threshold stress is respectively 245, 170 and 105MPa, either compressive or tensile. Both the stress and sheet resistance change during the self-annealing process. As shown on figure 4.31b, the sheet resistance decreases faster for thicker copper films. Notice that even after several months storage at room temperature, the self-anneal of both 100nm and 200nm thick films is still incomplete, while in case of a 500nm thick film the self-anneal is already completed, resulting in a decrease in sheet resistance of about 25%. The variation in film stress over time is consistent with the sheet resistance evolution. Both the stress value before and after self-annealing are respectively indicated on figure 4.31 as dark grey and light grey circles. Apparently there is a continuous (almost linear in time log scale) tensile trend in the copper that is independent of the

initial stress level. However, a rapid relaxation and drop in sheet resistance is observed when the new SSGG mode occurs for the 500nm thick film, hereby driving the initial strong {111} fiber texture to a more {100} fiber texture. This thickness dependence and the appearance of (100) oriented super grains in thicker films can be explained by strain energy density minimization as the energy source for the SSGG growth mode. In case of a 100nm film the initial film stress value of about -21MPa before grain growth occurs is located between the threshold stress values of -245MPa and 245MPa for this specific film thickness.

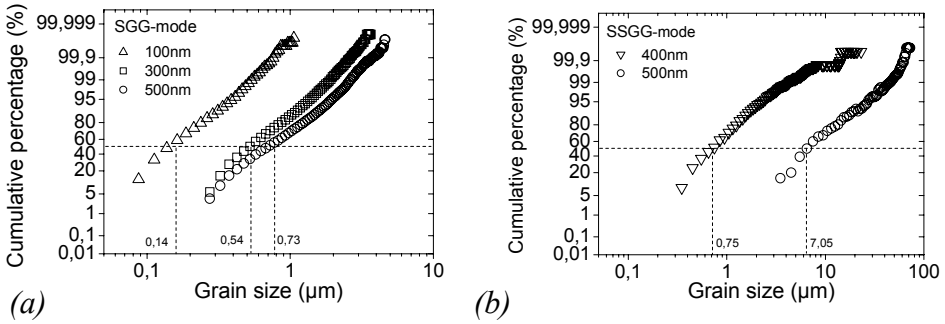


Figure 4.29: The cumulative percentage as a function of the SGG grain size (a) and the SSGG grain size (b).

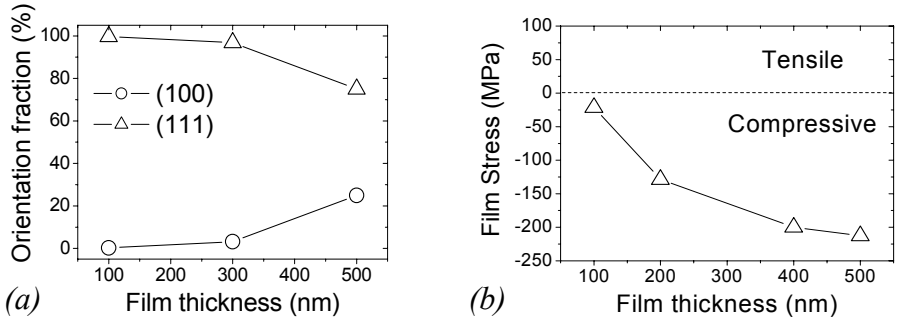


Figure 4.30: (111) and (100) orientation fraction (a) and the initial film stress (b) as a function of the film thickness. The (100) and (111) orientation fractions were determined taking into account all the grains with a misorientation below 15° compared to the ideal (100) and (111) orientations.

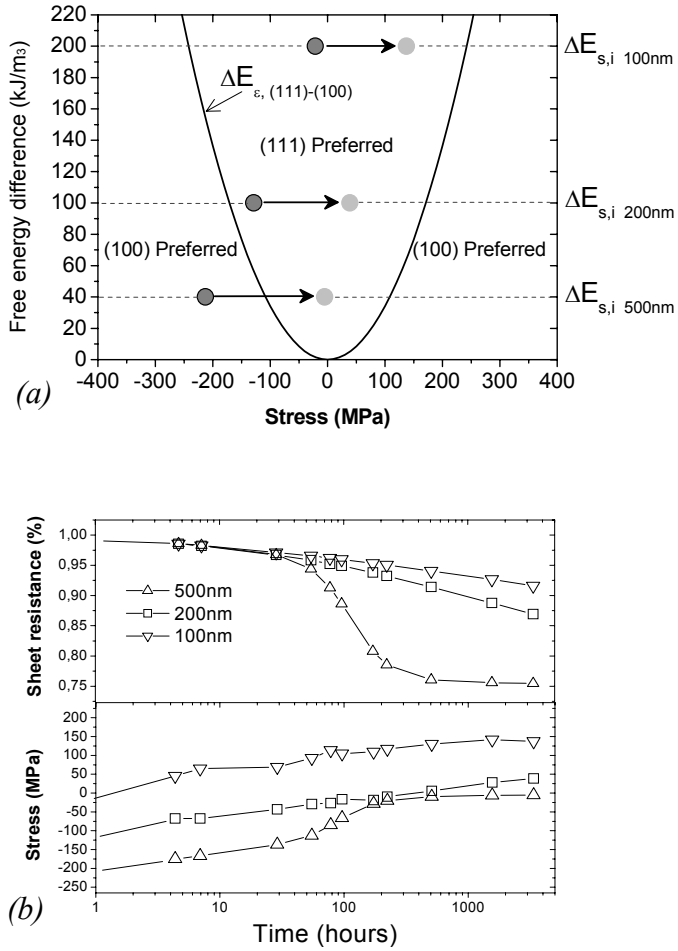


Figure 4.31: (a) difference in surface/interface energy density and strain energy density between (111) and (100) oriented grains. (b) evolution of stress and sheet resistance as a function of time of 3 different film thicknesses.

Therefore, grain growth starts from a strong {111} fiber texture and a situation on the texture map where surface/interface energy minimization is favoured over strain energy density minimization ($\Delta E_{s,i} < \Delta E_{\varepsilon}$). As the final stress value after self-annealing (~ 137MPa) is also located between the two threshold stresses on the texture map, this suggests that the film

textural evolution during the entire self-annealing process was mainly dominated by surface/interface energy minimization. This is in good agreement with an almost 100% observed {111} texture in this film (figure 4.30a). For thicker films, the grain growth also starts from a strong {111} fiber texture, but the initial film stress is more located towards the region where strain energy minimization is favoured over surface/interface energy minimization as driving force for textural evolution ($\Delta E_{s,i} > \Delta E_{\varepsilon}$). This shift towards the region where $\Delta E_{s,i} > \Delta E_{\varepsilon}$ is due to the fact that for thicker films the initial film stress increases and the fact that the interface and surface energy decreases with increasing film thickness, (equation 2.7). If the film thickness is increased from 100nm to 500nm for instance, the energy density available from interface energy minimization is already 5 times lower per unit volume. The location of the initial and final film stress values on the texture map agree very well with the increased (100) fraction and the increased appearance of the SSGG growth mode for thicker copper films. Therefore, we may conclude that the texture of thinner films is more driven by surface/interface energy density minimization, leading to a more {111} texture, while for thicker films, strain energy minimization is more dominant during textural evolution and will therefore lead to a more {100} texture.

4.7 Influence of the barrier composition on the appearance of Super Secondary Grain Growth in sputtered copper films

In the previous sections, we discussed the microstructural evolution in sputtered copper films on a 10nm TaN/5nm α-Ta barrier layer. As discussed in these sections, a new grain growth mode (SSGG-mode) was observed in thick copper films, which lead to a highly concentric growth and to grains of many tens of microns. Moreover, a clear rivalry between this new growth mode and the regularly observed secondary grain growth (SGG-mode) was found. In this section we will further discuss the influence of the barrier composition on the appearance of this new SSGG-mode during the microstructural evolution. Figure 4.32a shows the relative sheet resistance and stress evolution at room temperature of a 500nm 50W sputtered copper film on three different barrier compositions/textures:

15nm β-Ta, 15nm amorphous TaN and a 10nm TaN/5nm α-Ta barrier, as determined with XRD. As shown, there is a clear increase in self-annealing time for other barrier types than the 10nm TaN/5nm α-Ta barrier layer. This difference in self-annealing time is also reflected in the stress evolution and can be correlated to the decreased appearance of the SSGG growth mode on the 15nm TaN and 15nm β-Ta barrier as compared to the α-Ta bi-layer as shown on the EBSD maps on figure 4.33.

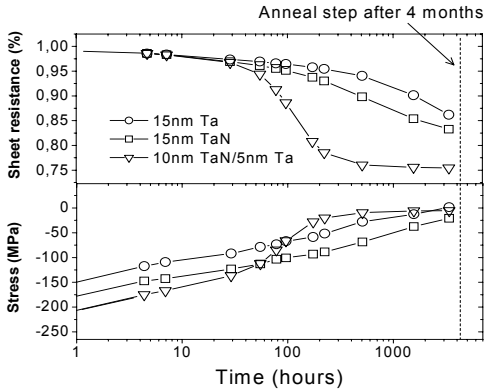
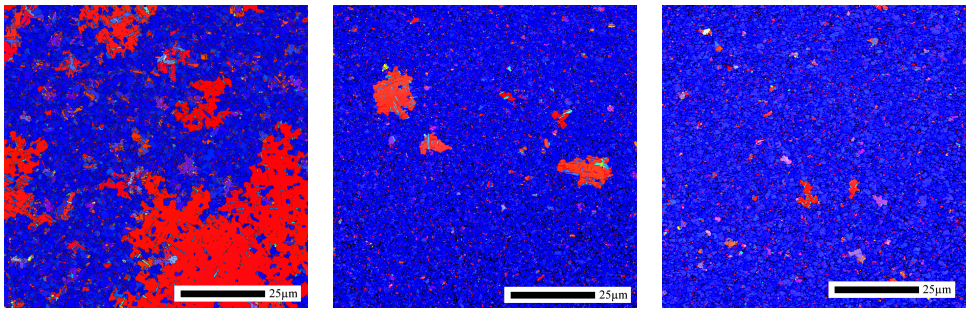


Figure 4.32: normalised sheet resistance and film stress as a function of time for 3 different barrier compositions/textures. After 4 months at room temperature, an annealing step at 200°C for 5 hours was carried out (dotted line) to reveal the final microstructures and textures.

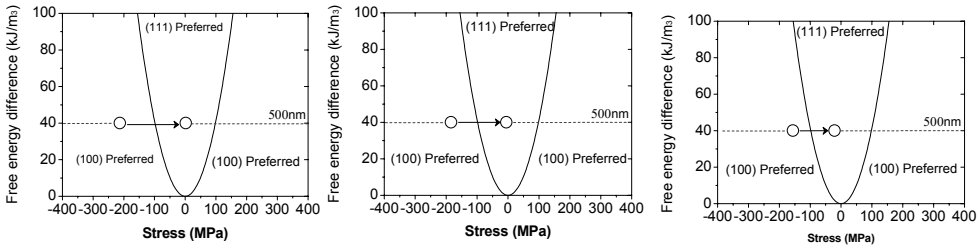
These maps were taken after self-annealing 4 months at room temperature and an additional anneal at 200°C for 5 hours. As shown, a clear decrease in the (100) oriented SSGG-mode is observed for other barrier types than the 10nm TaN/5nm α-Ta. The lowest fraction was found for the copper film where the slowest self-annealing was found, i.e. the copper film on a 15nm β-Ta barrier. This is in good agreement with the position of the initial film stress values for these films on the texture map and the decreased stress relaxation as indicated by the arrows on figure 4.34. This is because the impact of the strain energy density minimizing driving force for the SSGG growth mode increases for higher initial compressive film stress values. Therefore, the films which are in a higher initial film stress state start in a region on the texture map where the strain energy density minimization driving force is more dominant during the

microstructural/textural evolution of those films, as compared to films which are in a lower initial stress state. This will then lead to bigger and more (100) oriented super grains. The decreased number and size of the super grains for other barrier types than the 10nm TaN/5nm α-Ta barriers suggests that the barrier microstructure is instrumental in the nucleation process of abnormal super grains. In case of 250W sputtered copper films on a 10nm TaN/5nm Ta barrier layer, we observed that the super secondary grain growth was dominant at elevated temperatures above 90°C and with grain sizes in the order of 500µm and a nearly full super grain film coverage (see section 4.5).



(a) TaN/Ta (b) TaN (c) Ta

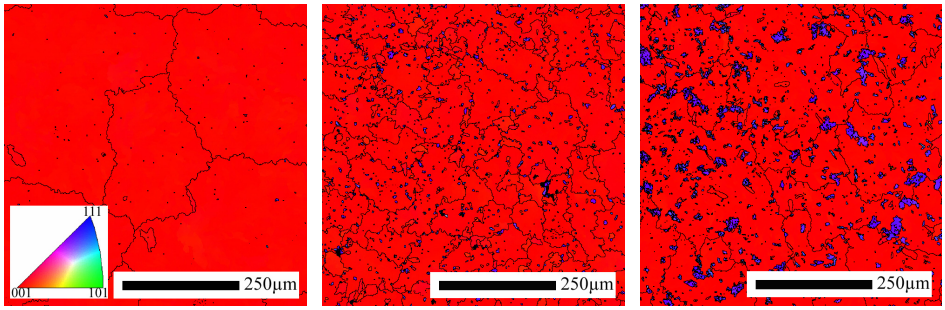
Figure 4.33: top view EBSD measurements of a 500nm 50W sputtered copper film on respectively 10nm TaN/5nm α-Ta barrier layer, amorphous 15nm TaN barrier and 15nm β-Ta barrier.



(a) TaN/Ta (b) TaN (c) Ta

Figure 4.34: difference in surface/interface energy density and strain energy density between (111) and (100) oriented grains for a 500nm 50W sputtered copper film on respectively 10nm TaN/5nm α-Ta barrier layer, amorphous 15nm TaN barrier and 15nm β-Ta barrier

On figure 4.35, top view EBSD maps of a 500nm sputtered copper film on respectively a 10nm TaN/5nm α-Ta, a 15nm TaN and a 15nm β-Ta barrier layer are shown. These maps show that for 250W sputter bias conditions, the super grain film coverage is more or less independent of the barrier composition underneath. This is most likely due to the fact that the film stresses for 250W sputtered films are sufficiently high to almost completely cover these films with (100) oriented super grains driven by strain energy density minimization (see figure 4.35). This can be beneficial for the implementation of these super grains in narrow structures. Notice however that in case of a 15nm TaN and a 15nm β-Ta barrier layer, the SSGG grain size is smaller and a small fraction of the SGG growth mode can still be found (see blue coloured regions on figure 4.35b-c). This suggests that the initial stress in these copper films is lower as compared to copper films on a 10nm TaN/5nm α-Ta barrier.



(a) TaN/Ta (b) TaN (c) Ta

Figure 4.35: top view EBSD measurements of a 500nm 250W sputtered copper film on respectively a 15nm TaN, 15nm Ta, and a 10nm TaN/5nm Ta barrier layer.

4.8 Summary

In this section we discussed the microstructural and textural evolution of sputtered copper thin films during self-annealing at room temperature and at elevated temperatures. The initial microstructure of a 500nm thick as-deposited film has a fine grained microstructure, containing grains with an in-plane grain size in the order of 100nm or less. An number of columnar grains appears in the as-deposited copper films. These columnar grains often contain a lot of twins, which are parallel to the film surface. However, the number of columnar grains in the as-deposited microstructure and their grain size depends on the applied bias voltage during deposition. Moreover, the initial texture could be described as a strong {111} fiber type texture to the film normal direction, with the presence of a weaker {113} texture. For higher sputter bias conditions, the in-plain grain size, the amount of columnar grains and the {111} texture strength of the as-deposited grains increases. These observed trends can be explained in terms of the increased energetic ion bombardment for higher sputter bias conditions (i.e. higher adatom mobilities and resputtering effect). After deposition of films with different thickness and/or different copper bias conditions, the self-annealing behaviour of these films at room temperature and elevated temperatures was discussed. The observed differences in microstructure and texture for different sputter bias conditions lead to a decreased self-annealing time. Possible explanations for this difference in self annealing time can possibly be linked to differences in grain boundary energy and/or defect concentrations. A new growth mode, also called Super Secondary Grain Growth (SSGG), was observed in thick sputtered copper films on different barrier types and using different sputter bias conditions. This new growth mode lead to highly concentric growth and grains of many tens of microns in diameter and drives the system more towards a {100} texture. Moreover, a clear rivalry between this new growth mode and the regularly observed Secondary-Grain-Growth (SGG) mode in sputtered copper films was found. The appearance, growth dynamics and self-annealing time of this growth mode is strongly dependent on the copper sputter bias conditions, copper layer thickness, barrier properties and post-deposition annealing temperature. By increasing the copper sputter bias conditions, a clear increase in self-annealing time at room temperature was observed. This difference in self-annealing time may be explained in terms of the different concentrations of defects and/or differences in grain boundary

energy due to different as-deposited microstructures (grain morphology, grain size, grain boundary types, …) arising from various bias conditions. Thick sputtered copper films using high sputter bias conditions and an annealing step directly after deposition yield the largest grain diameters (up to ~500µm) and the most complete film coverage. In contrast to the low sputter bias initiated super secondary grains, which are more pronouncedly at room temperature, high sputter bias super secondary grain growth is more pronouncedly present at elevated temperatures and leads to even bigger grain sizes (in the order of 500µm) and a nearly full super grain film coverage independent of the barrier composition/texture underneath. Final grain sizes for this new growth mode range from 50µm to 500µm depending on the sputter bias conditions. In case of high bias sputtered copper films, besides the growth of super grains, also an additional stress relief mechanism was observed preceding the growth of super grains. This observed additional stress relief could be explained by hillock formation. All the observed textures in these films were explained in terms of the available driving forces, i.e. strain energy density minimization, surface/interface energy density minimization and grain boundary energy minimization, where strain energy density minimization seems to be an important driving force for the observed SSGG growth mode.

4.9 References of the chapter

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Chapter 5

Introduction of super secondary grains in electroplated copper films and structures

5.1 Introduction

In advanced silicon chip manufacturing, the electroplating technique has found its wide use in copper metallization due to its relatively simple tooling and its capability of filling high aspect ratios in a void-free and seam-free way [1-2] provided that a continuous copper seed layer and diffusion barrier exists in these recessed features. This copper seed layer provides the electrical contact necessary for the initiation of the subsequent electroplating process, while the diffusion barrier is mainly due to reliability considerations. In a modern metallization scheme commonly seen today, both diffusion barrier and copper seed layer are physical vapour deposited, while the void-free filling is realized through the use of proprietary additives in the plating bath [3]. Depending on the electroplating chemistry and the plating conditions, a certain amount of impurities is incorporated into the copper films and features [4]. The use of additives in the electroplating chemistry can also have a great impact on the properties of the deposited copper. For instance, certain additives can result in a reduction of the as-deposited grain size (typically tens of nanometers in size), which leads to the secondary grain growth at room temperature, also known as self-annealing. Moreover, it was found that impurity incorporation retards copper grain growth in electroplated films, thereby resulting in smaller grain sizes and a higher resistivity. This is because during secondary grain growth in those films, the impurities are driven out from the grains which leads to an accumulation at the grain boundaries. When the concentration of the impurities in the moving grain

boundaries has reached a critical value, further grain growth is inhibited. This phenomenon, also referred as pinning, becomes even more complicated in the case of narrow features, as it is very difficult to predict the relative influence of impurity incorporation on grain growth in narrow wires of different width. Even though some data can be found on impurity levels in electroplated films, it has rarely been reported on narrow wires [5]. Finding ways to control the impurity incorporation in narrow features and their influence on the subsequent grain growth remains of great importance. It is however beyond the scope of this thesis to discuss the role of these impurities during grain growth in electroplated films. More information on this can be found in [5-7]. Besides the complicated influence of the impurity concentration, copper grain growth in thin films also suffers from geometrical constraints. In case of narrow copper wires, these restrictions are 2-dimensional (2-D) instead of the 1-dimensional (1-D) restrictions observed in blanket films. These 1-D and 2-D geometric constraints lead to a strong dependence of the copper grain size on the film thickness or wire width/height. As the relative volume fractions of the electroplated copper and sputtered copper (i.e. different ECD/PVD ratio) in narrow features are severely changed when the dimensions of those features are scaled down, this may also have a huge impact on the growth dynamics in those features. Annealing at elevated temperatures can increase the mean copper grain size, due to the desorption of carbon-related and sulphur-related species [4], but the geometric dependence still holds. The copper overburden, which is excessively deposited copper over the trenches and field areas, can partly compensate these geometric confinements and further enhance copper grain growth in narrow wires. It is reported that the grain size in copper wires is much larger if self-anneal or anneal at elevated temperatures is done before the overburden is removed by CMP [8]. This is because the large grains that are formed in the thick overburden can grow into narrow trenches an cause a larger average size there. This enhanced growth from copper overburden only seems to happen in relatively wide interconnects. Up till now, the wire width dependent overburden in-growth remains rather unclear. Therefore, the further enhancement of the impact of the overburden in-growth is of great importance for the achievement of larger grain sizes in nanowires. We already demonstrated in the previous chapter the introduction of a new growth mode in thick sputtered copper blanket (or unpatterned) films. This

new growth mode lead to an improved mean grain size and drove the films more towards a {100} texture. As nowadays, narrow copper wires mainly contain electroplated copper in combination with a thin sputtered copper seed layer, we will focus in this chapter on the introduction of this new growth mode in electroplated copper blanket films and features.

In section 5.2, we investigate if the observed SSGG growth mode in sputtered copper films can also be initiated in electroplated copper films of different thickness. It will be shown that only for thick sputtered copper films in combination with electroplated copper, super grains can grow from the underlying seed layer further into these electroplated copper films. A disadvantage however is the decreased final super grain size for increasing thickness of the electroplated film and the increased self-annealing time for thinner electroplated films at room temperature.

In section 5.3, the knowledge on sputtered and electroplated copper films will be used to increase the mean grain size in patterned structures. In practice, the grain microstructure and texture for two different processing techniques will be compared with the results of the standard deposition process.

5.2 Introduction of super secondary grains in electroplated copper films

As known from the previous chapter, a new growth mode (SSGG) was observed in sputtered copper films, leading to grains of many tens of microns in diameter and drove the system more towards a {100} texture. Moreover, it was shown the amount of super grains was dependent on the used copper sputter bias condition, the applied annealing temperature and annealing time, the film thickness and the texture and composition of the underlying barrier layer. In order to know if these super grains can also be implemented in electroplated copper, 500nm (50W) sputtered blanket films on a 10nm TaN/5nm α-Ta barrier were combined with electroplated copper films of different thickness varying from 200nm to 500nm. For electroplating of these films we have used a commercially available

Electraplate^{TM} chemistry. There are several reasons why we choose a 50W sputter bias condition instead of a higher sputter bias. First of all, this low copper sputter bias is chosen in order to largely exclude the influence of the annealing temperature during the microstructure evolution of both the sputtered and electroplated copper in these films. Despite the fact that the mean grain size of the super grains in the sputtered copper films will decrease for lower sputter bias conditions, the self-annealing time of the sputtered copper will also decrease, thereby enabling us to study the growth of super grains at room temperature (see chapter 4). Secondly, the choice of a 50W copper sputter bias is justified because this is a standard bias used for seed layer deposition in patterned and blanket wafers. As a reference for these films, we deposit a 100nm (50W) thick sputtered seed layer with and without a 500nm electroplated copper layer on top. The main reason for this choice is because no super grains are observed during post-depositional microstructural/textural evolution of a 100nm sputtered copper film (see chapter 4). In this way, the influence of the SSGG growth mode on the self-annealing behaviour of electroplated copper can be investigated.

The microstructural evolution and growth dynamics of all these films was examined using the real-time SEM monitoring technique. Afterwards, the films were given an additional annealing step to reveal the final microstructure of those films. The results of these experiments are shown in figures 5.1a-f. These figures show backscatter electron images during self-annealing, respectively taken at 50, 100, 150 and 200 hours after deposition and reveal a highly concentric growth of super grains in electroplated copper blanket films on a 500nm copper seed layer (figures 5.1b-d). These super grains were observed for all ECD thickness in combination with this seed layer thickness. Notice that the observed growth dynamics is comparable to the SSGG growth mode as observed in the sputtered copper seed layers on α-Ta barriers (figure 5.1a). As shown on figure 5.1e, this SSGG growth mode was not observed in a 100nm sputtered copper film. This concentric growth is rather unusual in ECD copper layers, as the grain growth dynamics is believed to happen rather erratically due to the strong influence of additive concentrations as determined by the plating process [4, 9]. This typically observed erratic growth is illustrated on figure 5.1f, where the microstructure evolution of a 100nm seed layer/500nm ECD combination is shown.

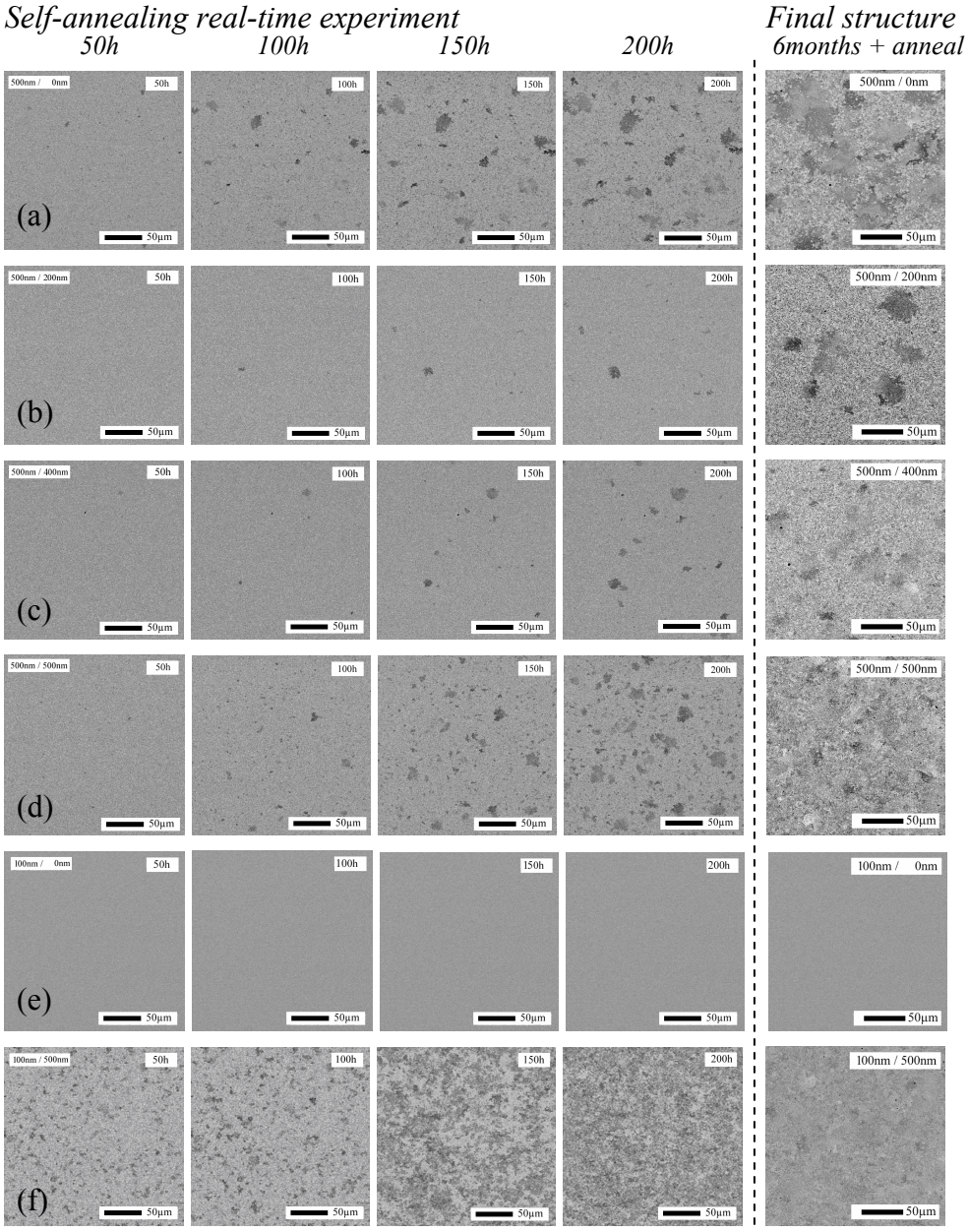


Figure 5.1: backscattered electron images of a 500nm (50W) sputtered copper film with respectively (a) no, (b) 200nm, (c) 400nm and (d) 500nm electroplated copper. As a reference, a 100 / 0 nm (e) and a 100nm / 500nm combination was included (f). These figures were taken from real time experiments, respectively after 50, 100, 150 and 200hours after deposition. After 6 months room temperature storage, all films were annealed at 200°C for 5 hours to obtain the final structures.

For this combination, no concentric super grain growth was observed. Besides the different growth dynamics for the 500nm/ECD combinations compared with the 100nm/500nm combination, also differences in self-annealing times of the electroplated copper (i.e. time where 50% of the copper has self-annealed) can be found from the real-time experiments. As shown on figure 5.2a, which illustrates the grain growth fraction as a function of time, a strong dependence of the self-annealing time of the electroplated copper on its layer thickness can be found. This grain growth fraction was determined from real-time experiments at room temperature. The self-annealing time clearly increases with decreasing layer thickness of the electroplated copper film (i.e. decreasing ECD/PVD ratio). This trend is extensively reported in literature [4, 10-11]. It is shown that these observations are mainly due to a change in nucleation sites per unit area with increasing layer thickness as these sites are proportional to layer volume [10-11]. The use of the term "nucleation" here is somewhat ambiguous as it is used to indicate the onset of growth for a secondary grain. Remarkably, this trend does not hold anymore when no ECD is deposited on a 500nm sputtered seed layer (i.e. for zero ECD/PVD ratio). In this case, the self-annealing time is smaller compared to all the other 500nm/ECD combinations. Only when a sufficiently high ECD/PVD ratio is reached, the self-annealing time can decrease to values below those for sputtered copper films. In case of a 500nm seed layer, the ECD/PVD ratio should be at least above 1, as illustrated on figure 5.2b. A possible explanation for this rather deviant behaviour might be attributed to the number of impurities that is incorporated in a electroplated copper film and the important role that these impurities play during self-annealing in electroplated copper films, as compared to sputtered copper films. Be aware that the values for the grain growth fraction shown on figure 5.2 are only valid for a 500nm seed layer in combination with electroplated copper films of different thickness. For other seed layer thicknesses in combination with the same set of electroplated copper films similar trends were observed (i.e. increased self-annealing time with increasing ECD thickness). However, despite the fact that some of these films may have the same ECD/PVD ratio (for instance a 500nm seed layer combined with 500nm ECD, compared with a 100nm seed layer combined with 100nm ECD copper), this does not always necessarily lead to the same self-annealing time or grain growth fraction. Therefore, it is impossible to

generalize the data for all seed layer thickness and all ECD/PVD ratio's into 1 curve. This emphasizes that the self-annealing behaviour of the PVD/ECD bi-layered system is very complex and more experiments are needed to get a better comprehension of the self-annealing behaviour in those films. This is however beyond the scope of this work. In this work, we will only restrict to the influence of the ECD copper on evolution of the SSGG growth mode.

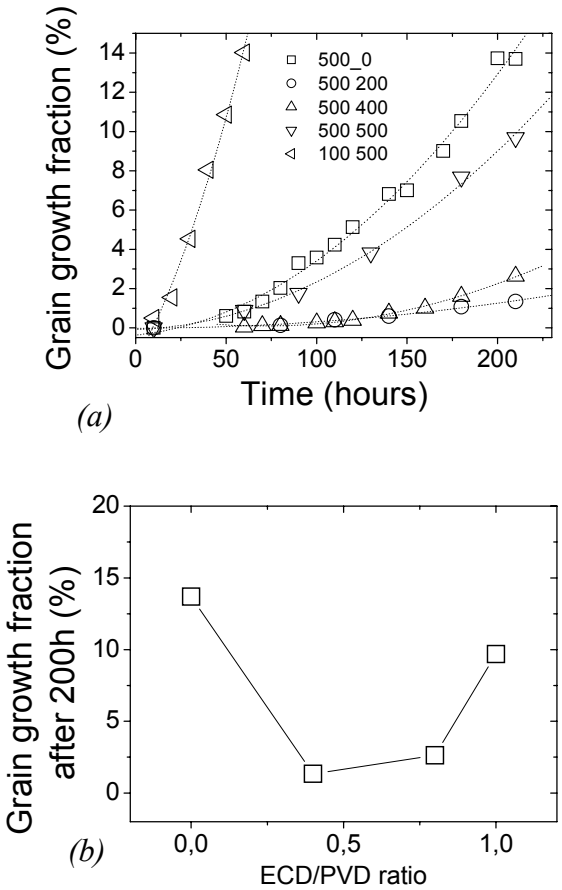
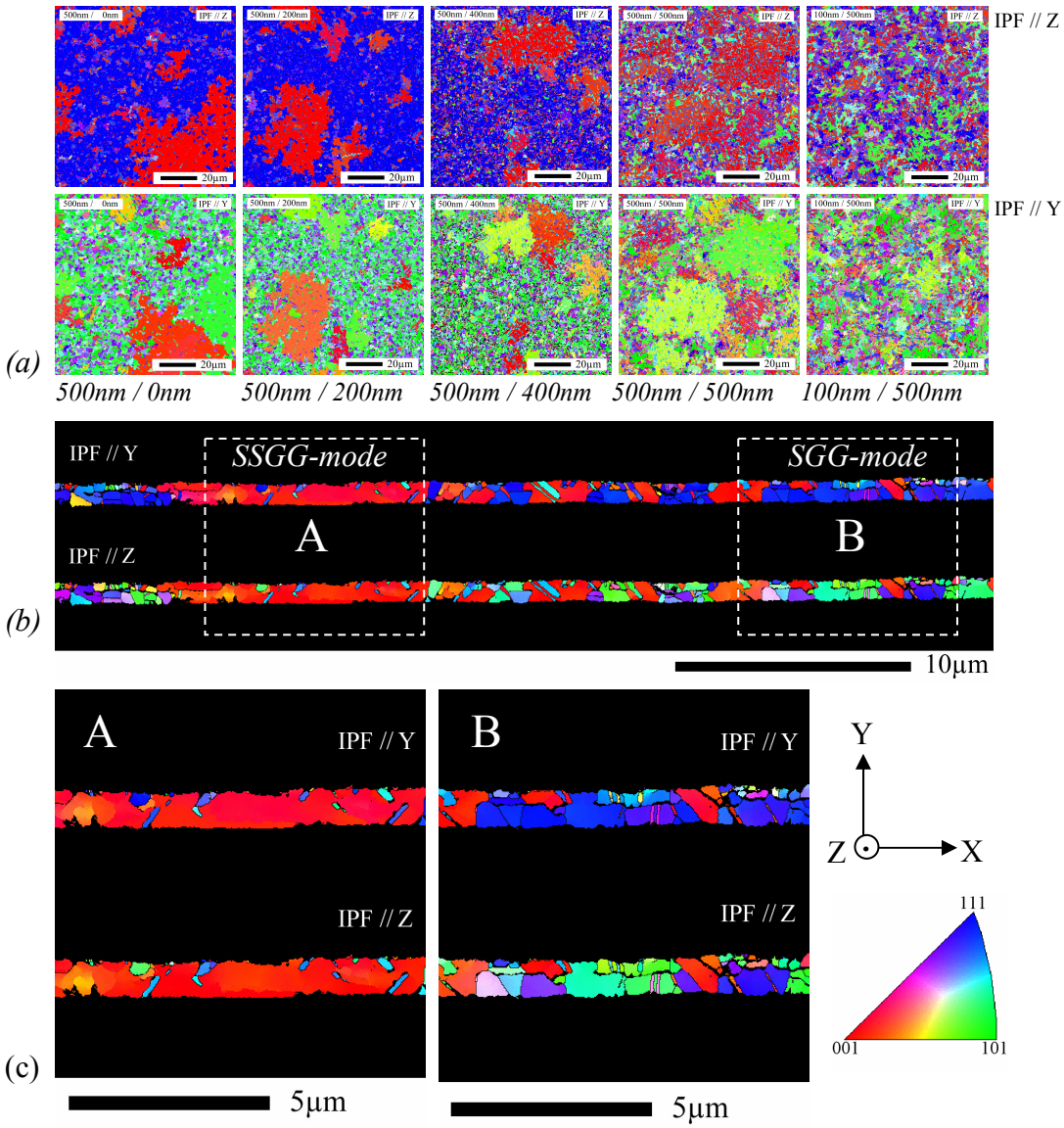


Figure 5.2: (a) grain growth copper fraction after 200 hours, as a function of time for a 500nm copper seed layer combined with ECD copper films of different thickness. (b) grain growth fraction as a function of the ECD/PVD ratio in case of a 500nm thick copper seed layer.



Figures 5.3: (a) top view EBSD IPF // Z and IPF // Y maps of the final texture of a 500nm thick sputtered copper films on a 10nm TaN/5nm α-Ta barrier, combined with or without an electroplated copper film of different thickness. (b) cross sectional EBSD IPF // Y and IPF // Z maps of a 500nm/400nm PVD/ECD combination. (c) Regions A (SSGG-mode) and B (SGG-mode) at higher magnifications.

As can be seen on figures 5.1, the unusual concentric growth behaviour observed during the self-annealing of 500nm/ECD combinations in contrast to the rather erratic growth dynamics observed in a 100nm/500nm combination can be explained assuming that the super grains observed in the electroplated copper are in fact super secondary grains which are initiated in the thick 500nm underlying sputtered seed layer (see chapter 4) and then subsequently grow further throughout the ECD layer. This is in agreement with the presence of super grains in the 500nm / ECD combinations and the absence of super grains in both the 100nm sputtered film and the 100nm / 500nm PVD / ECD combination. In order to further confirm this hypothesis, both top view and cross sectional EBSD measurements are essential.

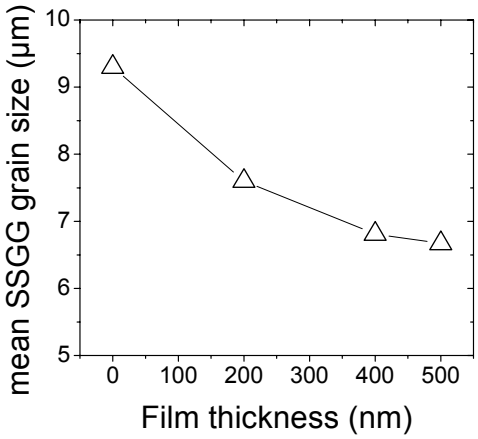


Figure 5.4: mean SSGG grain size as a function of the ECD film thickness on top of a 500nm sputtered copper seed layer

On figures 5.3a, top view EBSD maps (IPF // Z and IPF // Y) of a 500nm thick sputtered copper film on a 10nm TaN/5nm α-Ta barrier combined with or without an electroplated copper film of different thickness are shown. These figures show that the super grains observed in the electroplated copper films during real-time experiments are all (100) oriented (IPF // Z maps), which is in agreement with the orientation of the super secondary grain growth mode observed in sputtered copper films

without electroplated copper on top. From the top view EBSD maps (IPF // Y and IPF // Z) maps the fiber texture nature of these super grains is illustrated. In case of a 100nm / 0nm and 100nm/500nm combination, no super grains could be detected. As shown on the cross sectional EBSD mapping of a 500nm/400nm combination on figures 5.3b-c, the (100) oriented super grains (SSGG-mode; see region A on figures 5.3b-c) are all columnar and span the entire film thickness, while a clear boundary between the sputtered and electroplated copper can still be found in the regions along those super grains (see region B on figures 5.3b-c). This therefore suggests that the super grains are most likely initiated in the underlying sputtered seed layer and then have further grown throughout the ECD layer. As illustrated on figure 5.4, the final mean SSGG grain size decreases with increasing electroplated film thickness. This may be explained by the observed decrease in self-annealing time for thicker ECD copper films, as shown on figure 5.2. In this way, grain growth in thicker electroplated copper films can start at more places during self-annealing, thereby increasing the chance that the super grains are blocked by energetically unfavourable material as they grow throughout the electroplated copper. This decrease in mean SSGG grain size for thicker electroplated copper films indicates that despite the fact that super grains can be initiated in electroplated copper, there is still a clear restriction to the final SSGG grain size. Nevertheless, the implementation of these super grains in ECD copper films is already an important breakthrough and an essential step forward towards the introduction of these super grains in narrow features.

5.3 Implementation of super secondary grains in structures using two different processing techniques

In this section, we will only focus on enhancing the grain size and impact of the overburden, by introducing super grains in the overburden using all the knowledge on blanket wafer level of the previous sections and chapters. In this way we will try to increase the average grain size in features. In practice, we will investigate and evaluate two different

processing techniques and compare the grain microstructure and texture in features of different line widths, with those of a standard deposition process. The two different analysed deposition techniques, together with the standard deposition process are schematically illustrated on figure 5.5a-c. For all three deposition processes, all samples are produced on 200 mm Si(100) wafers with standard layers of 500 nm SiO_2 and 50 nm Si_3N_4. Moreover, the same mask set was used to etch the recessed features in the dielectric layer, so that the microstructure/texture of the same recessed features can be compared.

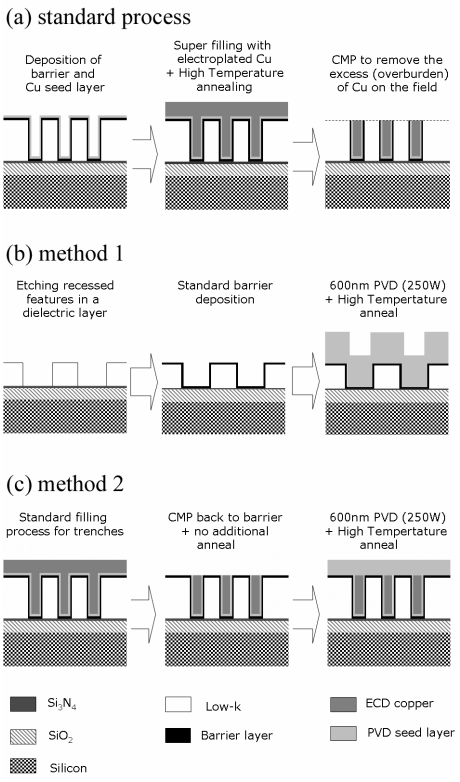


Figure 5.5: schematic overview of the standard deposition process for patterned wafers (a), together with two different alternative deposition processes (b and c) to implement super secondary grains in features.

In case of the standard process (figure 5.5a), this is then followed by SIP (Self Ionised Plasma) deposition of a 10nm TaN/5nm Ta barrier layer and a 70nm Cu seed layer. Typical barrier/seed layer thickness depends on the technology. For the 65nm node typically a 5nm TaN/10nm α-Ta (+ resputter step) barrier layer is used, instead of the 10nm TaN/5nm α-Ta barrier we use. However, in order to maintain consistency with the results on blanket wafers we use the 10nm TaN/5nm α-Ta instead of the standard barrier used nowadays. The standard bias condition used during deposition of barrier layers is 50W, while for seed layer this is 100W. This seed layer is then contacted electrically from the wafer edge for electroplating the copper layer of interest. For electroplating we have used a commercially available Electraplate^{TM} chemistry.

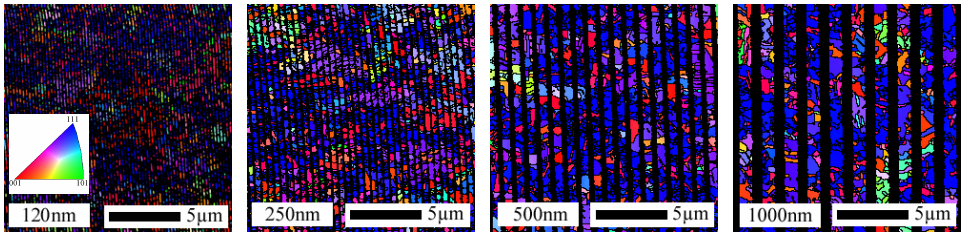


Figure 5.6: EBSD mappings revealing the texture with respect to the film normal (Z-direction) as a function of line widths, in case of the standard deposition process.

The electroplating is followed by an annealing step at 200°C for 30 seconds. Finally, the wafer is chemically mechanically polished (CMP) in order to remove the excess of copper and planarize the field. On figure 5.6, EBSD maps are shown, revealing the texture (with respect to the film normal direction) as a function of the line width varying from 120nm up to 1µm. These maps show that a clear difference in texture can be found for narrower lines. This is more clearly shown on figure 5.7. This figure shows the orientation fraction of the (111), (110) and (100) and random oriented grains, where all the grains were taken into account with a deviation less or equal than 15° from the ideal (111), (110) or (100) orientation. Deviations above this critical deviation angle are considered as random orientation. One can see that (111) fraction decreases from

around 50% for wide lines to about 25% for narrower lines. In literature, the grain orientation on Ta-based barriers exhibit a strong {111} texture and smaller grains are expected in smaller lines [12]. On figure 5.7b, one can see the relative {111} texture decreases in strength with decreasing line width. This observed trend can mainly be attributed to the increased influence of the sidewalls in narrower trenches. In case of wider lines the low {111} surface-free energy dominates the texture formation and therefore results in a preferred strong {111} texture. However with the height to width ratio increasing, the interface energy associated with the sidewalls can become a dominant in structure evolution [13-15].

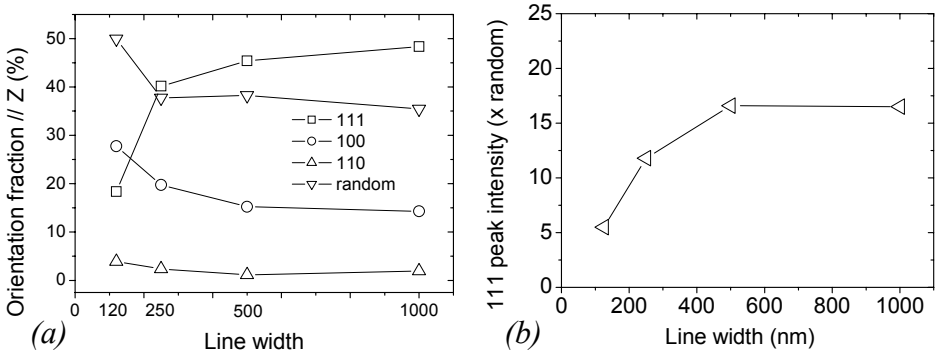
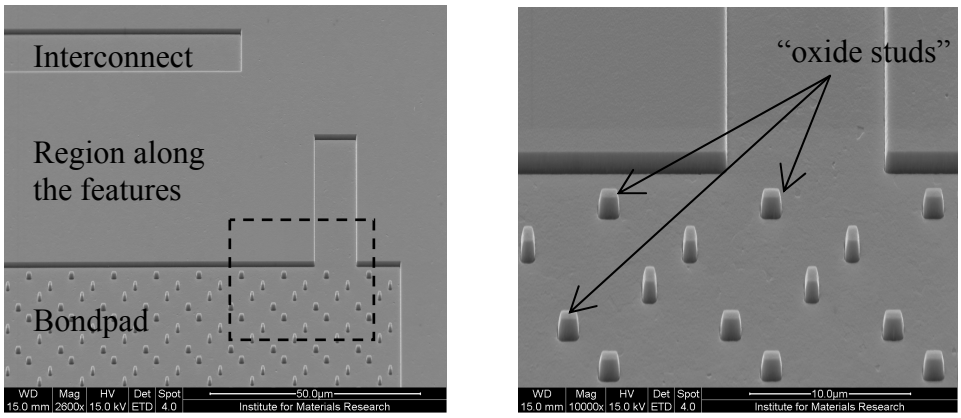


Figure 5.7: (a) evaluation of different orientations observed – (111), (110), (100) and random oriented grains – in studied Cu lines. (b) 111 peak intensity of Cu inside Cu wires of different width showing {111} texture decreasing with decreasing line width.

In a first alternative method (figure 5.5b), a standard barrier layer is deposited in the trenches and other regions in a similar way as was done for the standard process. Instead of filling the trenches with a thin copper seed layer and electroplated copper, all the trenches as well as the regions in between the trenches are filled with a 600nm thick copper sputtered seed layer and using a 250W copper sputter bias condition. After deposition, an annealing step at 200°C for several hours was carried out (see figure 5.5b). As mentioned in the previous chapter 4, in case of thick 250W sputtered copper films, super grains up to ~ 500µm in diameter, which cover almost the whole film surface, are observed after an

annealing step at elevated temperatures. Therefore, the objective of this method is to see if those super grain can still be initiated in the large regions along the features, and if so whether these super grains can grow further on top and into those features or not. Notice that in order to prevent void formation in the trenches during deposition, only the very wide and shallow trenches will be considered during the characterization. This is because for very narrow features, the I-PVD technique is not able to fill those small features in a defect-free and seamless way, and therefore these features are not relevant from industrial and scientific perspective.

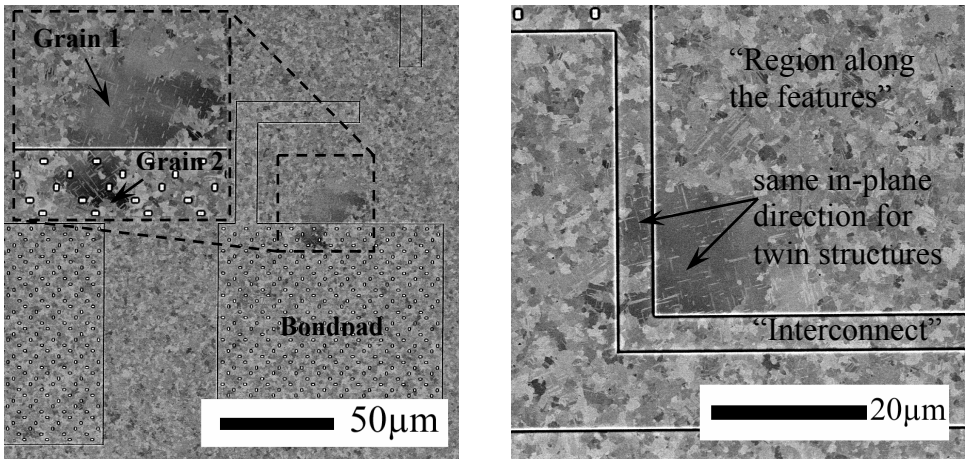


(a) *(b)*

Figure 5.8: (a) SEM image of a bondpad filled with a 600nm (250W) sputtered seed layer, and tilted at 70° (b) Further magnification of the dotted area on figure 5.8a, revealing the so called "oxide studs" present in the bond path (see arrows).

In any case, if super grains can be initiated in wide sputtered copper wires, this can already provide lots of important information on the electromigration behaviour as a function of orientation and the contribution of grain boundary scattering to the resistivity of copper in features. One of the disadvantages of this method is the fact that this method doesn't solve the problem with the hillock formation after the anneal step, as observed in thick copper films using the 250W sputter bias conditions. This can be solved afterwards by an additional CMP step.

Figures 5.8a-b shows the tilted surface of a bondpad, an interconnect and the region along the features, filled with a 600nm sputtered seed layer using 250W sputter bias conditions and after an annealing step at 200°C for several hours. The topographical differences between the features, bondpads and the region in between the features is illustrated on both images, as well as on the schematic overview on figure 5.5b.

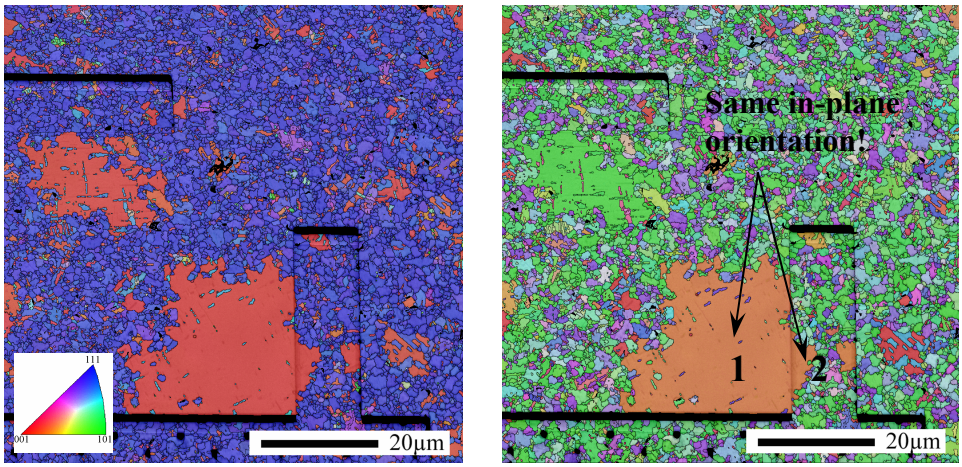


(a) *(b)*

Figure 5.9: backscattered electron SEM images of two different regions on a patterned wafer deposited using method 1.

Moreover, the bondpads contained so called "oxide studs". These rectangular features that can be found in large copper areas are meant to reduce copper dishing that occurs during the polishing of very wide structures, thereby improving the uniformity of the polished copper across the feature and wafer. Figures 5.9a-b show SEM images of two different regions on a patterned wafer deposited using method 1. These images reveal that super grains can be initiated in the regions along the features (grain 1 on figure 5.9a) and bondpads (grain 2 on figure 5.9a). However, in most cases these super grains cannot grow further down into the features (figure 5.9a), due to the difference in height between the copper in the interconnects/bondpads and the region along the features. Only in some isolated cases, some super grains overcome this height difference as

illustrated in figure 5.9b. As can be seen on this figure the twin structures inside the super grain in the region along the feature have the same in-plane direction as those inside the interconnect. The in-growth of super grains can more clearly be illustrated when looking to the EBSD maps in figures 510a-b. The red colour on figure 5.10a correspond to the SSGG growth mode, while the blue colour corresponds to the SGG growth mode.



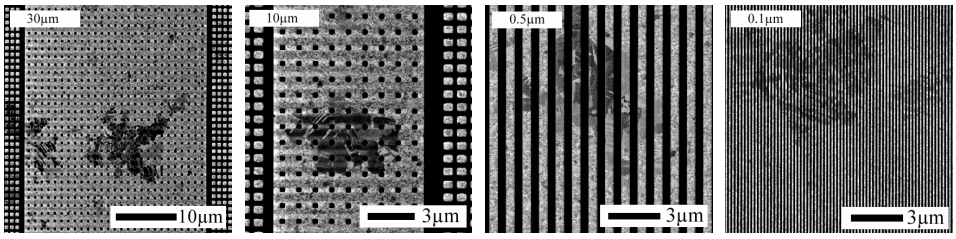
(a) IPF // Z *(b) IPF // Y*

Figure 5.10: EBSD mapping of the same region as shown in figure 5.8. (a) reveals the orientation with respect to the film normal direction. (b) shows the orientation with respect to the in-plane Y-direction The colours correspond to the colour map shown on figure 5.10a.

As shown on the IPF // Y map, the super grain has grown into the structure. This can be derived from the fact that the part from the super grain in the interconnect has the same in-plane orientation as the part in the region along the interconnect (region 1 and 2 on figure 5.10b). Remarkably, almost no super grains were initiated in bondpads even though these areas are quite large. A possible explanation can be the presence of so called “oxide studs” in these bondpads, as illustrated in figures 5.8a-b. The presence of these “oxide studs” can put a restriction on the initiation and further growth of super grains in these regions. This is mainly because their position inside these bondpads may probably change

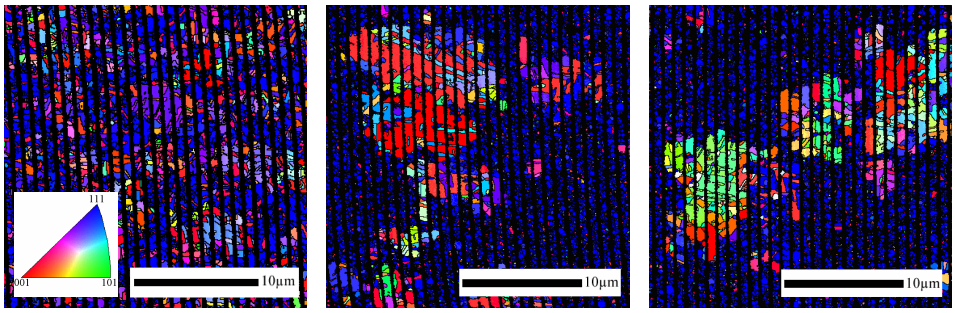
the local stress, thereby also changing the driving force for the super grains. Moreover, even when super grains are initiated in these regions, the large number of "oxide studs' may hamper further growth of these grains, thereby decreasing their final grain size. In conclusion, this method does not really serve as a good alternative deposition method for the implementation of super grains in features.

A second method is illustrated on figure 5.5c. For this method, all the trenches were filled using a standard filling process with a standard Electraplate^{TM} plating bath composition as used for the standard deposition process (figure 5.5a), followed by a chemically mechanically polishing (CMP) step back to the barrier layer and a subsequent barrier cleaning step. In a final step, a 600nm copper film is sputtered on top of the structures, using 250W sputter bias conditions. Finally a standard high temperature anneal at 200°C for 30 seconds is used, followed by a final CMP step to planarize the wafer surface. Be aware that no annealing step was used before and after the CMP step subsequent to the standard filling process. This was done to prevent self-annealing of the electroplated copper deposited in the trenches. The objective of this method is to initiate super grains in the 600nm 250W sputtered overburden and investigate the possible in-growth of super secondary grains in the structures. The results will be compared with the standard deposition/annealing process. For the latter, the trenches are filled using the same standard filling process and Electraplate^{TM} plating bath composition as used for method 2. After deposition, the wafers were annealed at 200°C for 30 seconds, followed by a CMP step to planarize the wafer surface. Figures 5.11 show the results using a final standard anneal at 200°C for 30 seconds.



Figures 5.11: backscatter electron SEM images revealing super secondary grain growth initiation in structures with line widths varying from 30µm down to 0.1µm.

These figures reveal some SSGG in-growth in line widths ranging from 30µm down to 100nm. However, as can be seen the in-growth of these super grains in those structures is still insufficient, as the grain size varies around 10µm and they do not cover the entire structure but merely a limited area fraction. This can most likely be ascribed to either the limited annealing time of only 30 seconds (in chapter 4, we showed that the super grain in-plane growth velocity at 200°C was around 200µm/hour) and/or a different stress state of the sputtered overburden as compared to blanket sputtered copper films. A reduced stress level in the overburden can lead to a reduced appearance of the SSGG growth mode in the copper features since the SSGG growth mode is a stress driven growth mode. Figure 5.12 shows three EBSD maps on 400nm wide lines in case of standard processing with a standard annealing at 200°C for 30 seconds (figure 5.12a), and using method 2 with the same standard annealing step at 200°C for 30 seconds (see figures 5.12b-c). These EBSD maps show the orientation with respect to the film normal direction (Z-direction). When comparing these EBSD maps, one can conclude that for method 2, the in-growth of super secondary grains can be observed in 400nm wide lines, while for the standard annealing process, no super grains could be detected. However, a variety of orientations for the observed super grains can be found, as illustrated in figure 5.12b-c. Not all super grains seem to have the (100) orientation. There can be several possible explanations for this variety of orientations.



(a) *(b)* *(c)*

Figure 5.12: EBSD maps of 400nm wide lines after a standard deposition process and anneal (a) and using method 2 (b-c). As shown super grains can be observed in these structures when using method 2. however, there is a variety of super grain orientations when comparing (b) and (c).

One possible explanation for this variety of orientations is that the stress state of the electroplated copper inside the trenches can be quite different to the film stress state of the sputtered overburden before and during the annealing step. It is plausible that this different stress state can change the orientations of the super grains growing inside the trenches, as in literature there are some articles which suggest that some orientations in structures are favoured during annealing depending on the actual stress state inside the interconnect [16]. Another possibility is that the delay time between the removal of the electroplated overburden and the PVD deposition (see method 2 on figure 5.5) is not short enough as compared to the self-annealing time of the electroplated copper. This could then possibly lead to the in-growth of several copper grains from the electroplated overburden into the interconnect structures. Further optimization of both SSGG grain size and film coverage in these structures is necessary. This can be achieved by increasing the annealing time and by further decreasing the delay between the different processing steps. This is however beyond the scope of this work.

5.4 Summary

We showed that by combining thick sputtered copper films with electroplated copper films of different thickness, the SSGG growth mode could also be introduced in these electroplated copper films. Here, the super grains grew from the underlying seed layer throughout the entire film thickness. It should however be noticed that both the final super grain size and self-annealing time are decreased for increasing thickness of the electroplated film. Using this knowledge on blanket wafer level, and by slightly modifying the standard deposition process, it was further shown that the SSGG growth mode could also be introduced in narrow features. These first results were already very promising. However, further enhancement of the impact of the overburden in-growth is still necessary in order to achieve the expected super grains with the desired textures in copper lines. This will further help to increase the mean grain size in those features, thereby rendering us to find a solution to reduce the resistivity of copper narrow lines and the subsequent interconnect RC delay.

5.5 References of the chapter

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Chapter 6

Conclusions and perspectives

This thesis discusses the introduction of super grains in both sputtered and electroplated copper films and the implementation of these grains in copper interconnects, whose dimensions vary from the micrometer regime to the nanometer regime. The final chapter summarizes the major results of this research and provides some perspectives for future work.

6.1 General conclusions

Nowadays, a clear increase in the resistivity of copper interconnect wires is observed for scaled wire geometries. This increase embodies several scattering mechanisms such as surface and grain boundary scattering which contribute to the classic electron-phonon scattering in bulk materials. Finding ways to increase the mean grain size and thereby decreasing the contribution of grain boundary scattering remains an important research topic. In this work, an extraordinary increased mean grain size was observed in both sputtered and electroplated copper blanket films, depending on the specific choice of layer thickness, deposition conditions and annealing temperature. This knowledge was further used to implement these super grains in copper features, thereby rendering us a solution to reduce the resistivity of copper nanowires and the subsequent interconnect RC delay for future technology nodes. The major results of this work are listed in the following categories.

6.2 Super Secondary Grain Growth in sputtered blanket copper films

In chapter 4 the microstructural evolution of sputtered thin films at room temperature and elevated temperatures is studied. For this study, the influence of different parameters like the film thickness, the copper sputter

bias conditions and the annealing temperature on the microstructural and textural evolution are investigated.

The initial microstructure of a 500nm thick as-deposited film has a fine grained microstructure, containing grains with an in-plane grain size in the order of 100nm or less. An number of columnar grains appears in the as-deposited copper films. These columnar grains often contain a lot of twins, which lie parallel to the film surface. Moreover, the initial film texture can be described as a strong {111} fiber texture along the film normal. Besides the predominant {111} fiber texture, also a weaker {113} texture along the film normal is observed in those films. For higher sputter bias conditions, the film stress, in-plain grain size, the number of columnar grains and the {111} texture strength of the as-deposited grains increases. A strong correlation between this difference in initial microstructure/texture and the post depositional microstructure/texture evolution at low and elevated temperatures was found.

During self-annealing of these films, a new concentric growth mode was found in thick copper seed layers deposited on α-Ta barriers, called Super Secondary Grain Growth (SSGG). This new growth mode is different in both final grain size and growth dynamics, compared to the normal Secondary Grain Growth mode (SGG) observed in most sputtered seed layers nowadays. A clear rivalry between these two growth modes is observed at room temperature and elevated temperatures, thereby changing the mean grain size and proportions of orientation fractions for both growth modes. Moreover, the final mean SSGG grain size and self-annealing time of those films strongly depends on the copper seed layer thickness, the annealing time and temperature, sputter bias conditions and barrier composition/texture.

It was shown that the SSGG growth mode was only observed for thicker copper films and that the copper sputter bias conditions have a clear influence on the self-annealing time of the super grains at room temperature. Higher sputter bias conditions lead to an increased self-annealing time. There are several possible explanations for the observed difference in self-annealing time. One of the possibilities is that this difference in self-annealing time may be linked to a difference in grain boundary energy, which arises from the difference in the as-deposited grain size for different sputter bias conditions. Another explanation may be due to different concentrations of defects in the sputtered copper films

arising from various bias conditions. However, no clear conclusions could be made concerning differences in defect densities for different sputter bias conditions. For low sputter bias conditions (0W-150W), the super secondary grain growth mode is more pronouncedly present at room temperature, leading to reduced grain sizes and film coverage when these copper films are annealed directly after deposition. In case of low sputter bias conditions, the best results were found using a 10nm TaN/5nm α-Ta barrier layer, while smaller grain sizes and film coverage were found for other barrier types. In contrast, high sputter bias super secondary grains (~250W) are more pronouncedly present at elevated temperatures and lead to even bigger grain sizes (~ 500μm) and a nearly full super grain film coverage independent of the barrier composition/texture underneath. Moreover, in these high sputter bias copper films, two different stress relief mechanisms were observed, in contrast to low sputter bias conditions. Besides the SSGG growth mode, also hillock were formed in these films. These always appeared before the initiation of the SSGG growth mode.

The activation energy of the SSGG growth mode was estimated to be around 0.77eV, which was somewhat lower that the 0.93 eV that was found for SGG in ECD copper, which corresponds to copper grain boundary self-diffusion. This activation energy is independent of the used sputter bias conditions.

All the results in this work were discussed in terms of surface/interface energy density minimization and strain energy density minimization. It is known that normal grain growth happens when the driving forces act homogeneously, while if these driving forces act selectively, abnormal grain growth can occur. The main reason for such selectivity is an anisotropy of surface/interface energy and/or strain energy. For face-centered-cubic materials, the former promotes the growth of (111) orientations, while the latter favours the growth of (100) oriented grains. It is shown that the observed super grains are all (100) oriented and are driven by strain energy density minimization.

6.3 Introduction of super secondary grains in electroplated blanket copper films and features

In chapter 5, the main objective was to enhance the mean grain size and impact of the overburden on the grain size in electroplated copper blanket films and features by introducing super grains in the overburden using the knowledge on blanket wafer level of chapter 4.

In a first step, we focused on the microstructure and texture evolution of electroplated copper films of different thickness in combination with a thick sputtered copper seed layer. The layer thickness and sputter deposition conditions for these seed layers were chosen in such way that the SSGG mode was present in these seed layers. It was shown that super grains could be introduced in electroplated copper films of different thickness. However, the SSGG grain size decreases for thicker electroplated copper films. Nevertheless, the implementation of super grains in electroplated copper was an important step forward towards the introduction of these super grains in narrow features.

In a next step, the knowledge on blanket wafer level is used to initiate super secondary grains in structures. For this purpose, two different methods were proposed and their efficiency on initiating super grains in structures were tested. It is shown that super grains can be introduced in copper features up to 100nm. However, further optimizations are still necessary as the in-growth of super grains is still insufficient and there the texture of these super grains in structures can sometimes deviate from the super grains observed in blanket films.

6.4 Perspectives

As Cu/low-k interconnect lines further scales down to 45nm technology node, it is critical not only to deposit ultra-thin conformal barrier/seed layers inside the recessed features to provide a defect-free copper filling, but also to reduce the strong resistivity increase in those narrow structures. In order to reduce the resistivity increase in nanowires, it is important to further explore ways to increase the mean grain size in nanowires.

As already shown in this work, the introduction of super grains in sputtered and electroplated copper blanket films can be used to implement these super grains in small features up to 100nm. Despite the fact that these first results are already very promising, the impact of the overburden in-growth has to be further enhanced in order to achieve the expected super grains with the desired textures in nanowires. Moreover, further investigations on sub-100nm lines should clarify whether these super grains will also have an impact on the copper at the bottoms in the more advanced sub-100nm technology nodes, and thereby will offer a solution to reduce the resistivity of copper nanowires and the subsequent interconnect RC delay.

As grain growth in nanowires is limited by both dimensional constraints and impurity pinning, also finding ways to control the impurity concentration in nanowires remains an important research topic. This is because not only geometric constraints but also the impurity incorporation in narrow copper lines can retard grain growth in these narrow lines. So a better understanding of the two-dimensional distribution of different impurities in the cross section of wires and the characterization of the impurities that are trapped at the grain boundaries remains of great importance. This knowledge will then enable us to obtain a better understanding on how the impurities are incorporated into the lines during the plating process and in the following anneal process.

The combination of blanket Al sputter deposition and reactive ion etching (RIE) has been used for years to deposit and pattern aluminium features. By applying the same metallization scheme on blanket sputtered copper films containing columnar grown super grains with an in-plane grain size in the order of 500µm, in stead of the commonly used damascene patterning process, this may offer another opportunity to produce Cu features with bamboo type grain structures. However, using a reactive ion etch process to define features in copper is not trivial because copper is very difficult to dry-etch. In order to achieve reasonable etch rates, the substrate temperatures has to be increased during etching, which complicates the masking procedure and may also lead to additional problems due to the oxidation of copper at elevated temperatures and/or the corrosion of copper due to the gas chemistry. Up till now, only a few reports are available of successful copper etch of features, and in most of the cases this was only effective for structures with line widths above

2μm. Therefore, further improving the etch behaviour of copper is of great importance and remains an interesting research topic.

Once an adequate solution to overcome grain size limitations had been found, efforts can be directed to investigating the reliability of these copper interconnects. Electromigration related reliability problems are expected to severely limit the use of standard interconnects in future very large scale integrated circuits (VLSI). Electromigration describes atomic diffusion caused by the momentum exchange between electrical charge carriers and diffusing atoms [1] and has been the subject of intensive study, both theoretical and experimental, over the past 40 years. The reason for this interest is that electromigration can cause shorts in integrated circuit interconnect under conditions of normal use, resulting in circuit failure. In spite of this exhausting study, many aspects of electromigration are not well understood. This is due in part to many factors (grain structure, grain texture, interface structure, stresses, film composition, …) that influence electromigration and to the inability to isolate the effect of these factors experimentally. The reasons for the recent adoption of copper in stead of Al (Cu) alloys as a conductor in integrated circuit technology are its properties of low electrical resistivity and the supposed immunity from electromigration damage. The former is undoubtedly true, but the latter has been shown to be somewhat elusive. For Al interconnects, the electromigration resistance has shown to be dependent on the film's microstructure: longer lifetimes can result from larger grain sizes [2-3]. In some instances however, electromigration lifetime gains are due to more than just larger grains. With Al alloy films, a strong correlation between {111} texture and an increased electromigration lifetime has been observed [4, 5-7]. But whether this correlation also exists with Cu is not clear yet because of the limited data nowadays. Therefore, the electromigration behaviour of copper features as a function of their orientation remains an interesting research topic: the implementation of (100) oriented super grains in narrow features, in comparison to the usual observed strong {111} texture might help to get a better understanding of the electromigration related reliability of copper interconnects.

6.5 References of the chapter

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