Understanding Oxide Degradation Mechanisms in ultra-thin SiO_2 through High-Speed, High-Resolution in-situ Measurements

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Abstract

A model is proposed and validated for the degradation mechanisms occurring in ultra-thin SiO_2 at real operation conditions, based on high-resolution, high-speed in-situ measurements. This state-of-the-art set-up proves that oxide degradation still occurs at low stress conditions and allows distinguishing quantitatively the SILC-contribution from the contribution due to trapping.

Keywords: SiO_2; CVS; SILC; high-resolution measurement; charge trapping

1. Introduction

Due to the continuous downscaling, ultra-thin oxide devices operating under very low gate voltages, require special attention for the correct interpretation of the degradation behaviour. The prediction of oxide reliability under operating conditions still involves extrapolation beyond the range of gate voltages used in stress experiments, and this requires a trustful knowledge of the physical mechanisms involved in the generation of the oxide defects. The relative increase of the leakage current at low field (SILC) has already become an indirect standard method used for monitoring the oxide degradation [1]. In order to better understand the degradation mechanisms at real operation conditions, a high-resolution set-up has been developed at LUC/IMEC, allowing accurate SILC measurements at voltage levels as low as |Vg|=0.9 V, corresponding to actual device operating conditions. With this first generation measurement system we were able to demonstrate that oxide degradation still occurs under these low stress conditions and that the model of Nigam can be used to fit the measured data. Of great

importance for the understanding of the observed electrical behaviour is the demonstrated possibility to distinguish the contribution due to SILC and the contribution due to trapping. Through the use of an appropriate model, SILC-related parameters and trapping-related parameters can be quantified. At the lower voltage conditions, it will be shown that the contribution of the trapping component gets small when compared to the SILC contribution. The extrapolation of high voltage measurements to operating conditions is still possible taking into account these new results, but should be performed with care [2], [3]. Small values of trapping time and the low contribution of positive charge trapping compared with the SILC contribution, confirms the importance to detect small current changes after short stress time. As shown below, a second-generation measurement set-up has been developed at LUC/IMEC to achieve high-resolution current measurements in the microseconds time-range.

2. Devices and measurements

Planar MOS capacitors with 2.4 nm conventional oxides grown on p-type substrate were used for the purpose of this study. The capacitor area was 1.260 10^{-3} cm^2. A CVS is applied and the SILC is measured in-situ [3]. In total, 11 different stress voltages were applied: from –0.9V till –2.9 V in steps of 0.2 V, performed at 100 °C with a stability of 0.002 °C.

3. In-situ measurements and model

Even at these low voltages, the refined model of Nigam et al. [5] with some adaptations can describe the gate current behaviour:

$$J = J_0 + N^+ .\left[1 - e^{-t/\tau}\right] + \alpha . t^{\nu} \qquad (1)$$

with J the total current density, t the time, N^+ the saturation value of the current density component due to the positive charge trapping, τ the trapping time constant and α and ν the SILC-related parameters [5]. An alternative method for the determination of part of the fitting constants is used, fitting the current's derivative instead of the actual current density [3]:

$$\frac{dJ}{dt} = \frac{N^+}{\tau} .\left[e^{-t/\tau}\right] + \alpha . \nu t^{\nu-1} \qquad (2)$$

The derivative dJ/dt shows significant scattering particularly during the initial period of the measurement. A smoothing method, based on least structure method of Cook [6] is applied to the original measured data before taking the derivative. Equation (2) is then used to fit the derivative data and the parameter τ is determined in that way. Equation (1) is used to fit the measured data using a fixed value of τ as described extensively from Aresu at al. [3].

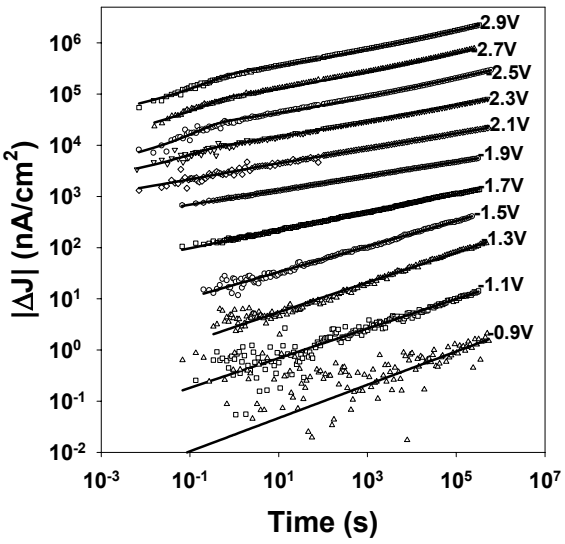

Fig.1 Dots: Change in current density as a function of time at 11 different voltages. Lines: fit with equation (1).

Figure 1 shows an overview of all the measurements that were performed during this study along with the model fitting. Besides the excellent fitting of the data, three distinct regions can be observed.

At high voltages, the trapping effect is superimposed on the straight-line SILC behaviour. However, at the lower measured voltages, the low contribution of positive charge trapping compared with the SILC contribution allowed fitting the measured data only with the second term of equation (1), resulting in a straight-line behaviour [3]. At the lowest voltages, the slope of the measured current gradually increases.

Figure 2 and 3 show the fit constants of equation (1) as a function of the gate voltage. As shown in

figure 2, the trapping time τ as a function of V_g, is nearly a constant value. The saturation value of the positive charge trapping N^+ decreases at low voltages.

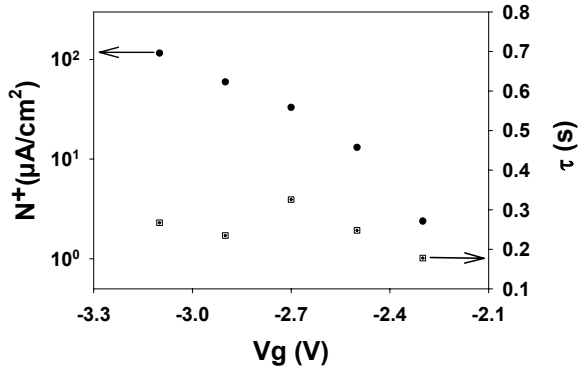

Fig.2 The fit constants N^+ (left axis) and τ (right axis) related to charge trapping as a function of V_g, Eq.1.

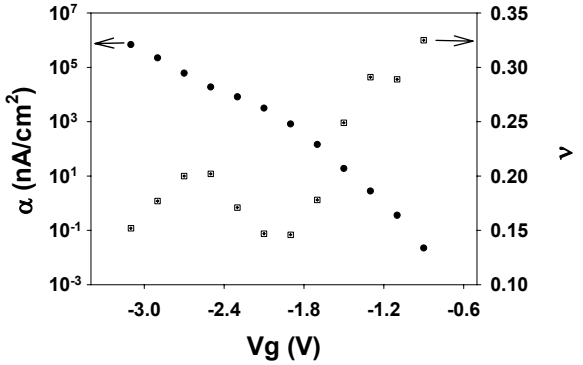

Fig.3 The fit constants α (left axis) and ν (right axis) related to SILC as a function of V_g, Eq.1.

The reduction can be explained by the smaller contribution of the charge trapping, as a consequence of the existence of fewer traps [1].

In figure 3, the SILC-related parameters are plotted. α is the leakage current caused by the traps generated after t=1 second and ν corresponds to the trap generation rate. The fit constant α decreases significantly at lower. The trap generation rate ν, as a function of V_g is nearly a constant value at high voltages as observed in literature, but increase drastically for voltages below –1.9V.

3. New generation high-speed, high-resolution measurement system

A complete new experimental system setup has been developed to monitor small current changes at high time resolution of the order of microseconds. This is important in order to determine the on-set of trapping so that the individual contributions of SILC and trapping can be distinguished in the complete time-frame of stress and therefore a full validation of the proposed model is obtained.

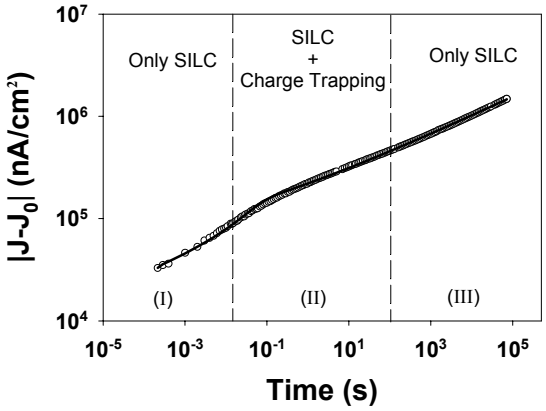

Fig.4 Dots: Change in current density as a function of time at Vg=-2.9V. Lines: fit with equation (1).

Figure 4 shows the current density as a function ot time at V_g=-2.9V with the model fitting. Compared to the previous measurements, a range of two more decades can be now analyzed. In the first interval (I), the charge-trapping component is almost negligible and the increasing current corresponds mainly to SILC, proving that the model is valid also in this region. In the second interval (II), the trapping effect is superimposed on the straight-line SILC behaviour and in the last interval (III), the current increases due to SILC. The same method, for the determination of the fitting constants, has been used and values of the same order have been found.

4. Conclusions

Ultra-thin SiO_2 layers were stressed at constant voltage and the SILC was measured in-situ with a high-resolution measurement system. A large gate stress voltage range was measured down to –0.9 V. The refined model of Nigam et al. [5] can describe

the gate current behaviour successfully by distinguishing the SILC-contribution from the trapping-contribution. At low voltages, it was observed that the contribution of the trapping component has no significant impact on the measured curves. Therefore, extrapolations from high voltage measurements towards operating conditions should be performed with care [3]. A new generation high-speed, high-resolution system setup has been developed to monitor small current changes at high time resolution of the order of microseconds and a complete analyses is possible.

Acknowledgements

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References

[1] Sune J., Jimenez D. and Miranda E. "Breakdown modes and breakdown statistics of ultra thin SiO_2 gate oxides ", *International Journal of High Speed Electronics and System*, Vol. 11, 2001, pp. 789-848.

[2] Aresu S., De Ceuninck W., Dreesen R., Croes K., Andries E., Manca J., De Schepper L., Degraeve R., Kaczer B., "High-resolution SILC measurements of thin SiO_2 at ultra low voltages", *Microelectronics Reliability*, Vol. 42, 2002, pp. 1485-1489.

[3] Aresu S., De Ceuninck W., Knuyt G., Mertens J., Manca J., De Schepper L., Degraeve R., Kaczer B., "A new method for the analysis of high-resolution SILC data", *Microelectronics Reliability*, Vol. 43, 2003, pp. 1483-1488.

[4] In-situ method patented by the LUC and IMEC, No. PCT/EP90/00291, April 19, 1990.

[5] Nigam T., Degraeve R., Groeseneken G., Heyns M. M., and Maes H. E., "A fast and sample methodology for lifetime prediction of ultra-thin oxides", Proceedings IRPS 1999, pp. 381-388.

[6] Cook B. C. "Least structure solution of photonuclear yield functions", *Nuclear Instruments and Methods*, Vol. 24, 1963, pp. 256-268.